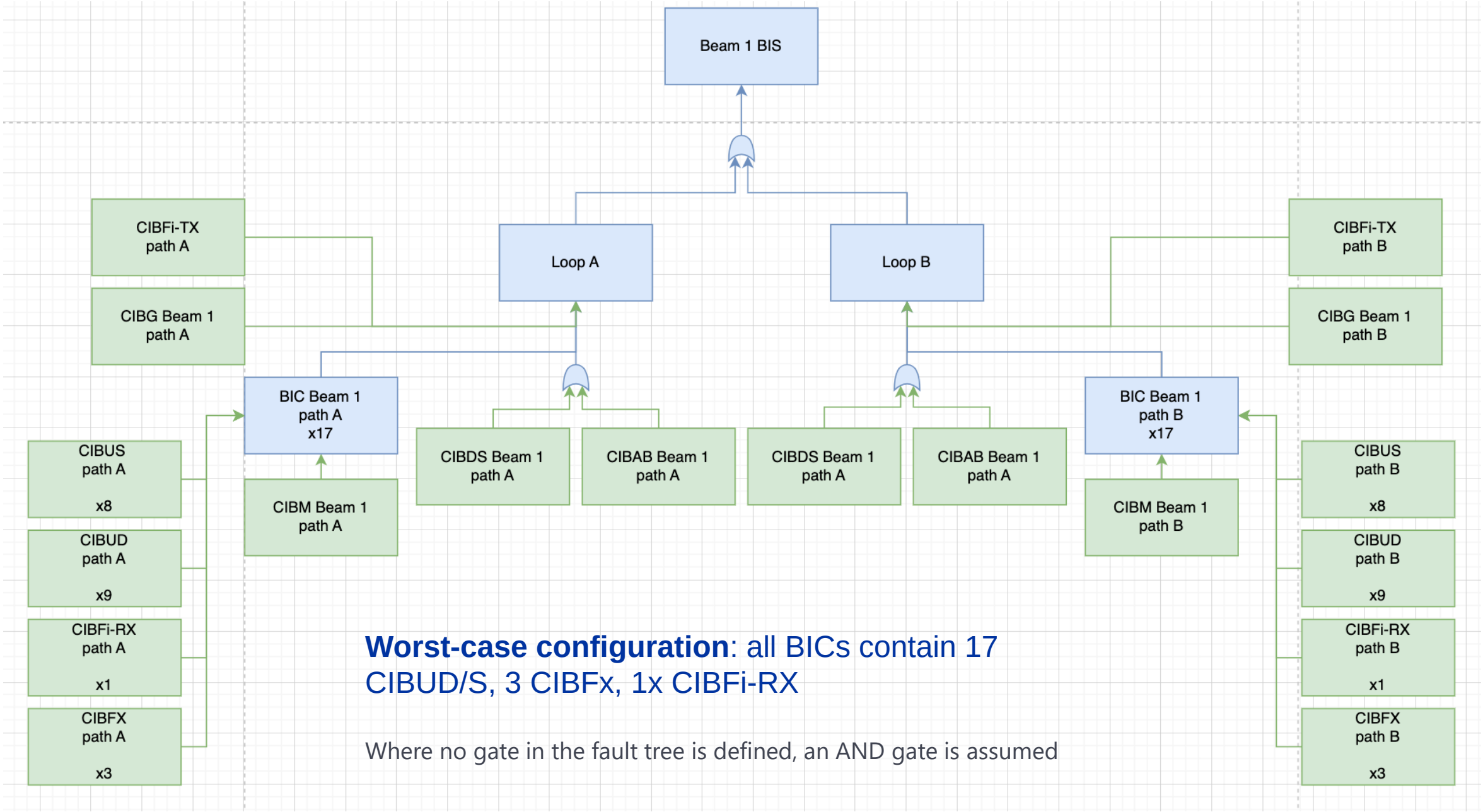
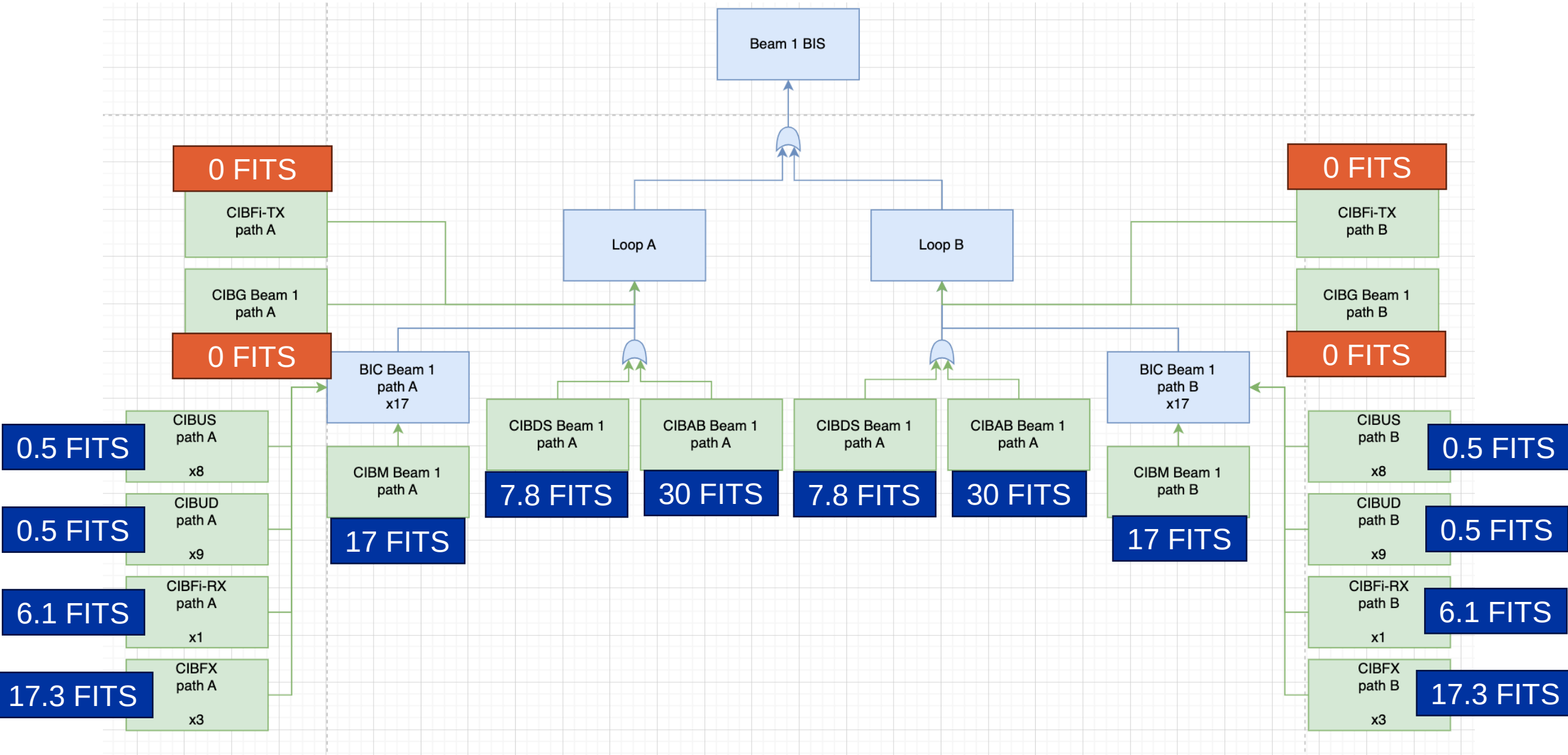
BISv2 Global Model

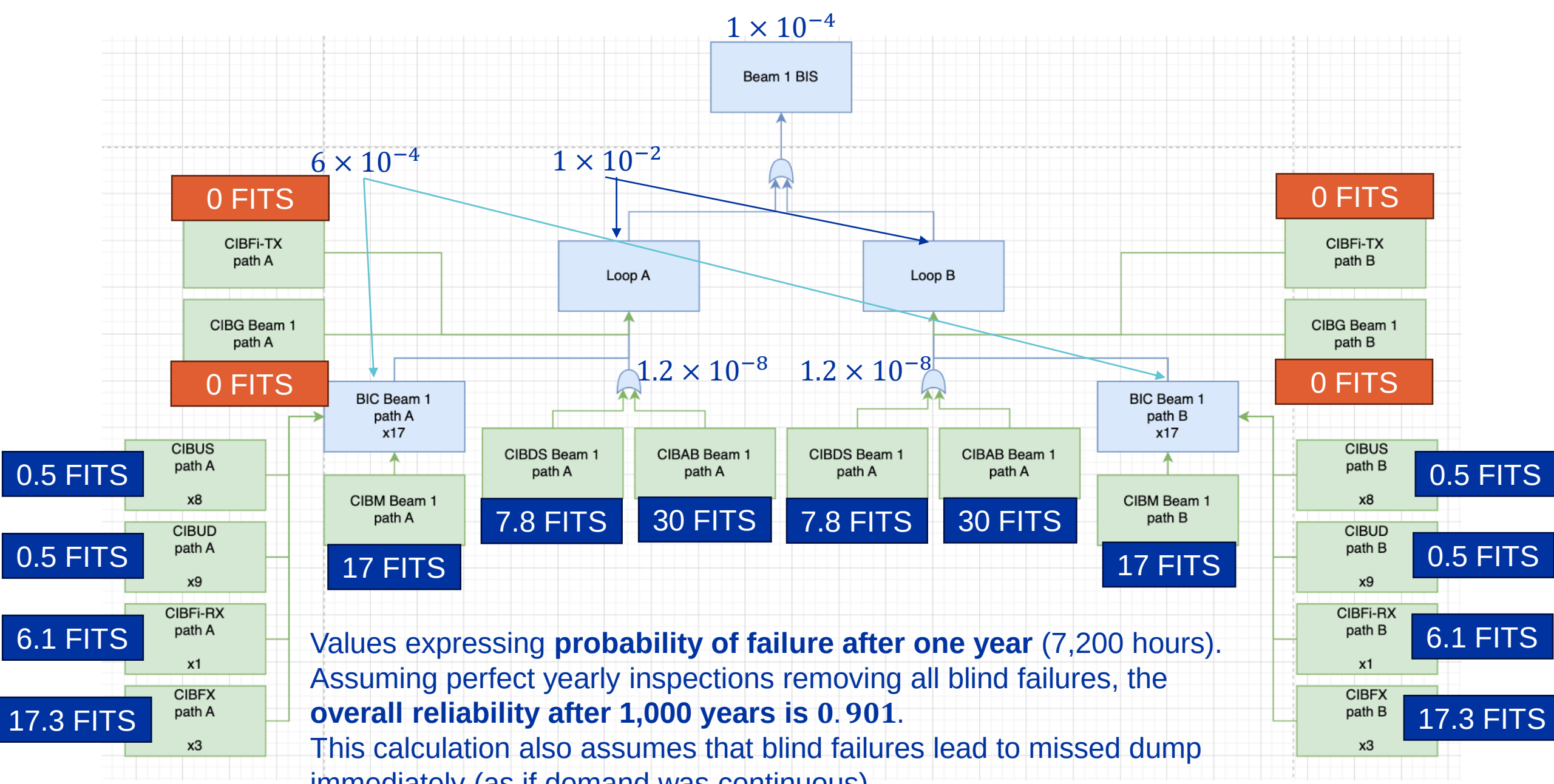
BISv2 Reliability Study Progress Meetings #7



Worst-case configuration: all BICs contain 17 CIBUD/S, 3 CIBFx, 1x CIBFi-RX

Where no gate in the fault tree is defined, an AND gate is assumed


Beam 1 BIS
Loop A
Loop B
0 FITS
CIBFi-TX path A
CIBG Beam 1 path A
0 FITS
BIC Beam 1 path A x17
CIBM Beam 1 path A
17 FITS
CIBDS Beam 1 path A
7.8 FITS
CIBAB Beam 1 path A
30 FITS
CIBDS Beam 1 path A
7.8 FITS
CIBAB Beam 1 path A
30 FITS
BIC Beam 1 path B x17
CIBM Beam 1 path B
17 FITS
0 FITS
CIBFi-TX path B
CIBG Beam 1 path B
0 FITS
CIBUS path A x8
0.5 FITS
CIBUD path A x9
0.5 FITS
CIBFi-RX path A x1
6.1 FITS
CIBFX path A x3
17.3 FITS
CIBUS path B x8
0.5 FITS
CIBUD path B x9
0.5 FITS
CIBFi-RX path B x1
6.1 FITS
CIBFX path B x3
17.3 FITS



Values expressing **probability of failure after one year** (7,200 hours).
Assuming perfect yearly inspections removing all blind failures, the **overall reliability after 1,000 years is 0.901**.
This calculation also assumes that blind failures lead to missed dump immediately (as if demand was continuous).

Boards

CIBM: 1 per path, in total 2 beams x 17 BICs x 2 loops (68 boards).

CIBUS & CIBUD: mulitple in each BIC, up to 17. Failure rate calcluated from “CIBU Channel”. (total – 160 boards)

CIBF & CIBFX: max 3 in a BICs (total 8 boards).

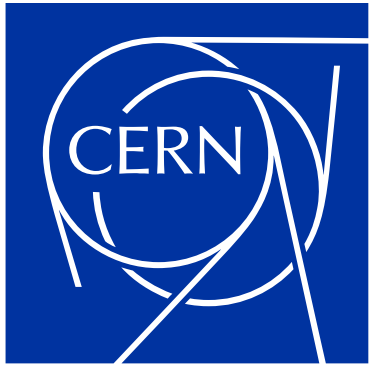
CIBAB: 1 per path, in total 2 beams x 2 loops (total 4 boards).

CIBDS: one shared across two loops, however: two independent paths inside (total – 2 boards).

- 7.8 FITS per path from an oscillator in ARTIX 7 IO page “FPGA wouldn't meet timing requirements, could potentially lead to a blind failure”

CIBG: one per beam; regardless: 0 FITS in blind failures (2 boards).

CIBFi-Rx: 3 x A&B (total – 4 boards)



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