Status WRPC (v5)

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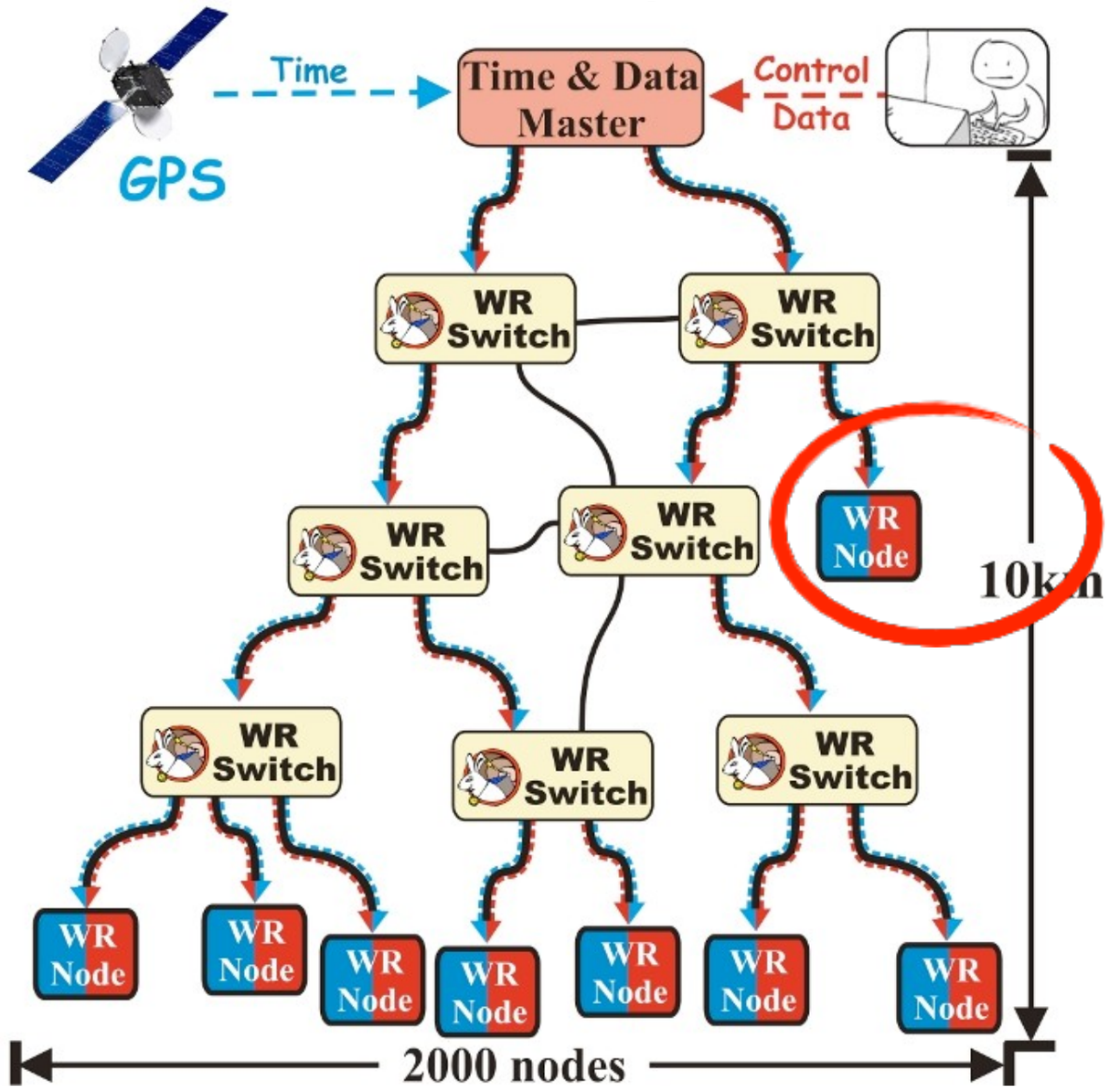
Agenda

- What is WRPC ?
- What is new in Release v5 ?
- Beyond v5

WRPC: **W**hite **R**abbit **P**recision time protocol **C**ore

What is WRPC ?

White Rabbit Precision time protocol Core



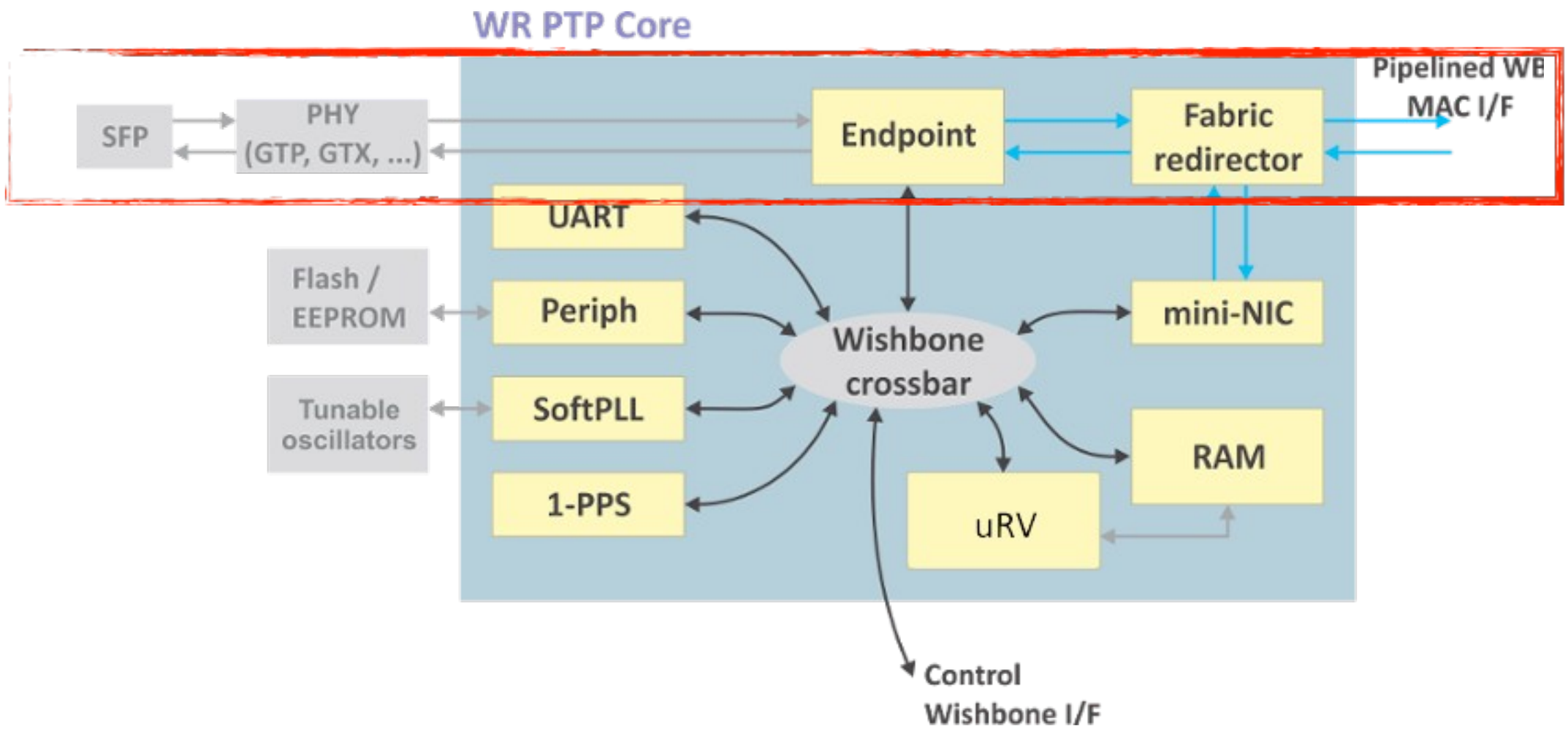
WRPC ?

- The HDL core used by nodes
  - Also requires some discrete components (VCXO, DAC…)
  - Part of it is shared with the switch (WRS)
- The software
  - PTP+WR, CLI, SoftPLL, …
- It’s open-source!

WRPC features: ethernet

WRPC is a network interface (1GB ethernet)

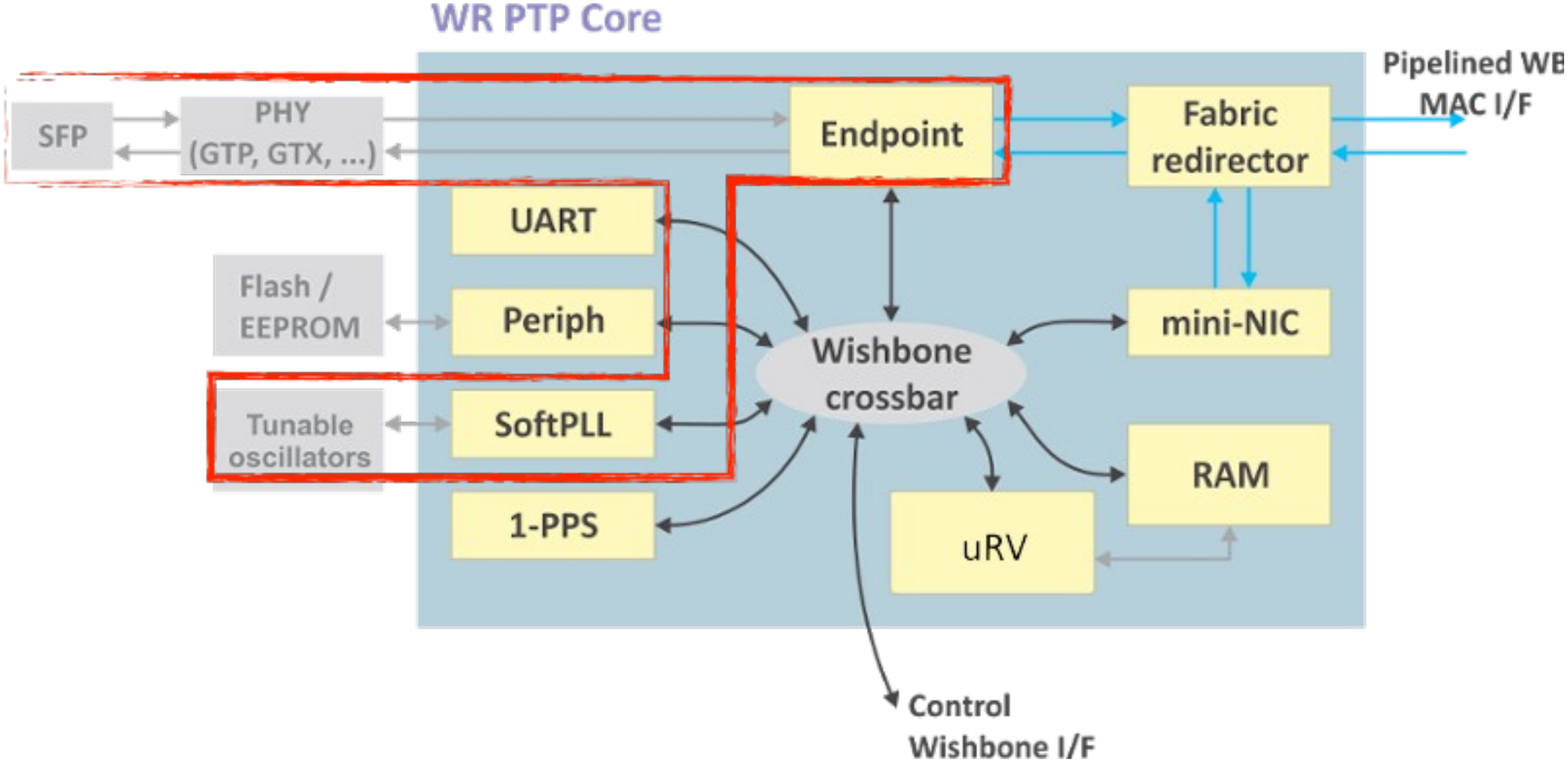
- For HW (streaming bus)



WRPC features: syntonisation

WRPC disciplines clocks

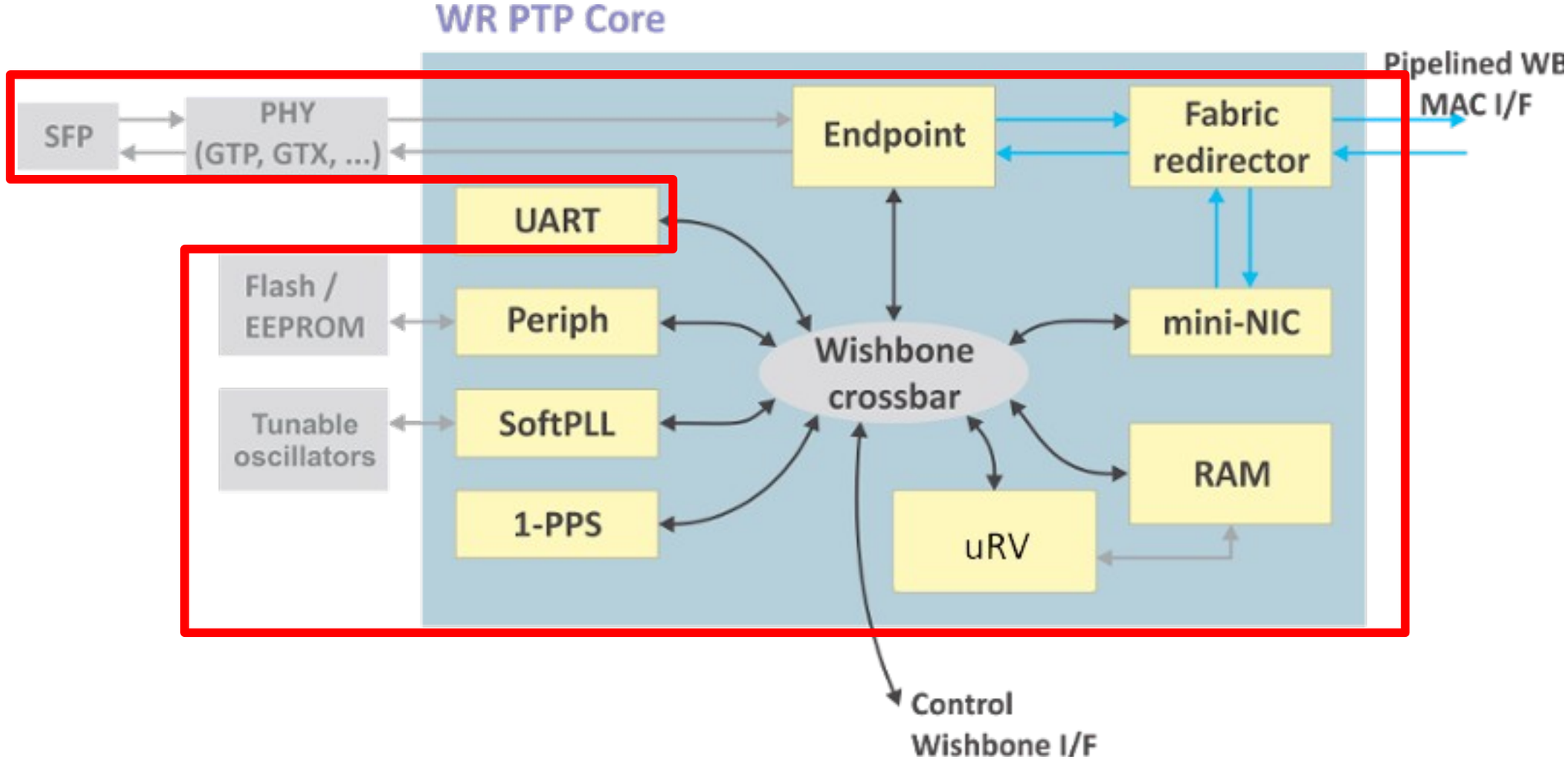
- Same frequency over the whole network (SyncE)



WRPC features: delay compensation

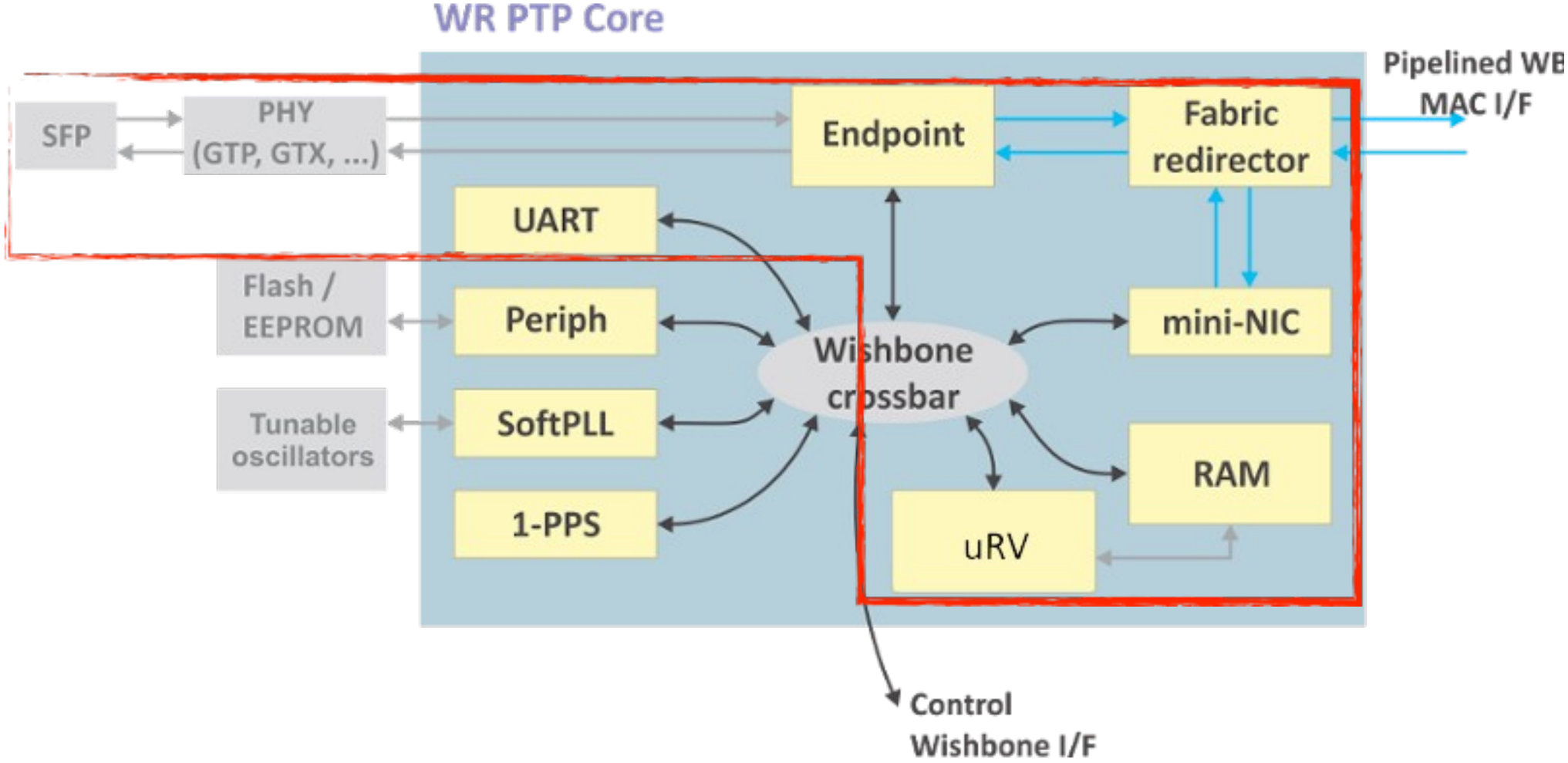
WRPC computes the network delay (using PTP)

- Provide absolute time



WRPC features: management and diagnostics

- Command line interface (uart + vuart)
- Standard protocols: SNMP, LLDP, ping, bootp, ...



WRPC documentation

Wrpc-user-manual-v5.0.pdf (~100 pages)

- User manual: CLI commands, features
- Designer manual: interfaces, how to insert the core in your design
- Memory map

Your feedback is always welcome!

New features in WRPC v5

New FPGAs

New FPGA: Xilinx Ultrascale+

Supported platforms:

- Xilinx AMD: Virtex 5, Spartan 6, Kintex 7, Artix 7, Zynq7, ZynqUS+
- Intel/Altera: arria2, arria5

  Note: not all platforms have been tested.

What does supporting a new FPGA mean ?

- Mainly its Gigabit Transceiver
  - The most complex part
  - Usually hard ip provided by the manufacturer
    - But we need to know the propagation delay
      - make it deterministic (bitslide + phase)
- Clocking (PLL)
- Demo board

Low phase drift calibration

Low phase drift calibration (LPDC) for Kintex-7

- Make delay-lines and clock dividers within the GT deterministic over reset.
- Improve phase stability (maximum deviation) to ~5ps (from ~75ps)
- Repeatedly resets the transceiver until clock phases are fixed on a previously calibrated value
- Cf: WHITE RABBIT AND MTCA.4 USE IN THE LLRF UPGRADE FOR CERN'S SPS

https://ohwr.org/project/white-rabbit/wikis/uploads/76d4587a2943d1ed0a1d605242d1979c/THBR02.pdf

Diagnostics

Diagnostics written in DPRAM

- Instead of registers
- That’s mostly technical
- But also changes the memory map

Risc-V CPU

Risc-V cpu instead of LM-32

- Risc-V is little-endian, while LM-32 is big-endian
- CPU memory is not anymore directly mapped to the host
- Debugging is now possible
  - wrpc gdbserver

Head less

- netconsole
  - console over UDP
- Can send a command over SNMP
- Can set init script over SNMP
- Allow head-less (without uart) systems
- Any WRPC can be controlled and diagnosed from the network

GUI

- change of gui command

```
WRRF WRPC Monitor 417046c | Esc/q = exit; r = redraw

TAI Time: 2024-03-19-14:13:37  UTC offset: 37   PLL mode: BC  state: Locked
---+-------------------+-------------------------+---------+---------+-----
 # |        MAC        |       IP (source)       |    RX   |    TX   | VLAN
---+-------------------+-------------------------+---------+---------+-----
 0 | e8:eb:1b:46:3d:b4 | BOOTP running           | 16450201| 7052933 |    0

--- HAL ---|------------ PPSI ------------------------------------------------
 Itf | Frq |  Config   | MAC of peer port  |    PTP/EXT/PDETECT States    | Pro
-----+-----+-----------+-------------------+------------------------------+-----
 wr0 | Lck | auto      | 64:fb:81:2f:cc:35 | SLAVE    /IDLE      /EXT_ON | R-W
Pro(tocol): R-RawEth, V-VLAN, U-UDP

--------------------------- Synchronization status ---------------------------
Servo state:          White-Rabbit: TRACK_PHASE

--- Timing parameters ------------------------------------------------------
meanDelay         :              168.380 ns  err state:      76
delayMS           :              168.380 ns  err offset:     75
delayMM           :              855.133 ns  err delta:      6
delayAsymmetry    :                0.000 ns
delayCoefficient  :   +0.000000000000000000  fpa   0
ingressLatency    :                1.000 ns
egressLatency     :                0.998 ns
semistaticLatency:                 0.000 ns
offsetFromMaster  :               -0.000 ns
Phase setpoint    :               30.420 ns
Skew              :               -0.003 ns
Update counter    :               200667 times
Master PHY delays TX:               237.687 ns   RX:           278.687 ns
Slave  PHY delays TX:                 0.998 ns   RX:             1.000 ns

Aux clock 0 status:        monitor
```

Generalized host tool: wrpc

- Simplify ports to new board
- Uniform CLI

```
>./wrpc board
List of boards:
 pci
 spec
 ertm14
 vme
 wr2rf
```

```
>./wrpc help
usage: ./wrpc [command] [OPTIONS...]
command is one of:
 help                - display list of commands (this help), or help for a
command
 version             - display tool version
 board               - display list of supported boards, or help for a board
 load                - load wrpc firmware and restart
 vuart               - virtual uart, connect to wrpc cli
 info                - display wrpc info and check board
 spll-recorder       - SoftPLL log recorder
 gdbserver           - risc-v gdb-sever
 wdiags              - WR diags dumper
 aux-logger          - display wdiag AUX0 value for logging
```

Misc

- Preliminary support of IEEE1588 HA profile
- Disciplining Si57x oscillator
  - Fractional frequency (eg: 100Mhz)
  - That’s experimental
- sfp database (stored in eeprom) has changed
  - Must be reprogrammed

Beyond v5 – the future

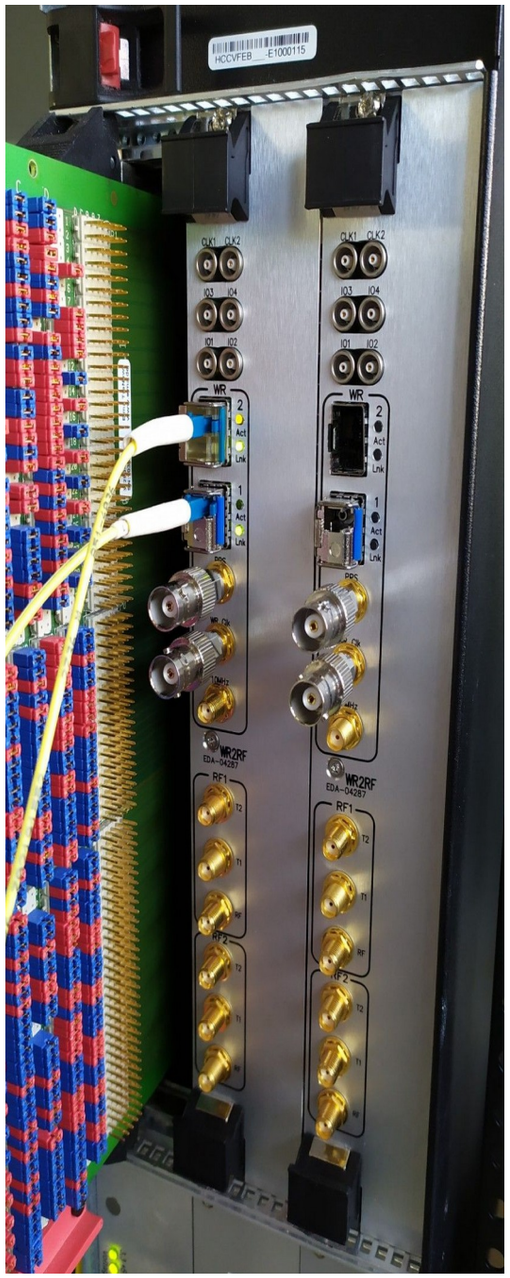
Next developments

- IEEE 1588 HA
- Exposing leap second flag in hw
- Fractional PLL support
  - Both internal and external (eg: Si534x)
  - No more need for DACs ?
  - No more need for external oscillator ?
- New reference board
  - Based on ZynqUS ?

And for discussion

- More RAM available in latest FPGA
  - More room for SW features
  - What do we want to add ?
- SoC FPGA
  - Use of the CPU for WRPC (eg: R5 in ZynqUS) ?
- Time to sync and lock
  - Can it be reduced from 1min to 30s ? 10s ?
- Double link
  - Redundancy ?

And for discussion



```
WRRF WRPC Monitor wrpc-v5.0-pre1-1071-g7ad2bc4c-d | Esc/q = exit; r = redraw

TAI Time: 1970-01-01-00:03:42  UTC offset: 37   PLL mode: BC  state: Locking
---+-------------------+-------------------------+---------+---------+-----
 # |        MAC        |       IP (source)       |    RX   |    TX   | VLAN
---+-------------------+-------------------------+---------+---------+-----
 0 | e8:eb:1b:46:3d:b4 | BOOTP running           |    1132 |     633 |    0
 1 | e8:eb:1b:46:3d:b5 | BOOTP running           |    1358 |     407 |    0

--- HAL ---|------------ PPSI ------------------------------------------------
 Itf | Frq |  Config    | MAC of peer port  |    PTP/EXT/PDETECT States    | Pro
-----+-----+------------+-------------------+------------------------------+-----
 wr0 | Frq | auto       | 64:fb:81:2f:cc:35 | UNCALIBR /WR_S_LOCK /EXT_ON | R-W
 wr1 | Frq | auto       | 64:fb:81:2f:cc:33 | UNCALIBR /WR_S_LOCK /EXT_ON | R-W
Pro(tocol): R-RawEth, V-VLAN, U-UDP

-------------------------- Synchronization status --------------------------
Servo state:          White-Rabbit: SYNC_TAI            0/1
meanDelay        :              436.996 ns
delayMS          :              436.996 ns
delayMM          :              873.993 ns
delayAsymmetry   :                0.000 ns
delayCoefficient :   +0.00000000000000000  fpa   0
ingressLatency   :                1.000 ns
egressLatency    :                0.990 ns
semistaticLatency:                0.000 ns
offsetFromMaster : 1710861093.803961067003 sec
Phase setpoint   :                0.000 ns
Skew             :                0.000 ns
Update counter   :                  183 times
Master PHY delays TX:               0.000 ns   RX:            0.000 ns
Slave  PHY delays TX:               0.000 ns   RX:            0.000 ns

Servo state:          White-Rabbit: SYNC_TAI            1/1
meanDelay        :              486.805 ns
delayMS          :              486.805 ns
delayMM          :              973.611 ns
delayAsymmetry   :                0.000 ns
delayCoefficient :   +0.00000000000000000  fpa   0
ingressLatency   :                0.000 ns
egressLatency    :                0.000 ns
semistaticLatency:                5.600 ns
offsetFromMaster : 1710861093.803960889195 sec
Phase setpoint   :                0.000 ns
Skew             :                0.000 ns
Update counter   :                  185 times
Master PHY delays TX:               0.000 ns   RX:            0.000 ns
Slave  PHY delays TX:               0.000 ns   RX:            0.000 ns
ERROR: slave_handle_followup: Slave was not waiting a follow up message
Aux clock 0 status:
```

Thanks!