WR-related standardisations

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Agenda

- WR and HA in IEEE1588
- WR vs. HA and migration
- WR-related standardisations:
  - P1588e
  - P1588f
- Conclusions

WR extends IEEE1588-2008 (PTP v2.0)

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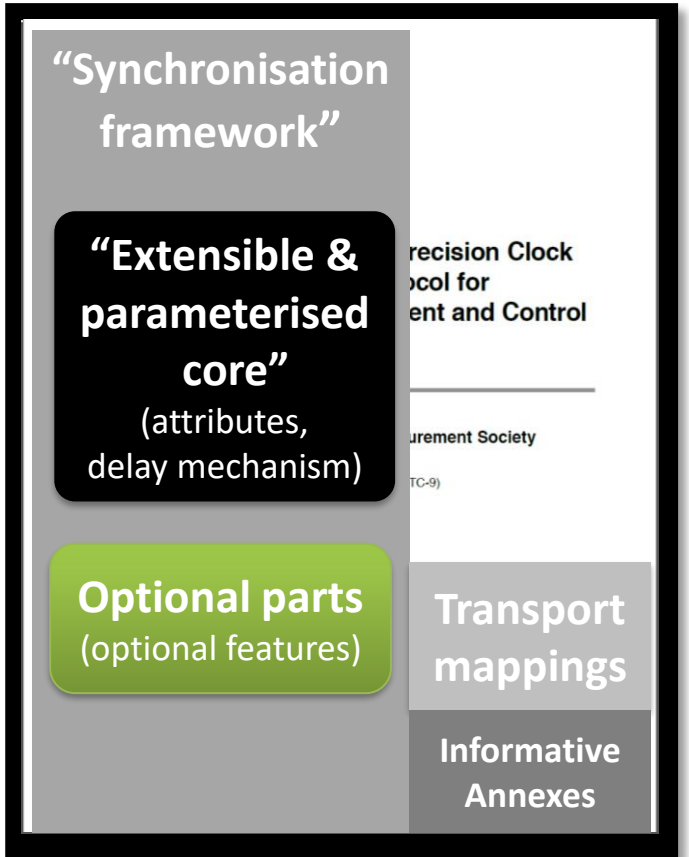

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"Extensible & parameterised core"
(attributes, delay mechanism)

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Optional parts
(optional features)

Transport mappings

Informative Annexes

Telecom

Applications

Power

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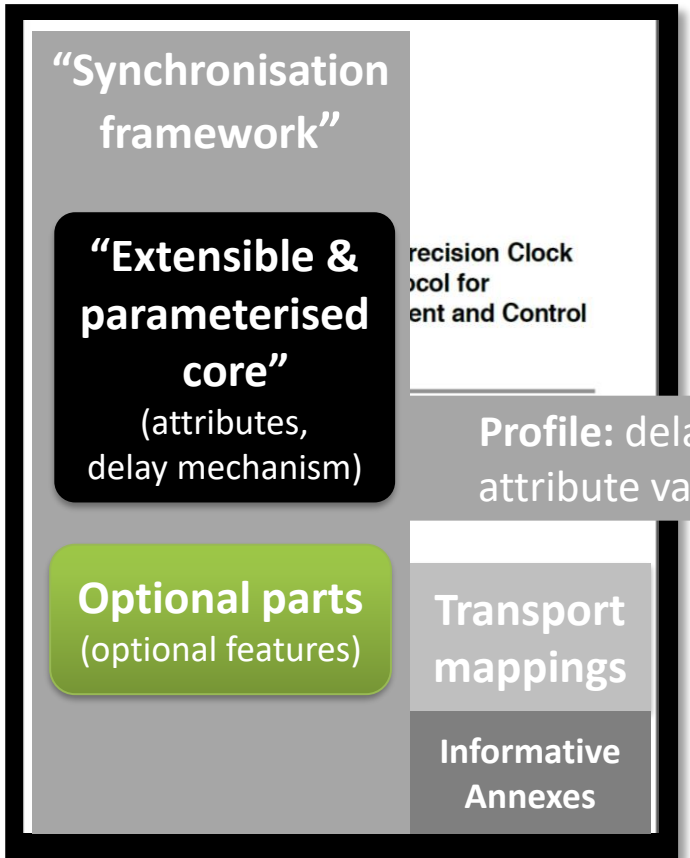

Profile: delay mechanism, attribute values & options

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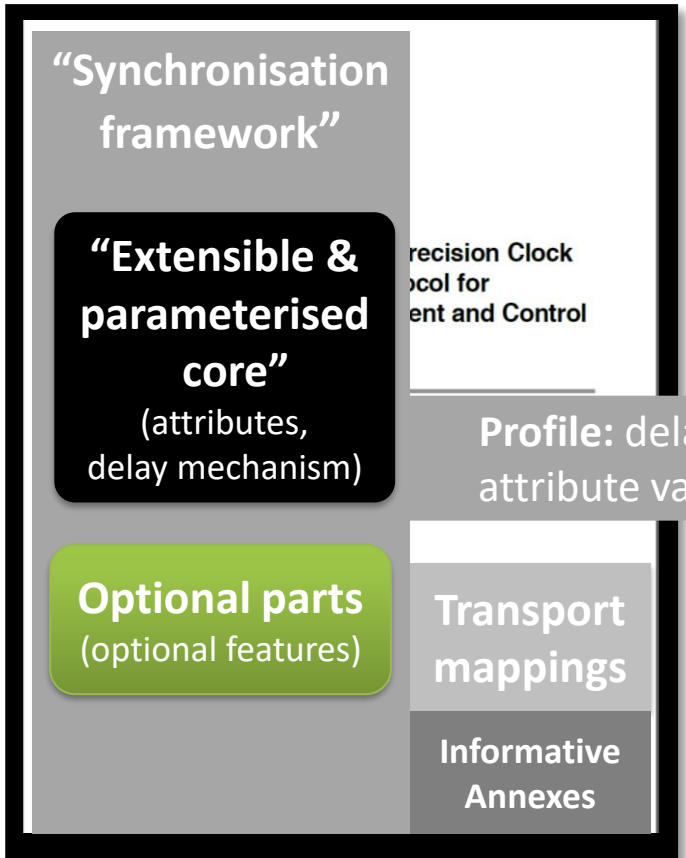

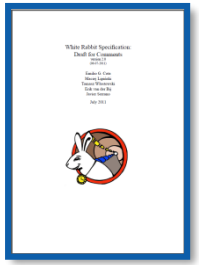

WR-PTP

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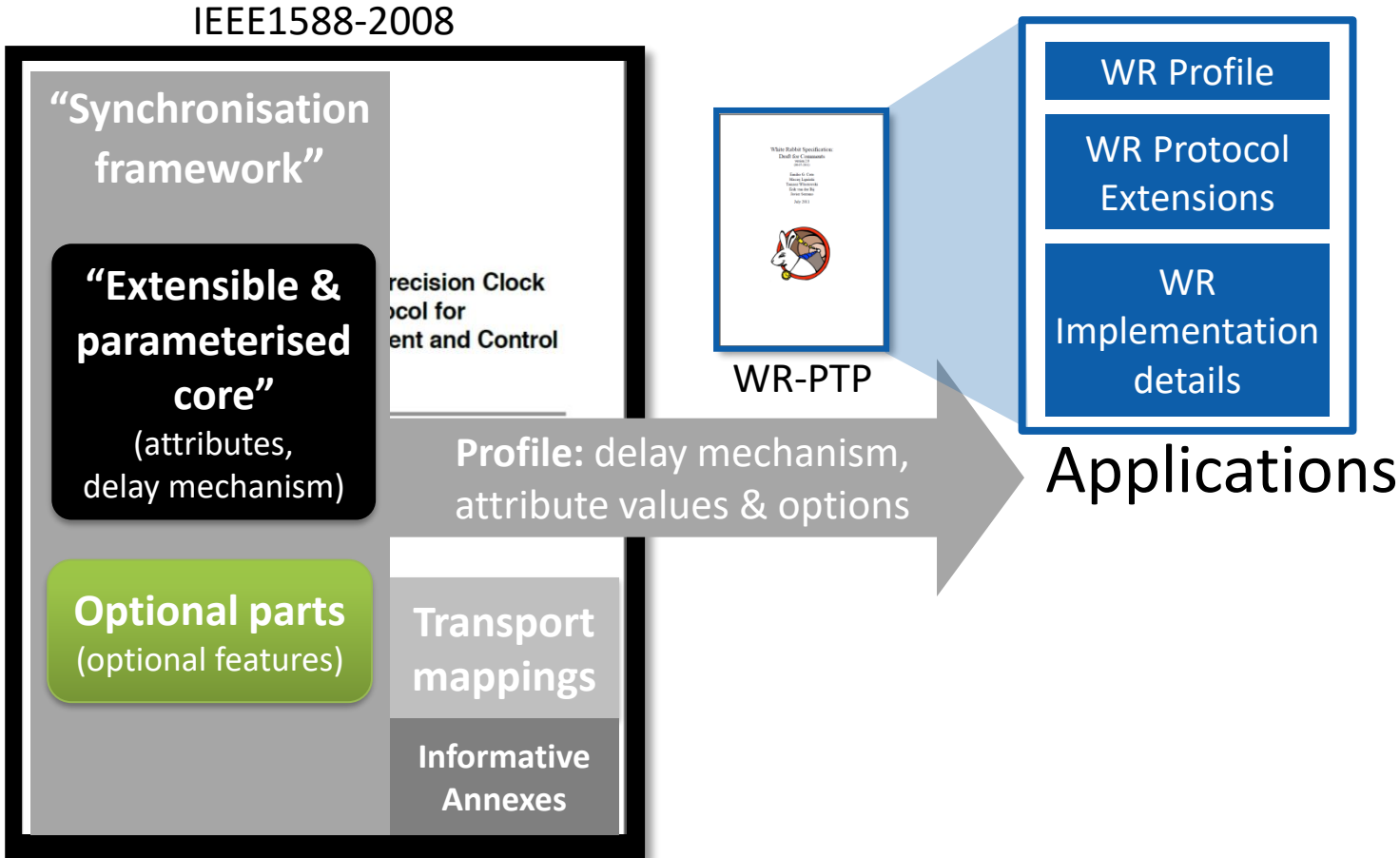

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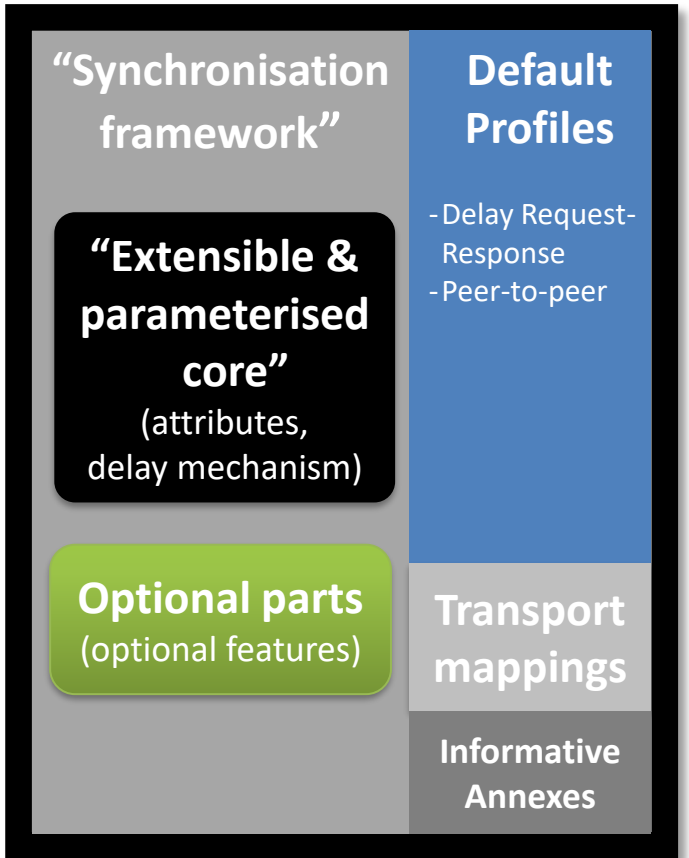

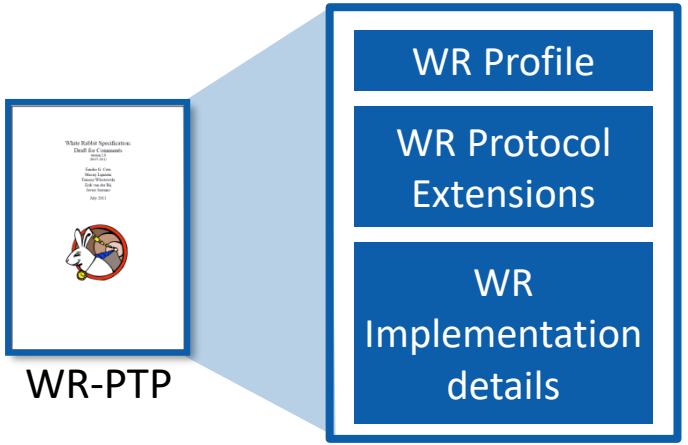

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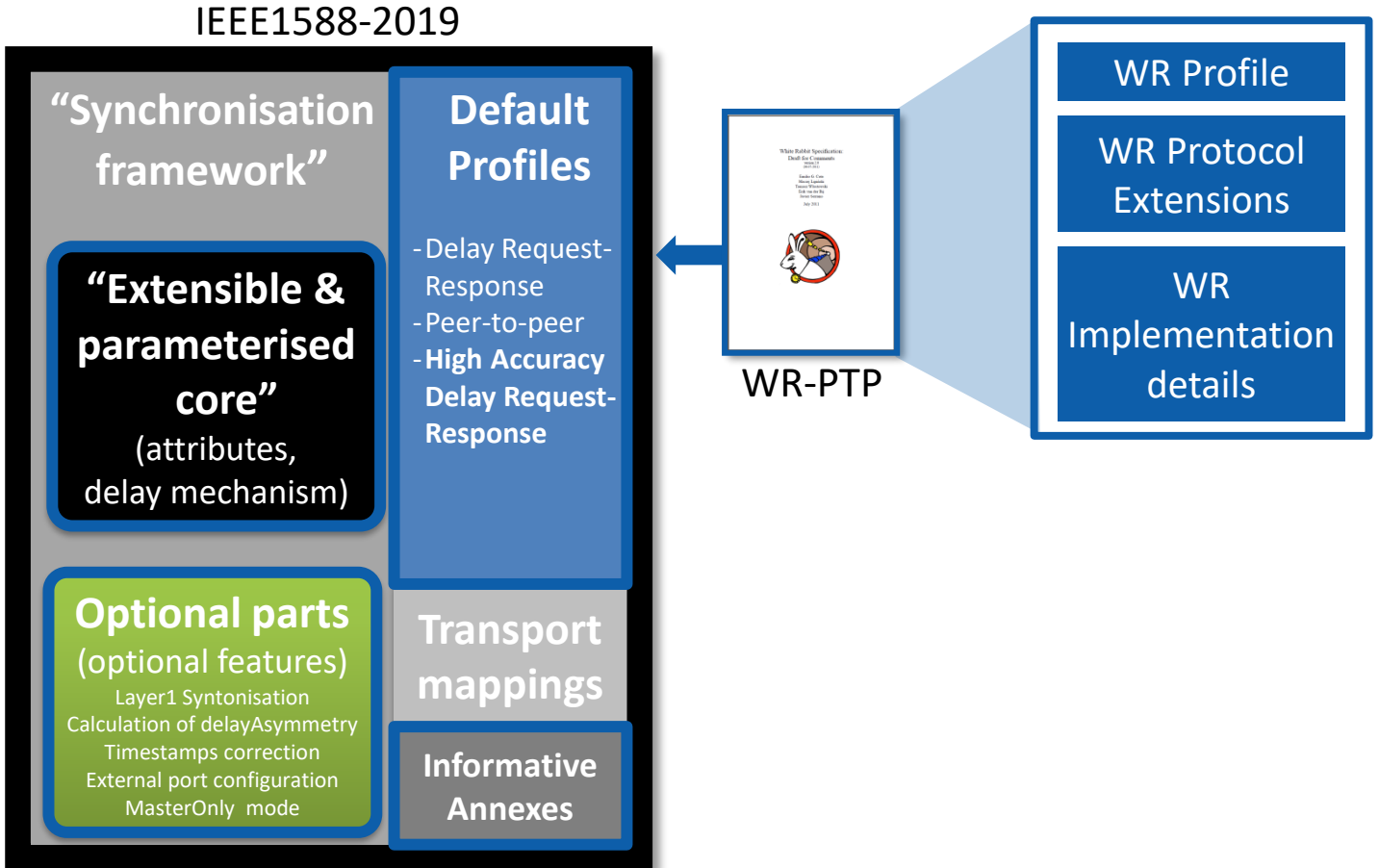

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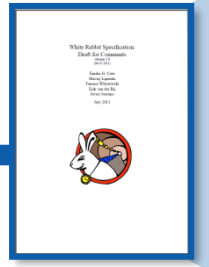


WR-PTP

- WR Profile
- WR Protocol Extensions
- WR Implementation details

WR Profile vs. HA Profile

- **Detailed description:** https://ohwr.org/projects/wr-std/wiki/wrin1588#translation-of-wr-parts-into-ieee1588-2019-annexesclause
- **Hardware / gateware:** WR Profile = HA Profile
- **Protocol / software:** WR Profile ≠ HA Profile -> migration required

Migration from WR Profile to HA Profile

- **Migration strategy:**
  WR Nodes (WRPC) will support either **WR Profile** or **HA Profile**
  WR Switches (WRS) will support both **WR Profile** and **HA Profile**
  will provide interoperability between the legacy (WR) and new (HA) devices
  Insitu calibration will be introduced with HA Profile
  Absolute Calibration will be introduced with HA Profile
- **Migration steps:**
  - **2018-2019** : Compliance tests for **WR Profile** and **HA Profile** (see)
  - **2019** : Prototype **HA Profile** on the WR Switch
  - **2020/2021** : WRS-3 v6.0 release – prepared for **WR Profile** together with **HA Profile**
  - **2023** : WRPC v5.0 release – **HA Profile** prototype tested on WRPCv5
  - **2024** : WRS-3 v7.0 release – **WR Profile** (default) and **HA Profile** with auto-negotiation
  - **2024** : WRPC v5.x release – configurable **WR Profile** or **HA Profile**
  - **202x** : WRS-3 v7.x release – **WR Profile** and **HA Profile** (default) with auto-negotiation

Ongoing WR-related standardistion works

- **IEEE P1588 Working Group** – amendments of IEEE1588-2019
  - P1588e – MIB and YANG Data Models (approved, to be published)
  - P1588f – Enhancements for Latency and/or asymmetry calibration (WG ballots)
    - Part A: In-situ calibration
    - Part B: Absolute calibration
    - Part C: MIB
- **SNIA, Transceivers subgroup** – amendments of standard(s) defining SFP's EEPROM
  - Addition of parameters required by Absolute Calibration in EEPROM space of SFPs as optional values, see: https://ohwr.org/project/sfp-plus-i2c/wikis/sff_std
  - First ballot completed
  - Common interest with Mobile Optical Pluggables Alliance (MOPA)
  - Details in presentation by Peter Jansweijer

P1588e – MIB and YANG Data Models

- Motivation
  - In WR Networks SNMP is used for monitoring
  - There is no official MIB for IEEE1588-2008 (PTPv2.0)
  - P1588 WG was to introduce official YANG management model for IEEE1588-2019
  - To facilitate uptake of WR, we pushed to also add an official MIB
  - Not enough resources in WRPC to implement YANG
- Adam Wujek was tasked to write the MIB
- MIB/YANG amendment to IEEE1588-2019 consists of
  - Normative clause to be added to the standard
  - MIB mapping of PTP data sets
    - MIB maps **all** datasets into OIDs (including HA)
    - All OIDs are optional
- **Status**: Approved by IEEE SA, to be published

P1588f Part A – In-situ calibration

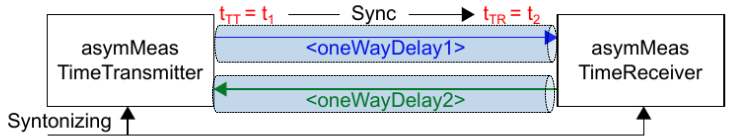
- Motivation
  - Calibration of asymmetry in already-deployed fibers
  - Needed in telecom, already standardized by ITU-T and IEEE802.1AS
  - Needed in long-distance WR links
- P1588f amendment adds “Delay asymmetry measurement mode” of PTP Port which
  - Excludes the PTP Port from BMCA
  - Allows transmission of desired PTP messages
  - Collects bursts of timestamps and makes them available to management
  - Optionally calculates <delayAsymmetry> and <delayCoefficient>
  - Expects control and configuration by a Network Management System (not automatic)
  - Two methods: Swapping of one-way delay (SOWD) and Three one-way delays (TOWD)
- **Status**:
  - 2nd Working Group ballot (3rd to be started, then 1-2 SA Ballots, expected completion 2025)
  - Proof-of-concept implementation

P1588f Part A – Swapping of one-way delay (SOWD)

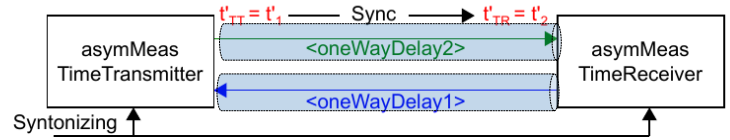
- Meant for duplex unidirectional fibers, already used in telecom
- Applicable to single bidirectional fibers, potentially useful in WR
- Requires
  - Physical swapping of fibers/SFPs between step 1 and 2
  - Syntonization during the measurement (e.g., via the same or another link, or holdover)
  - Collection of t_1, t_2

a) Using Sync messages (t_1, t_2)

Step 1:



Step 2:



$$< \text{oneWayDelay1} > = (t_{TR} - < \text{trOffset} >) - t_{TT}$$

$$< \text{oneWayDelay2} > = (t'_{TR} - < \text{trOffset} >) - t'_{TT}$$

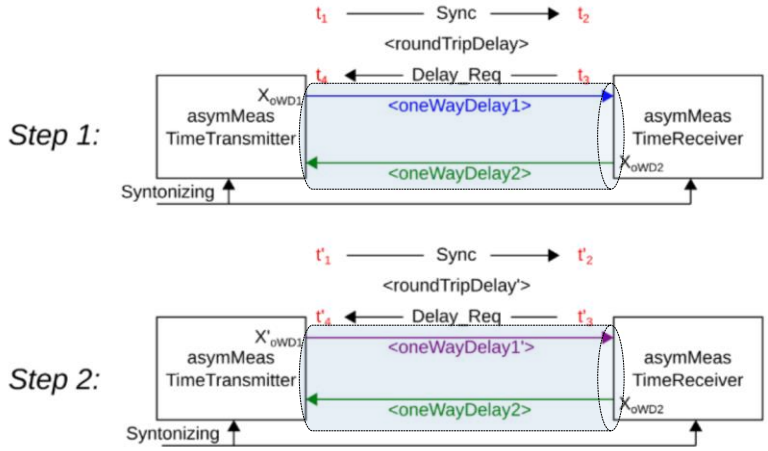
$$< \text{delayAsymmetry} > = \frac{< \text{oneWayDelay1} > - < \text{oneWayDelay2} >}{2}$$

$$= \frac{((t_{TR} - < \text{trOffset} >) - t_{TT}) - ((t'_{TR} - < \text{trOffset} >) - t'_{TT})}{2}$$

$$= \frac{t_{TR} - t_{TT} - t'_{TR} + t'_{TT}}{2}$$

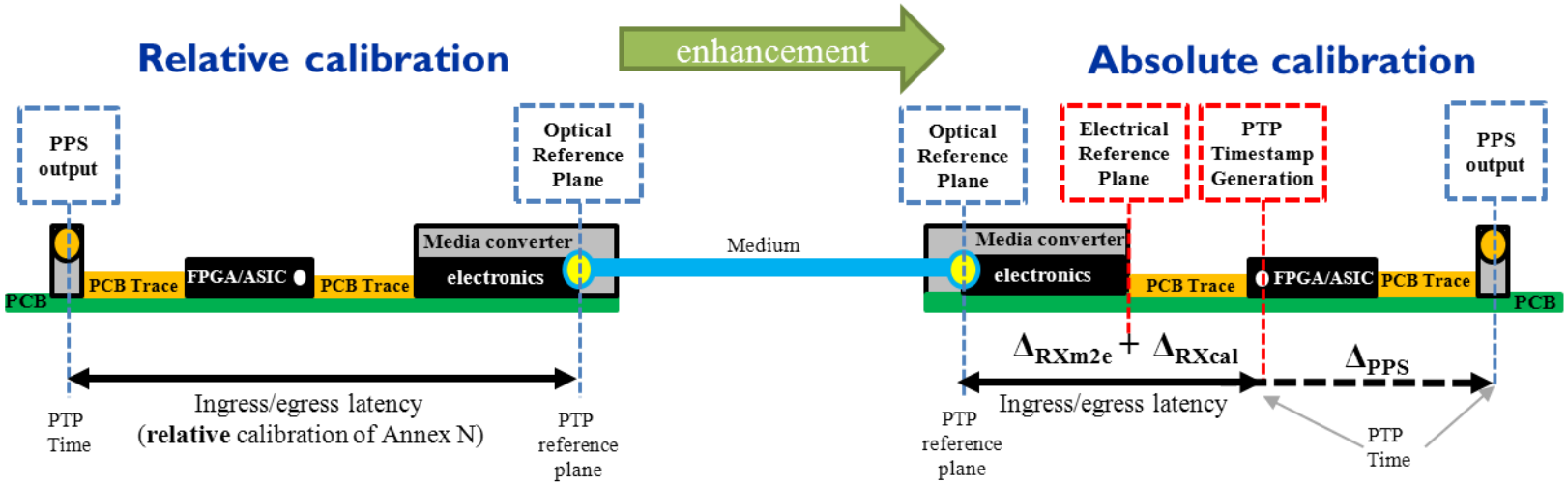
P1588f Part A – Three one-way delays (TOWD)

- Meant for single bidirectional fibers
- Developed by Peter Jansweijer
- Requires
  - Tunable SFP on one end
  - Syntonization during the measurement (e.g., via the same or another link, holdover)
  - Linear dependence between medium characteristics (X_{oWD}) and medium delay
  - Collection of t_1, t_2, t_3, t_4



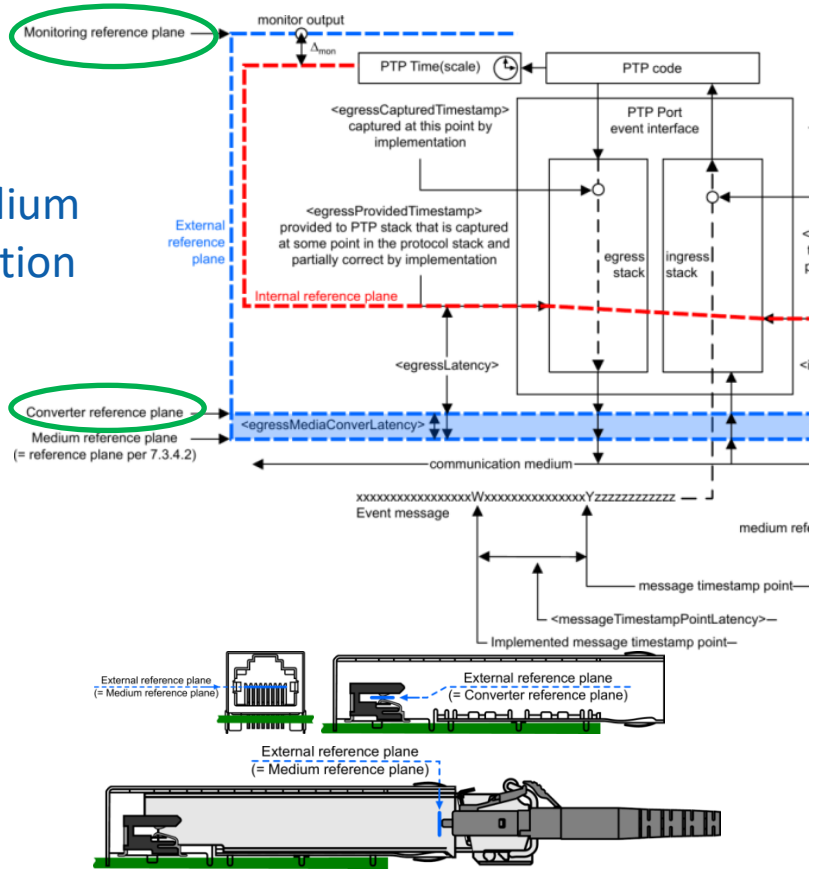
$$< \text{delayAsymmetry} > = \frac{(X_{oWD1} - X_{oWD2}) \cdot (< \text{roundTripDelay} > - < \text{roundTripDelay}' >)}{2 \cdot (X_{oWD1} - X'_{oWD1})}$$

P1588f Part B – Absolute Calibration



P1588f Part B – Absolute Calibration

- Explains absolute vs. relative calibration
- Defines new reference planes:
  internal, external, monitoring, converter, medium
- Explains concepts relevant to absolute calibration
- Defines “media converter latency”
  - Residual
  - Specific to media converter
- Status:
  - 1st Working Group Ballot – ongoing
  - expected completion 2025

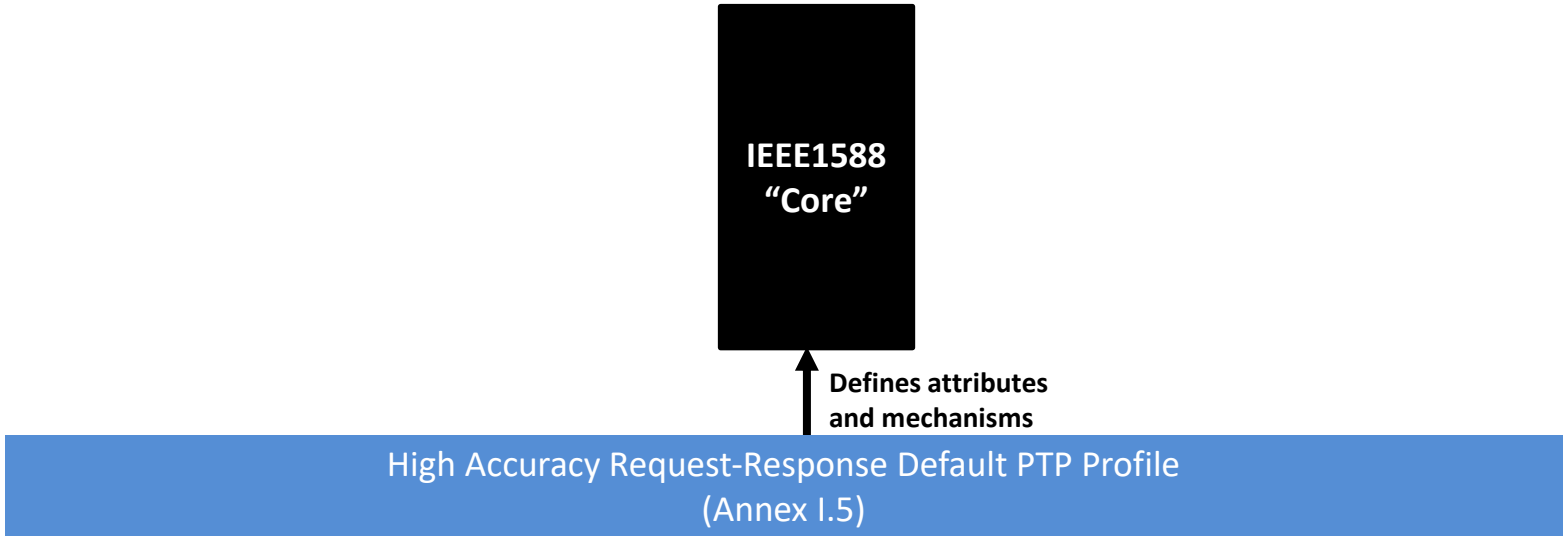


Conclusions

- White Rabbit is an open source sub-ns implementation of
  - **WR Profile** which extends IEEE1588-2008, and
  - **HA Profile** of IEEE1588-2019
- Compliance tests developed for
  - **WR Profile** to ensure backward compatibility and long-term support
  - **HA Profile** to ease implementation
- **HA Profile** – non-default configuration choice in upcoming WRS release v7.0
- Ongoing work on
  - In IEEE: in-situ and absolute calibration, official MIB
  - In SNIA: storage of media converter latencies and their characteristics

Backup slides

High Accuracy Default PTP Profile



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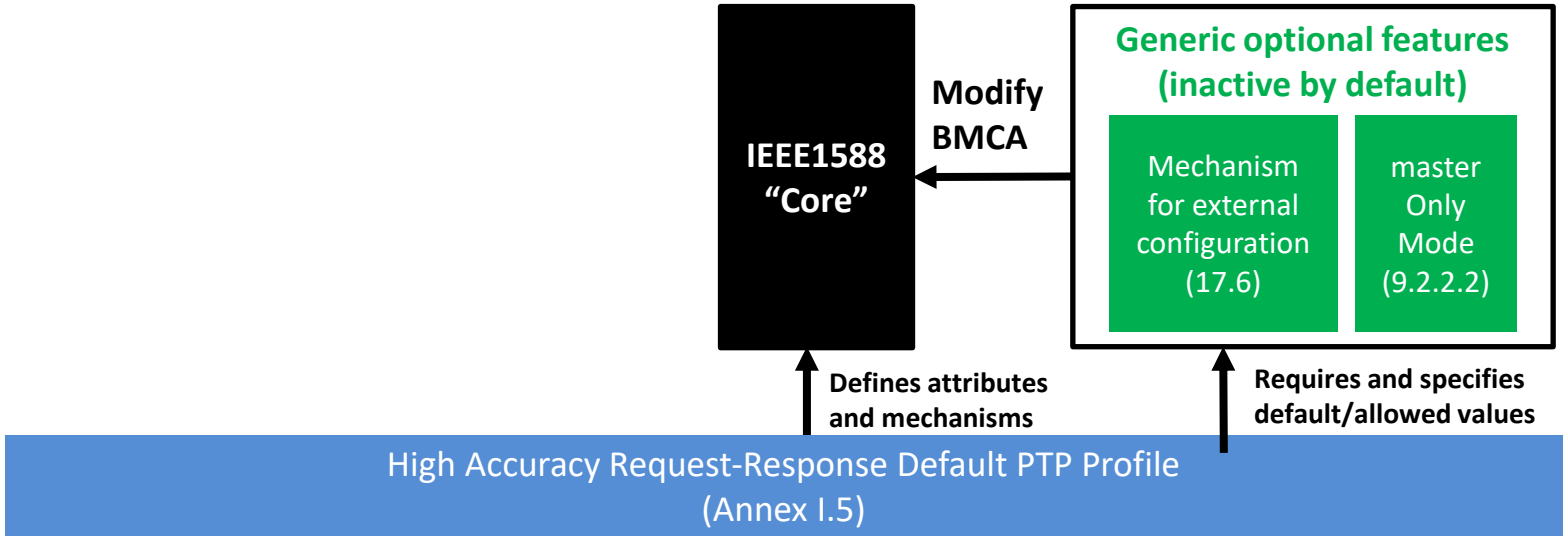

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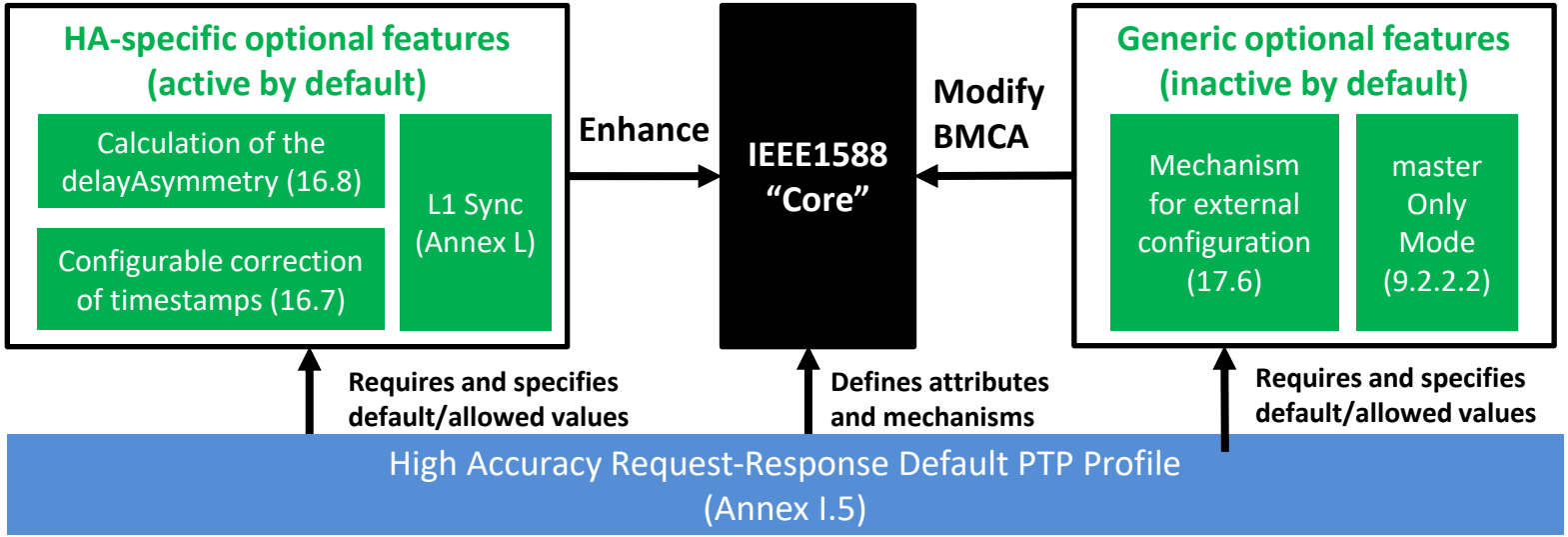

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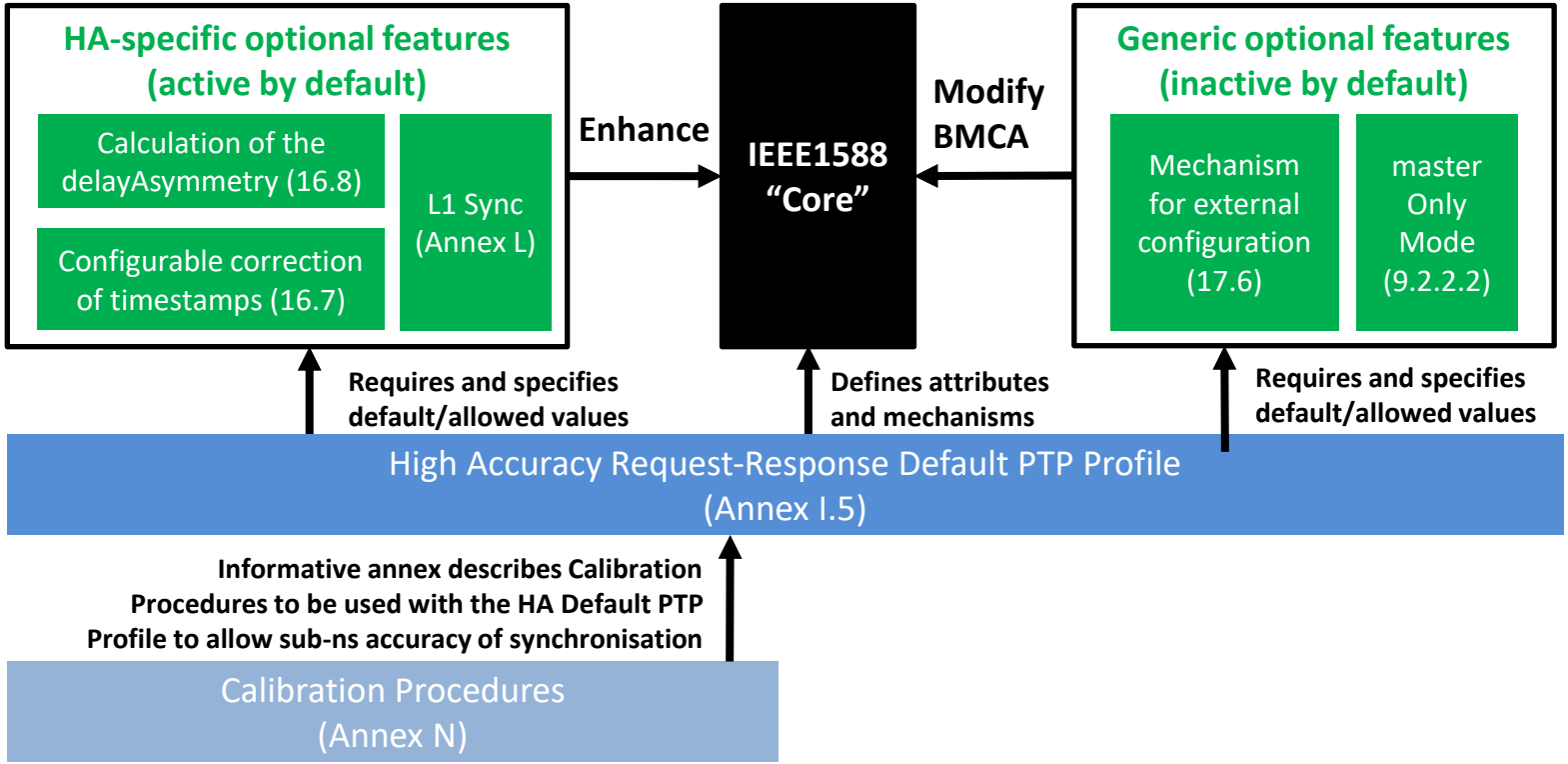

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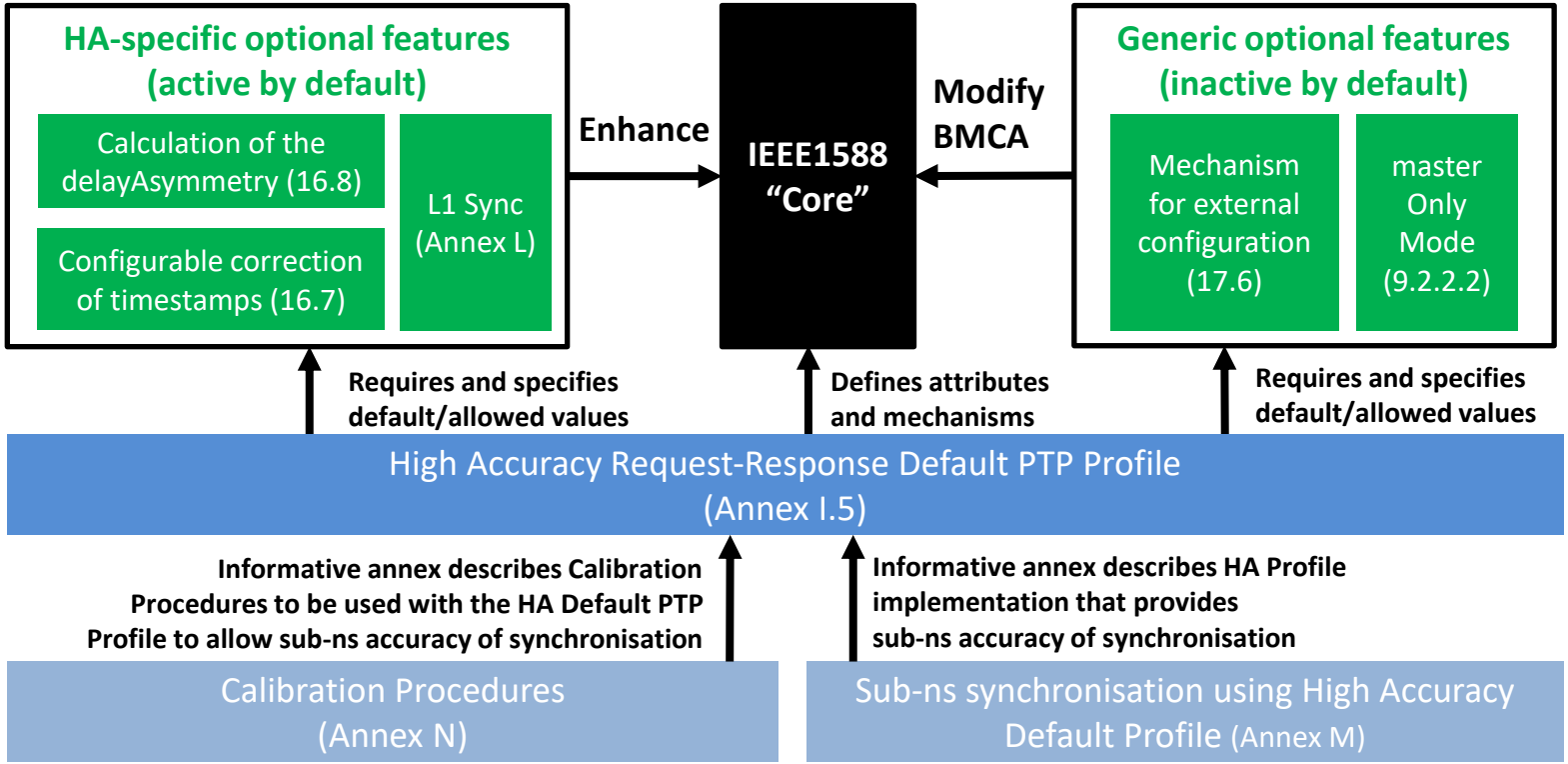

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- **WR-PTP and HA Profile are compatible hardware-wise and are not compatible protocol-wise**

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