[18]

[23]

GEFÖRDERT VOM

6G-ICAS4Mobility

Light Rabbit

Implementing a White Rabbit node on COTS AMD development boards without relying on external VCXOs

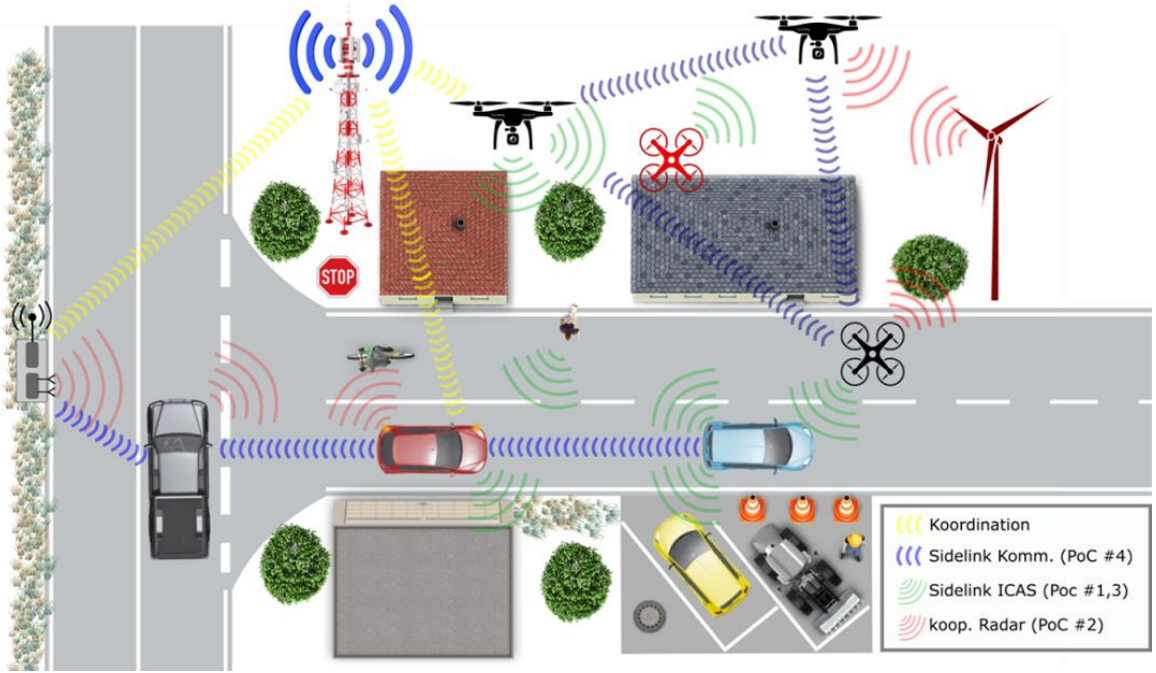
Frederik Pfautsch, Ulrich Langenbach

6G-ICAS4Mobility: Scenario

[23]

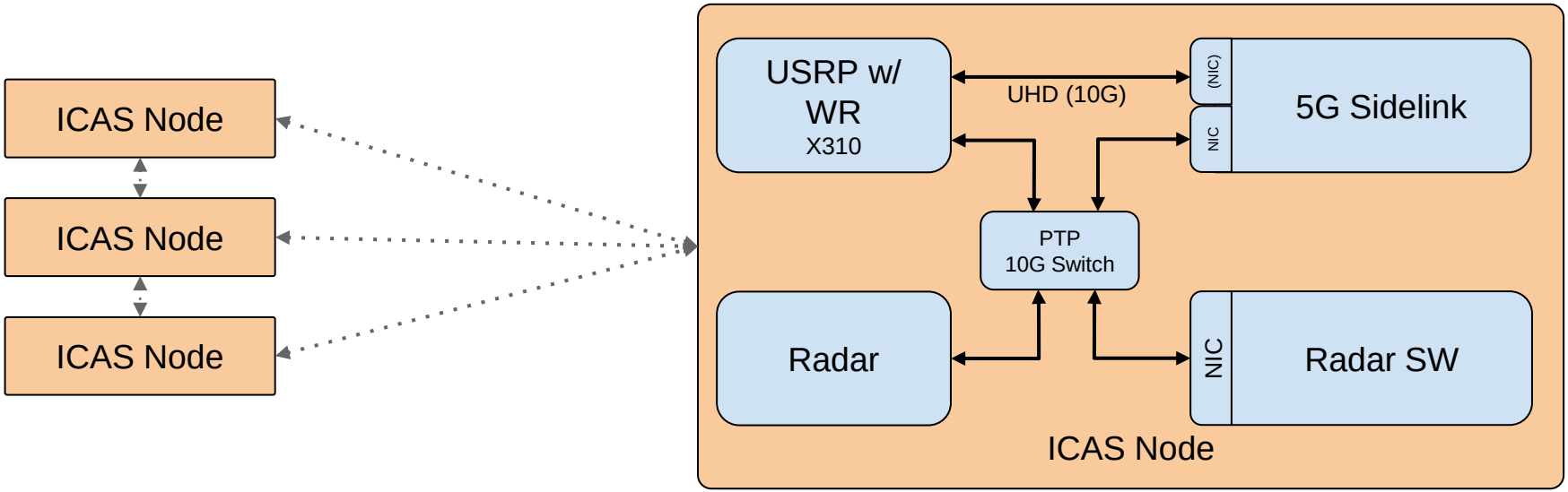
6G-ICAS4Mobility

Integrated Communication and Sensing in 6G for stationary and mobile nodes



[24]

6G-ICAS4Mobility: An example node structure



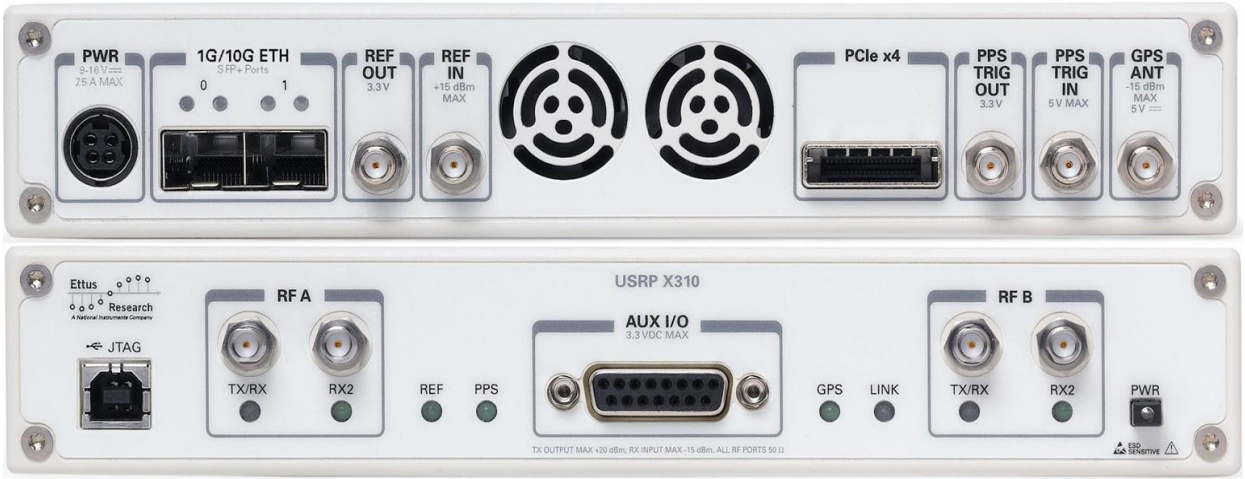
White Rabbit … on an Ettus X310 USRP

- AMD Kintex-7 XC7K410T FPGA
- PCIe
- 2x SFP+ (10G or 1G)
- Optional GPSDO
- DA-15 GPIO port
- 2x RF Front-End Daughter Board slots

⇒ **No VCXOs!**

⇒ **No QPLLs with FRAC-N support!**

⇒ **7Series fabric ⇒ use MMCMs!**



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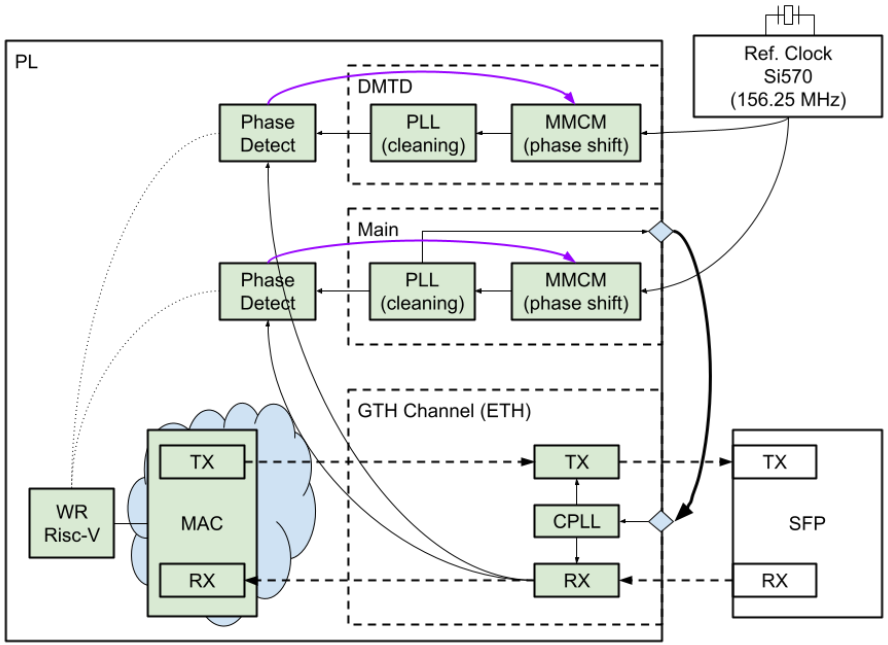
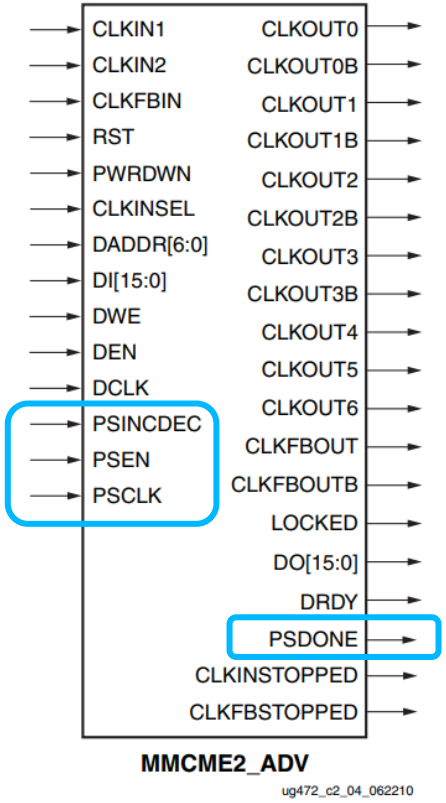
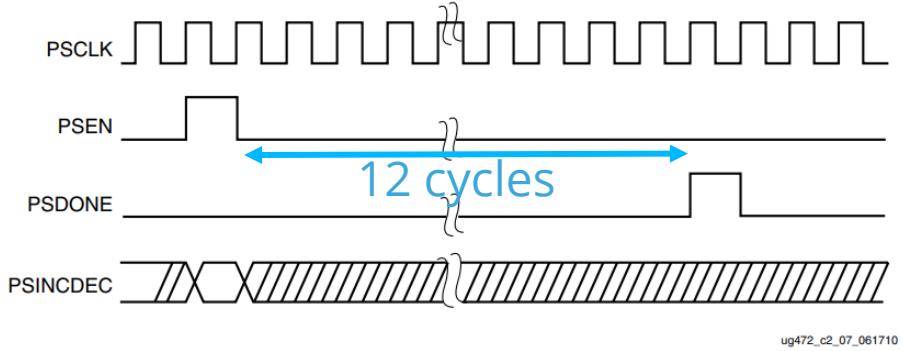
MMCM-based Implementation

- Clock oscillator can have any reasonable frequency
- Frequency is adjusted by repeated phase shifts
- PLL for cleaning chained behind phase-shifting MMCM



MMCM: Dynamic Phase Shift Interface





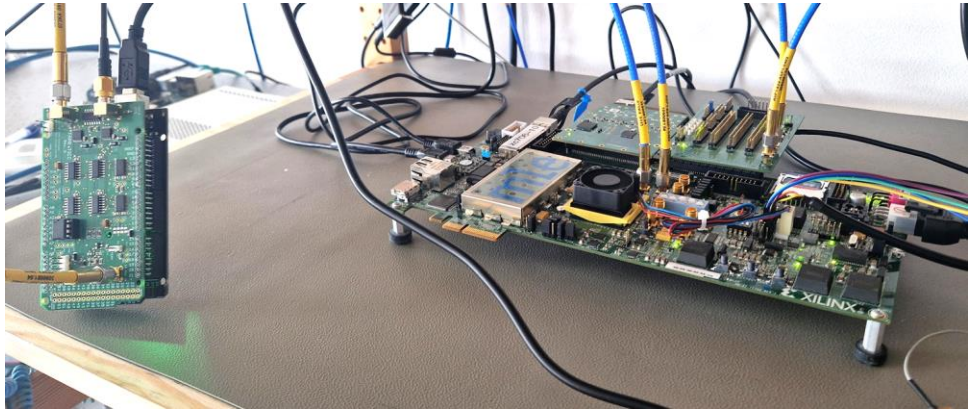
- Add up (unsigned part of) 16 Bit DAC value every 12 cycles
- Sign bit → PSINCDEC
- On wraparound → PSEN = ‘1’

- Shift by 1/56 th of a VCO period

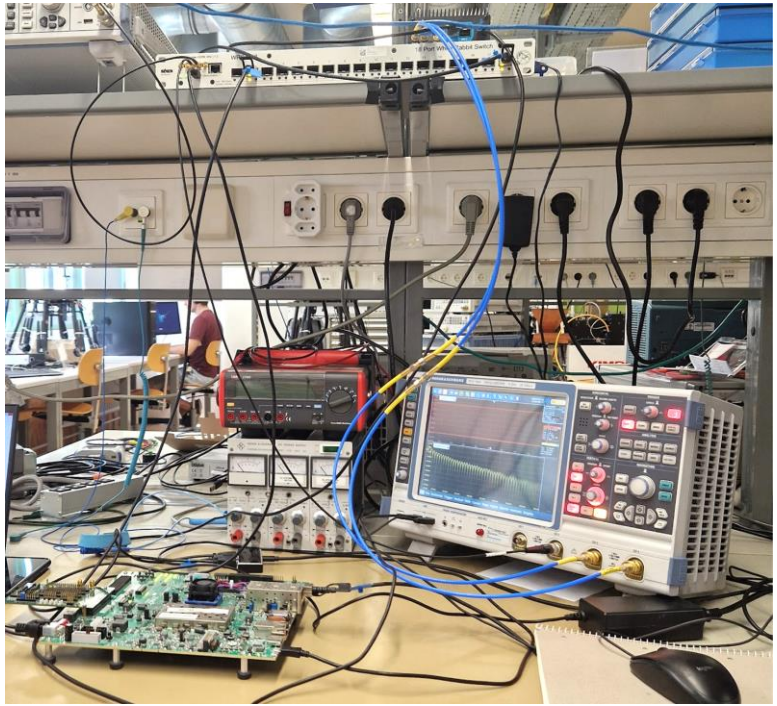
https://docs.amd.com/v/u/en-US/ug472_7Series_Clocking

Measurement Setups

TAPR-TICC (PPS), D-DMTD on ZC706 (10 MHz)

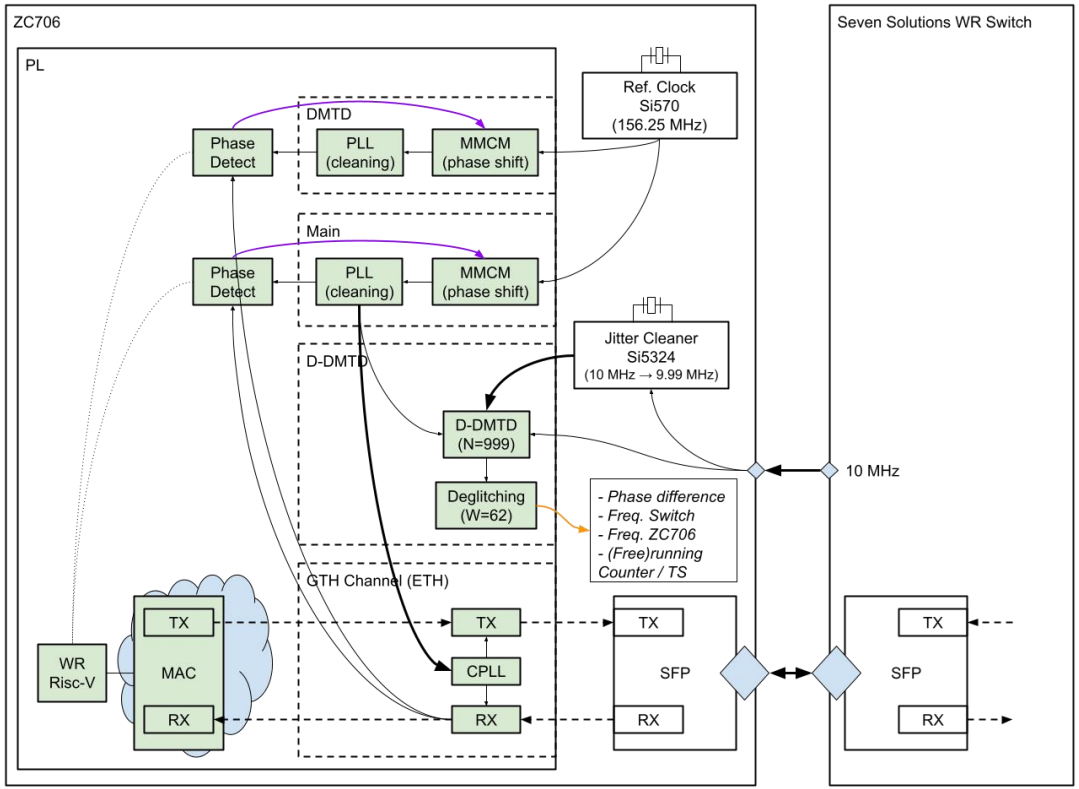


R&S RTO1044

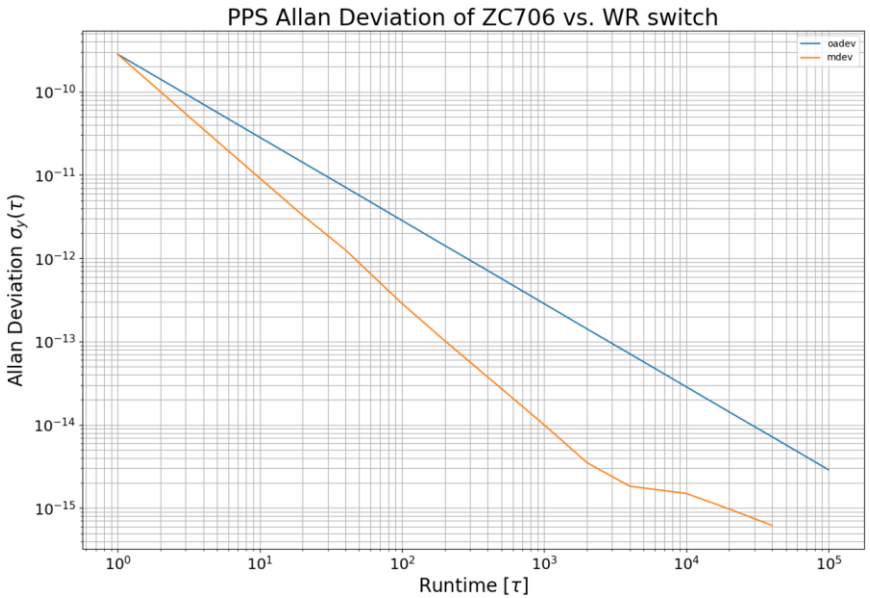


D-DMTD based Measurement Setup: 10MHz

- Employ D-DMTD again
  N = 999
  W = 62
  ⇒ 10ps resolution
- Compare to *Seven Solutions* WR switch
- Gather phase and frequency information

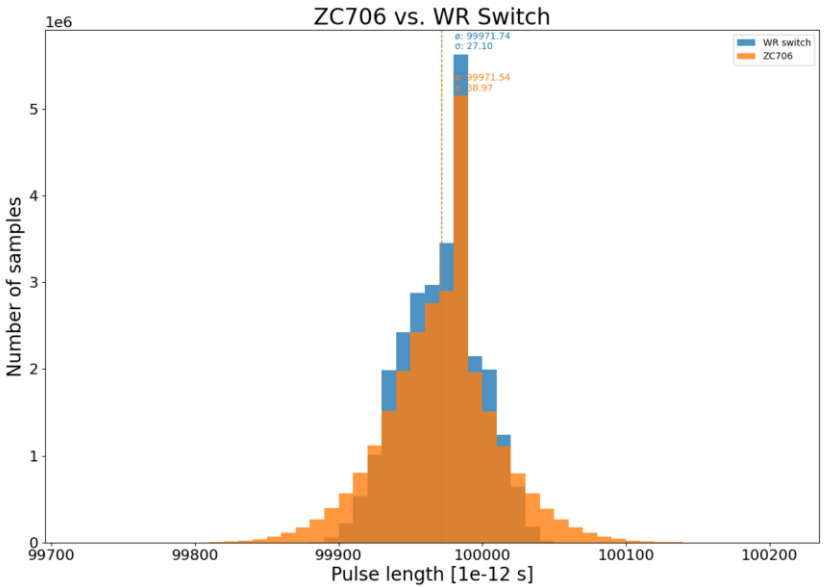


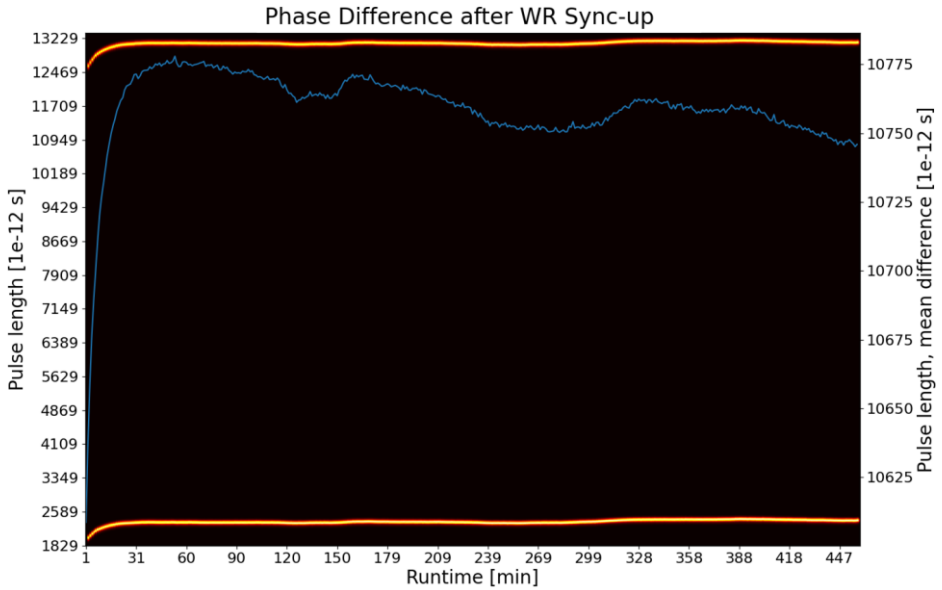
Allan Deviation: MMCM-based



TAPR-TICC based Measurement Setup

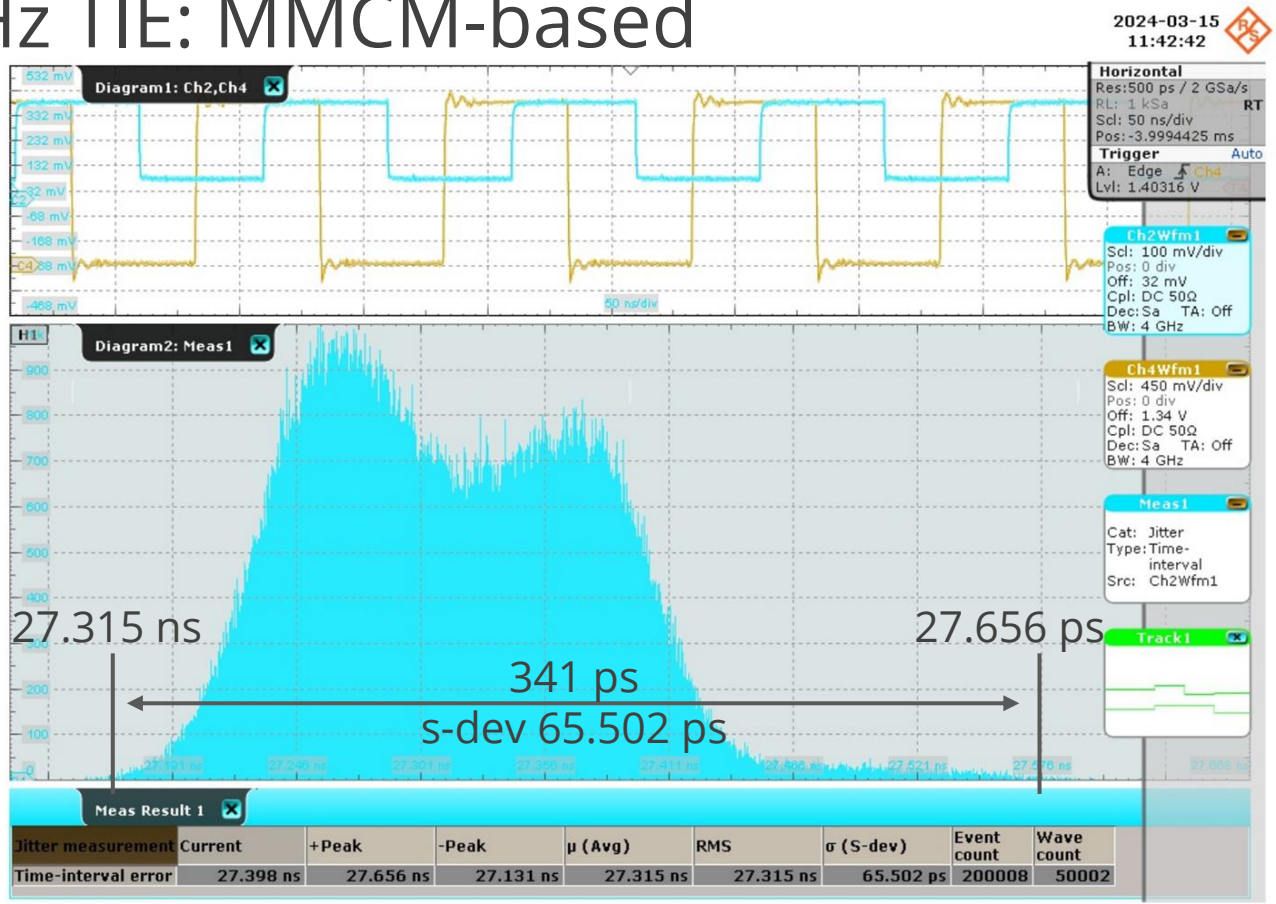
Histogram: MMCM-based





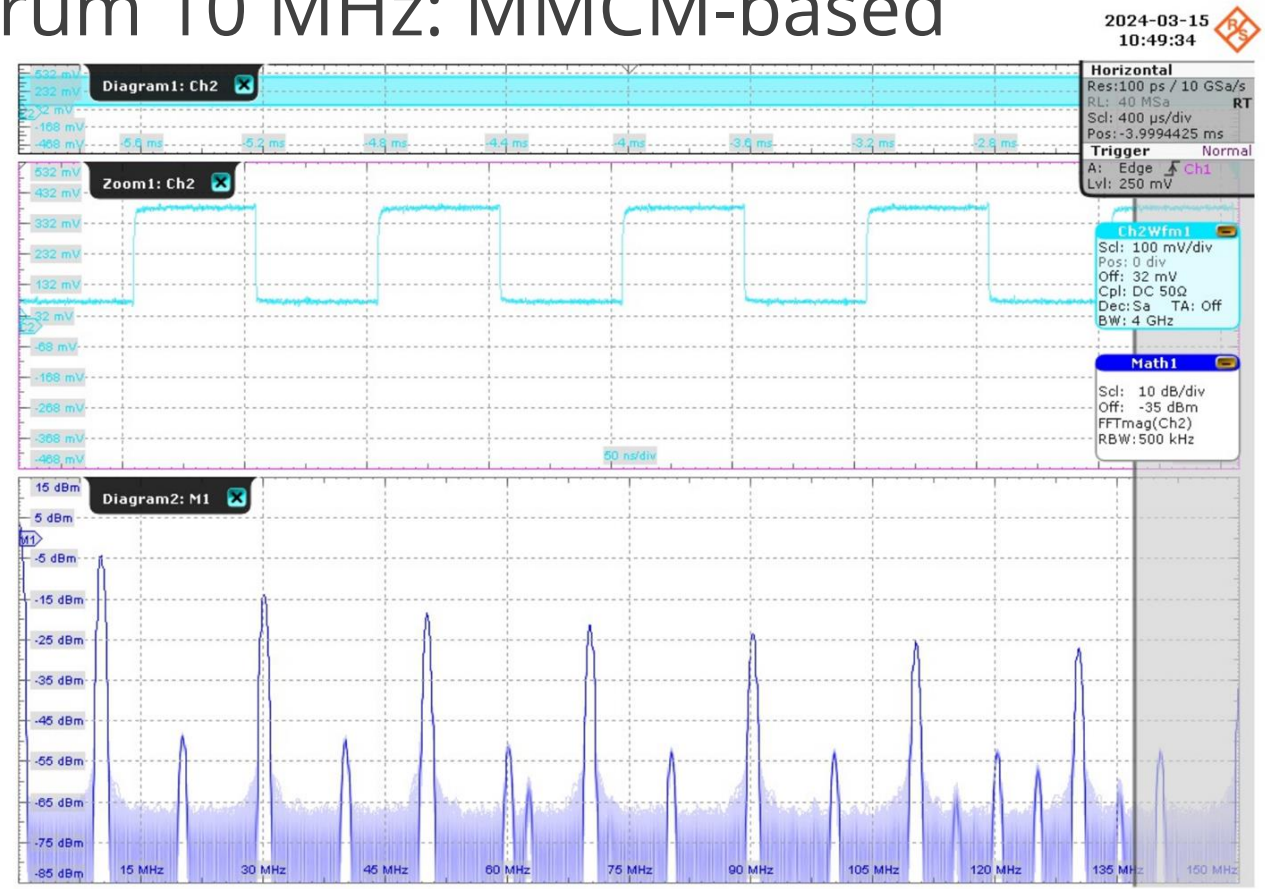
D-DMTD based Measurement Setup

10MHz TIE: MMCM-based



R&S Jitter Wizard
R&S RTO1044

Spectrum 10 MHz: MMCM-based



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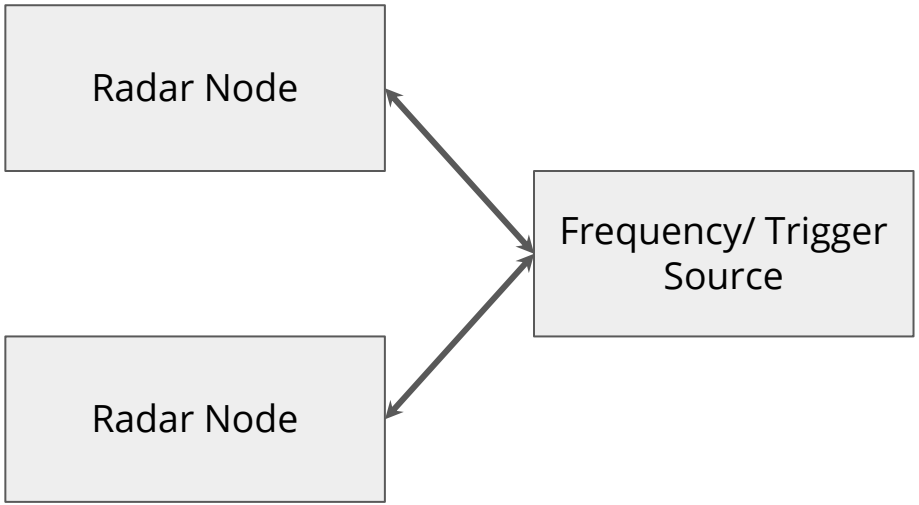
VERANO: In-vehicle Radar Networks

[18]



Radar Network Demonstrators

- AI based Radar Image Processing
- Radar Image Compression
- OFDM Radar, etc.
- Radar Imaging
- Front-end research

Frequency/ Trigger Distribution via

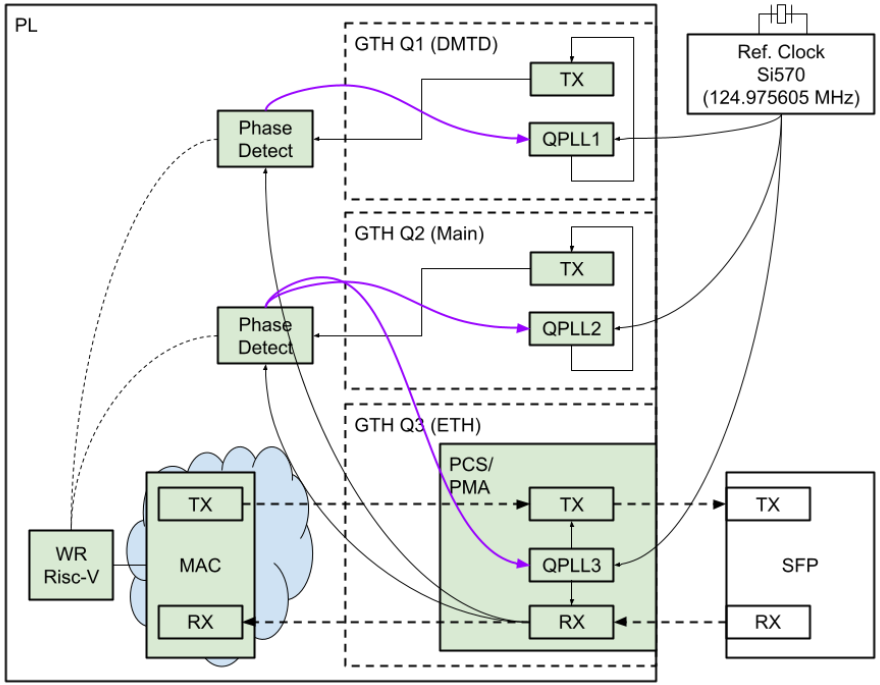
- Coax cable
- Ethernet with PTP v2.1
- Wireless LO distribution

VCXO Technologies (Dormouse FMC Card)

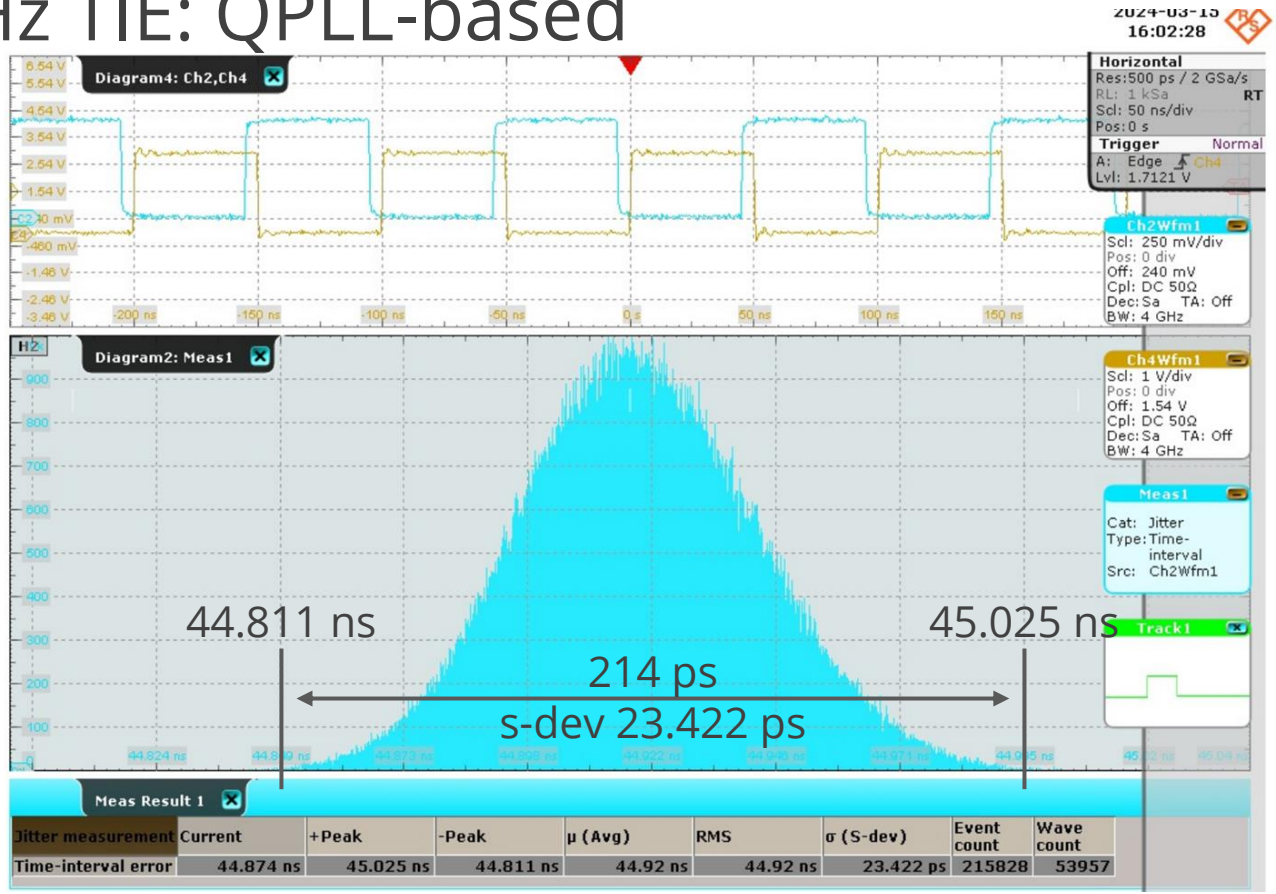
- AMD ZUP/RFSoC GTHe4/GTYe4 QPLL
- SiT3521

QPLL-based Implementation

- Multiple GTH Quads
- External fixed GTH reference clock slightly below 125 MHz
- QPLL output clock needs to pass through a channel TX to be available in fabric
- Frequency is adjusted using the QPLL “SDM” feature

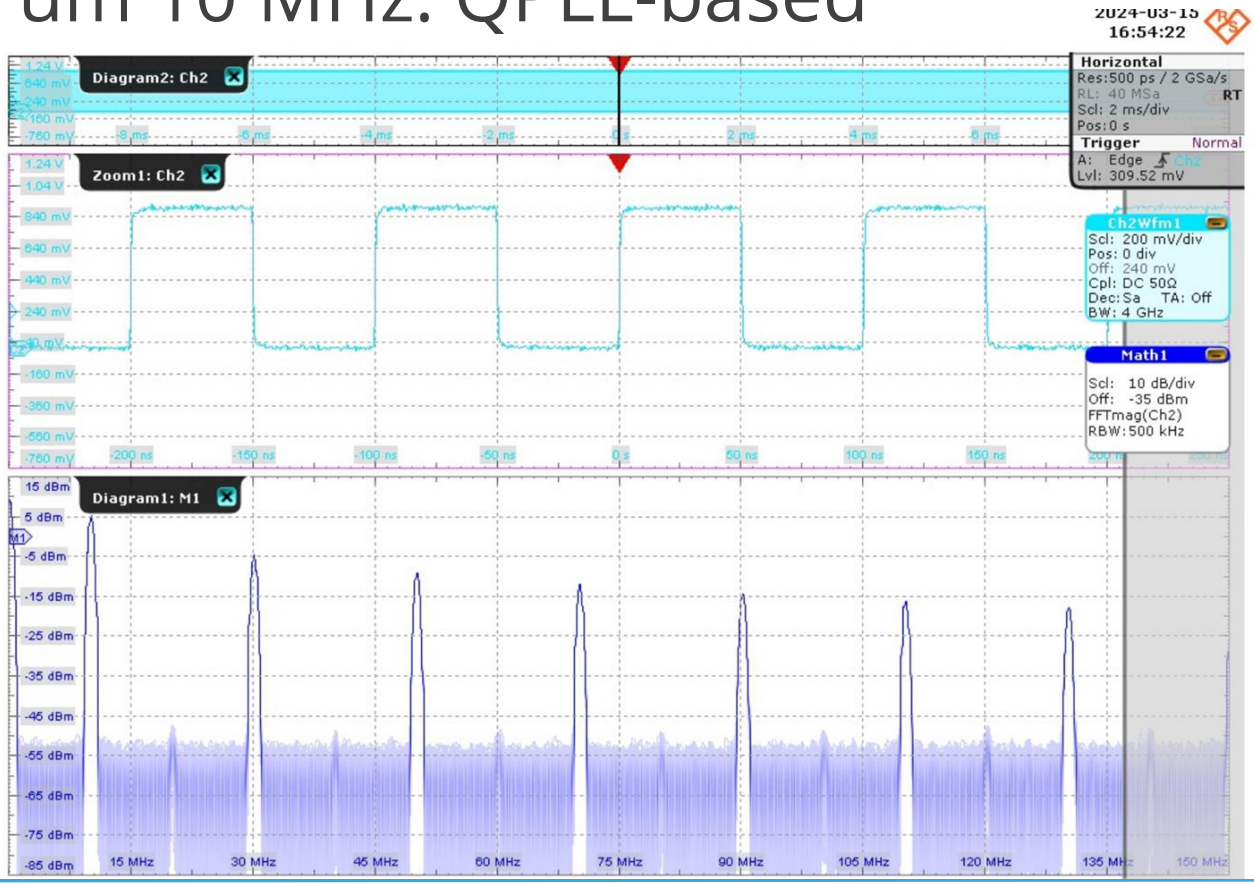


10MHz TIE: QPLL-based



R&S Jitter Wizard
R&S RTO1044

Spectrum 10 MHz: QPLL-based



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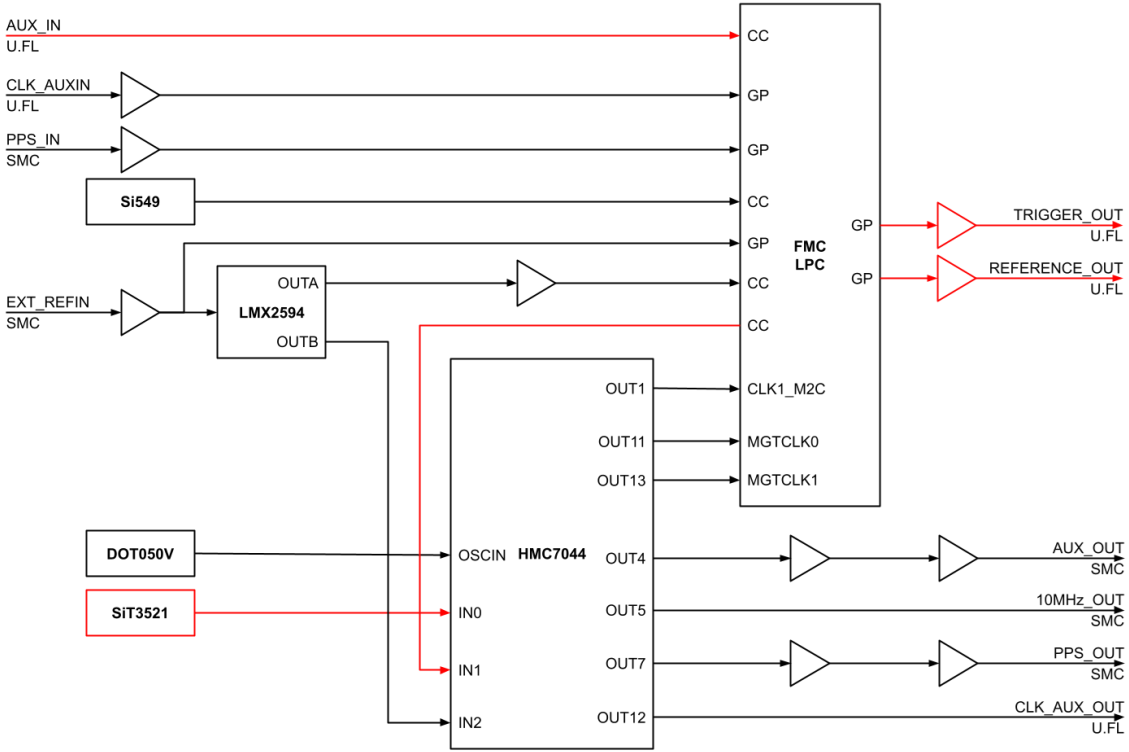
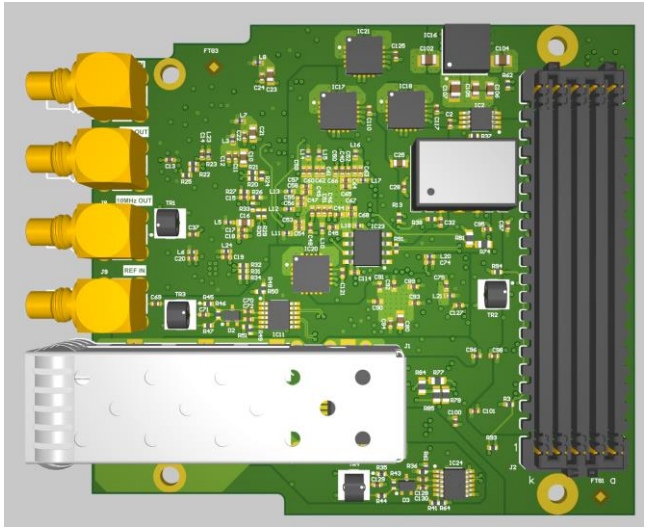
Dormouse: an FMC Card based on the FCWR Card





Conclusion

- Loss of accuracy compared to “conventional” VCXOs
- QPLL (Ultrascale fabric) has higher precision and accuracy (than MMCM)
- MMCMs are more widely available, requires less resources

⇒ **What’s next? Work-in-progress…**

- Absolute Calibration with the special SFP Loopback Module
- Measure FPGA-internal (bitstream) delays and jitter effects
- Investigate effects of phase-shifting MMCM
- Investigate reset and power-on randomness

Thank You!

- DESY for providing loaner of a White Rabbit Switch
- U Ulm for supporting the measurements, e.g. with their R&S RTO, etc.
- BMBF for funding the 6G-ICAS4Mobilitx and VERANO projects

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und Forschung

universität
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Institut für Mikrowellentechnik
Universität Ulm

Backup

References (1) (automatic numbering: don't delete or insert entries => append!)

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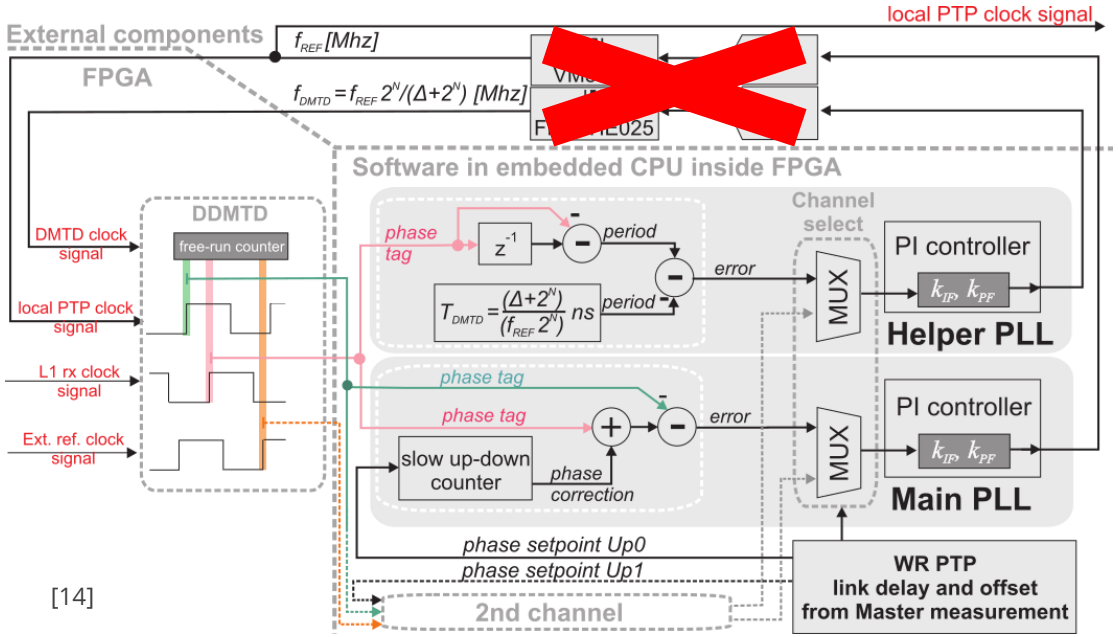
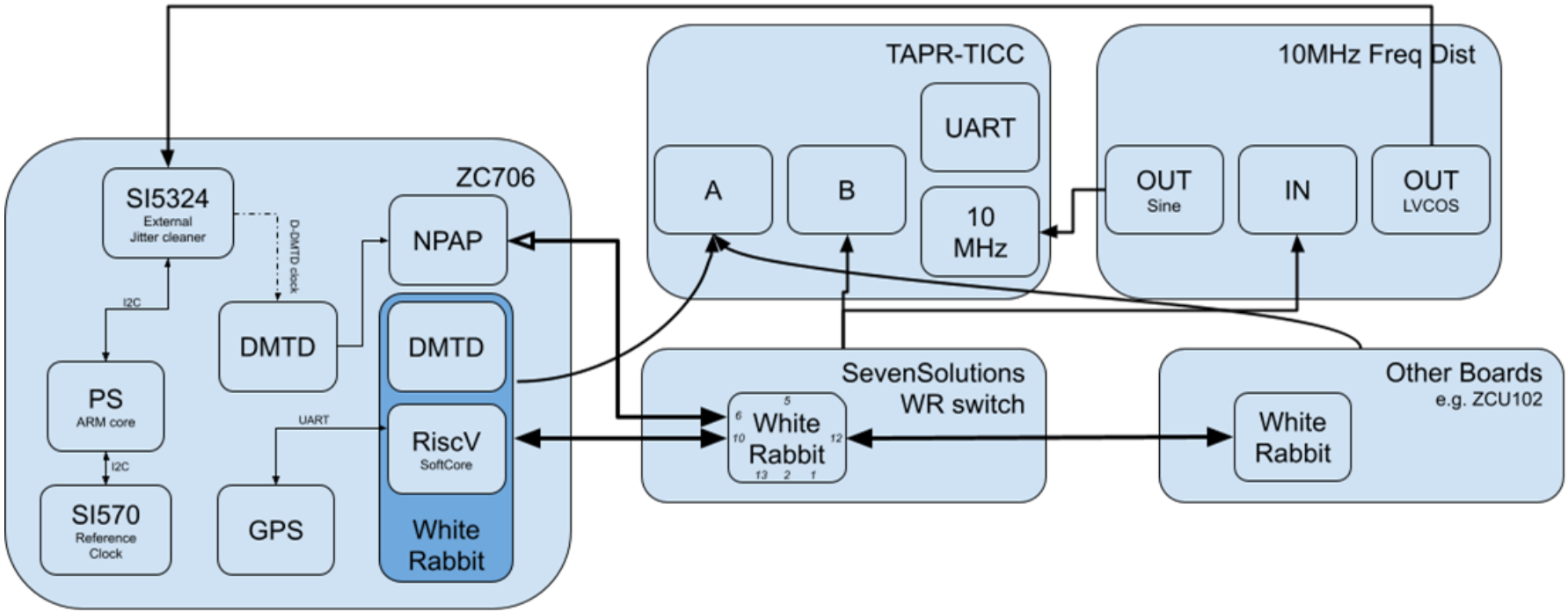
Light Rabbit

- Lower barrier to entry
- Reduces board complexity
- Enables ‘legacy’ HW w/o VCXOs

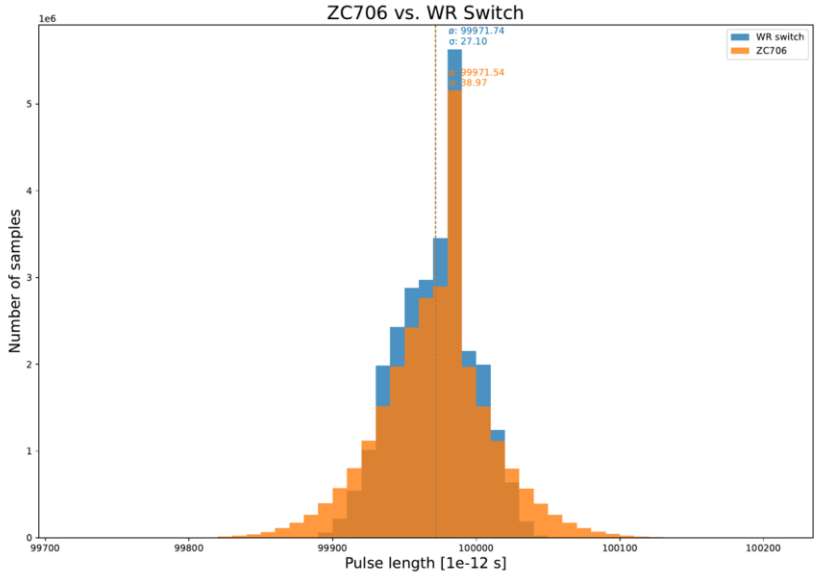


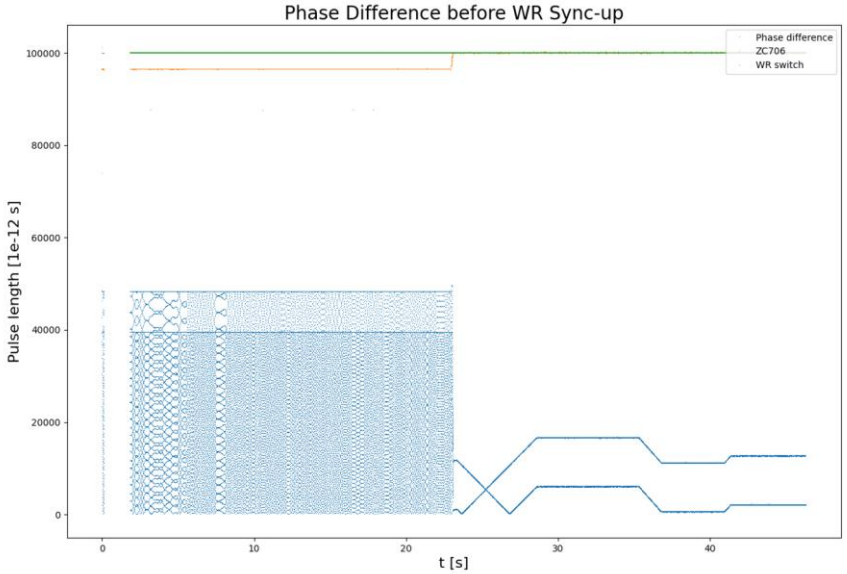
[14]

TAPR-TICC based Measurement Setup: PPS



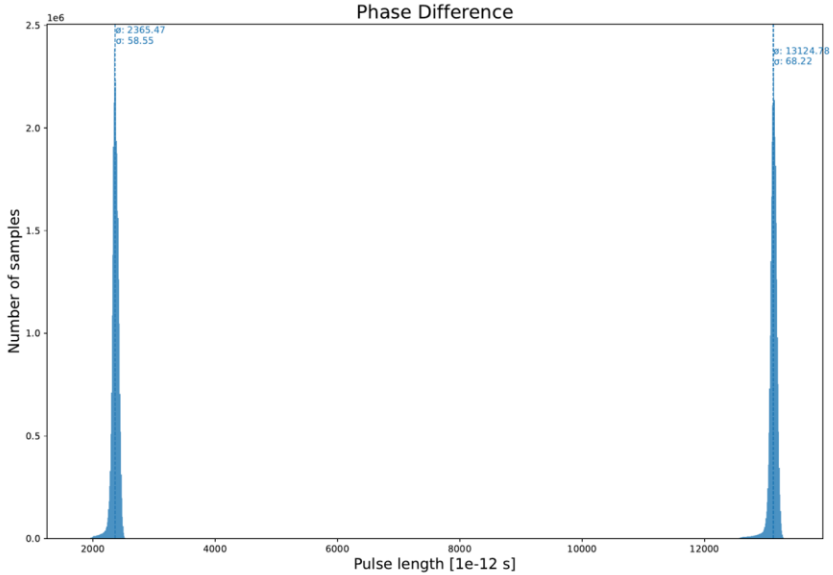
Histogram: MMCM-based

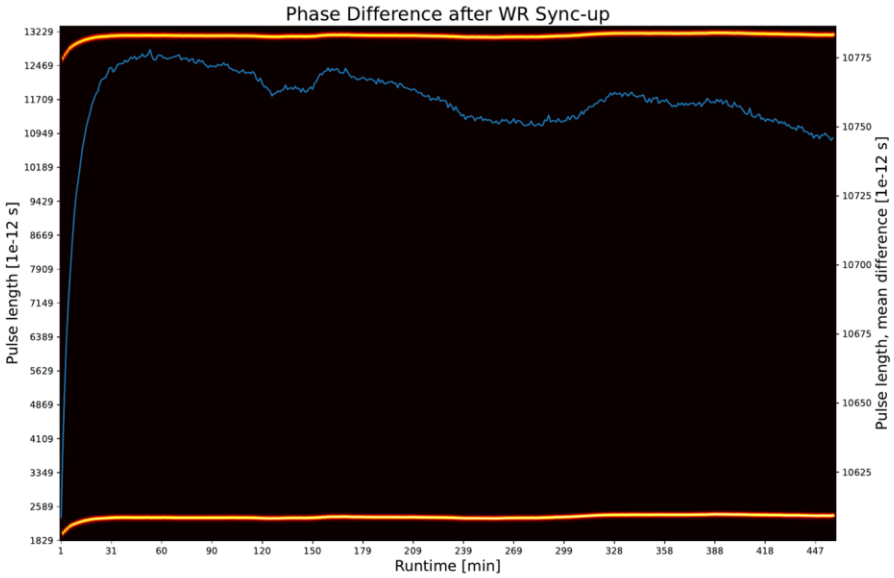




D-DMTD based Measurement Setup

Histogram: MMCM-based

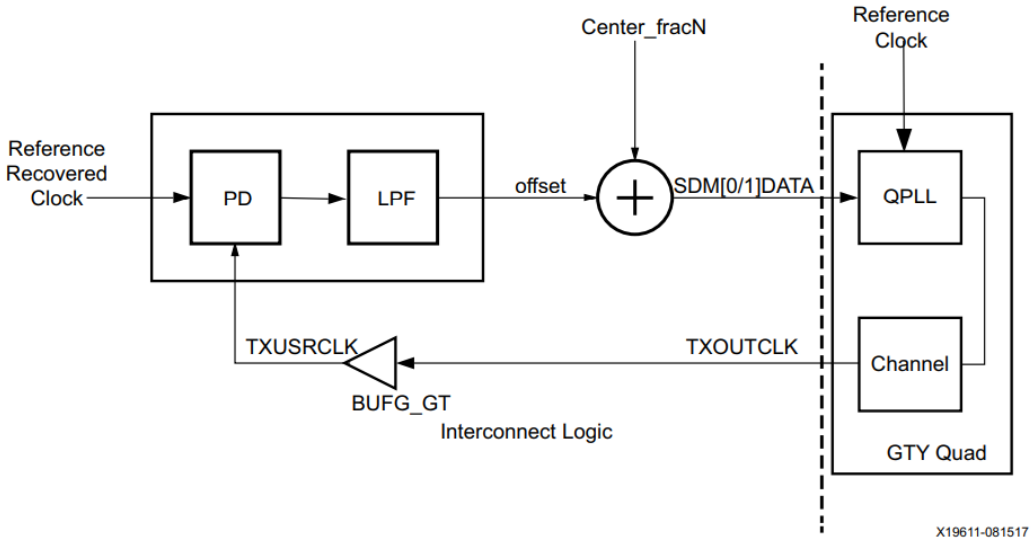




D-DMTD based Measurement Setup

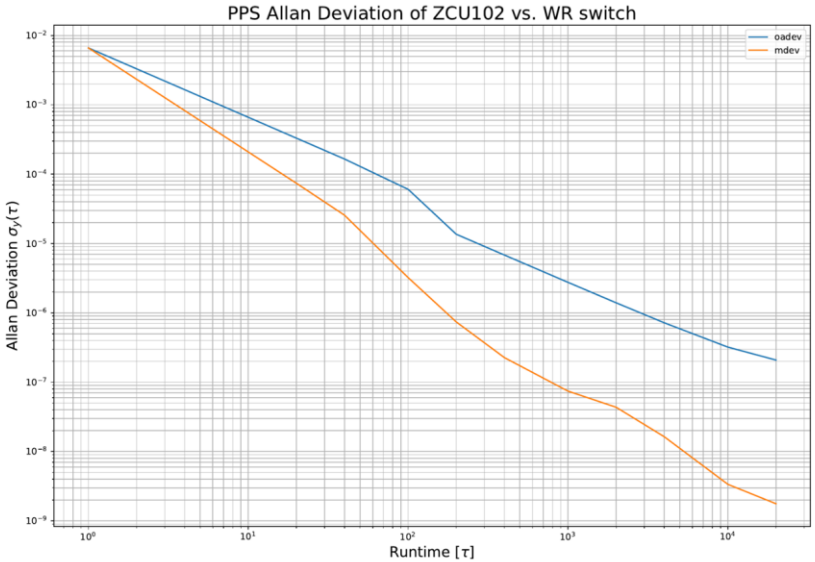
QPLL: Sigma-Delta Dynamic Frac-N Interface

- Sigma-Delta toggle between N and N+1
- 200 ppm dynamic tuning range
- 16 Bit DAC is mapped to 18 Bit SDM[0/1]DATA value

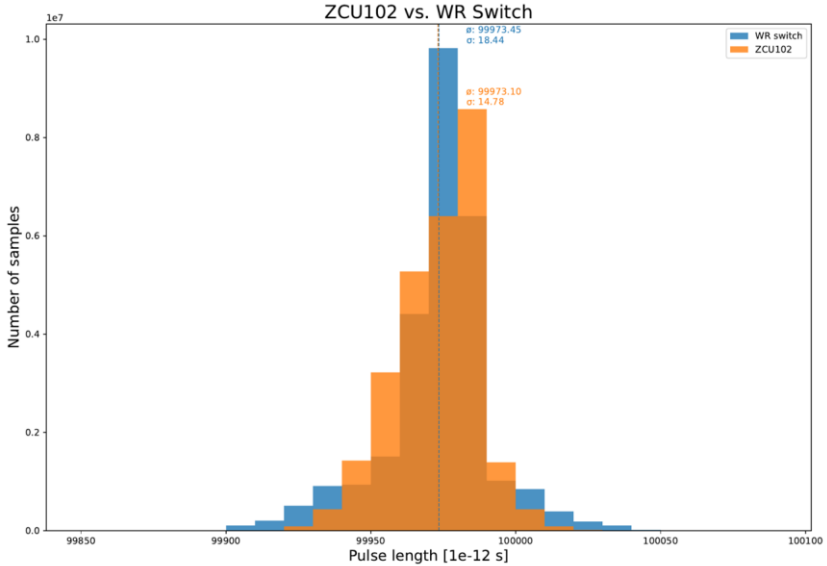


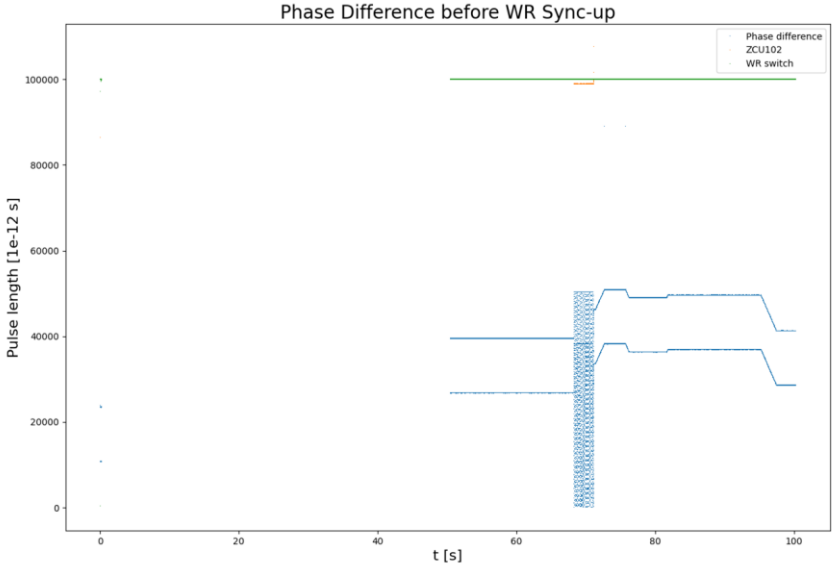
https://docs.amd.com/v/u/en-US/ug578-ultrascale-gty-transceivers

Allan Deviation: QPLL-based

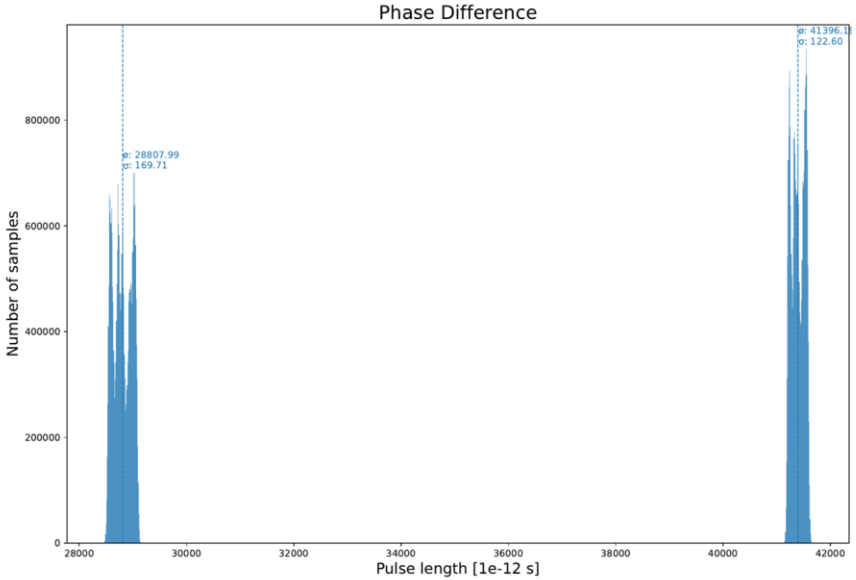


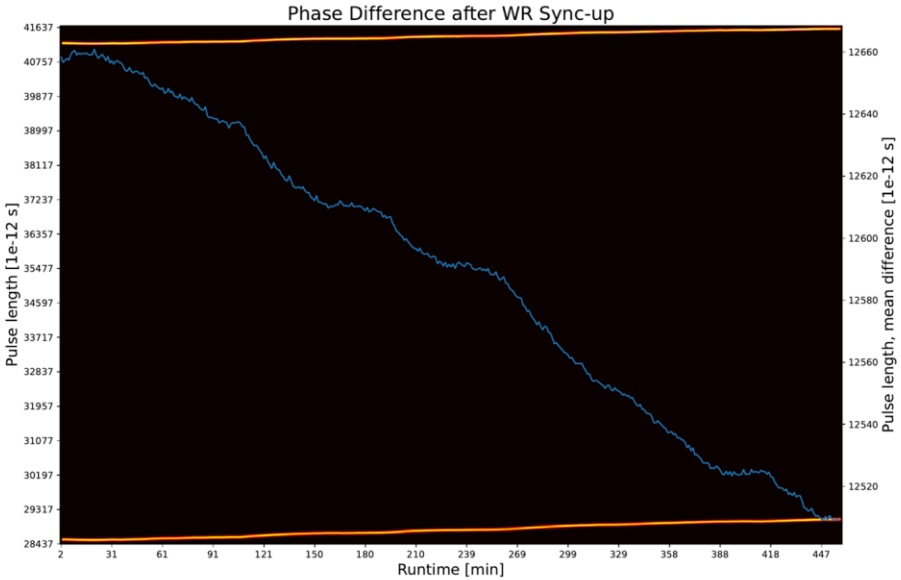
Histogram: QPLL-based



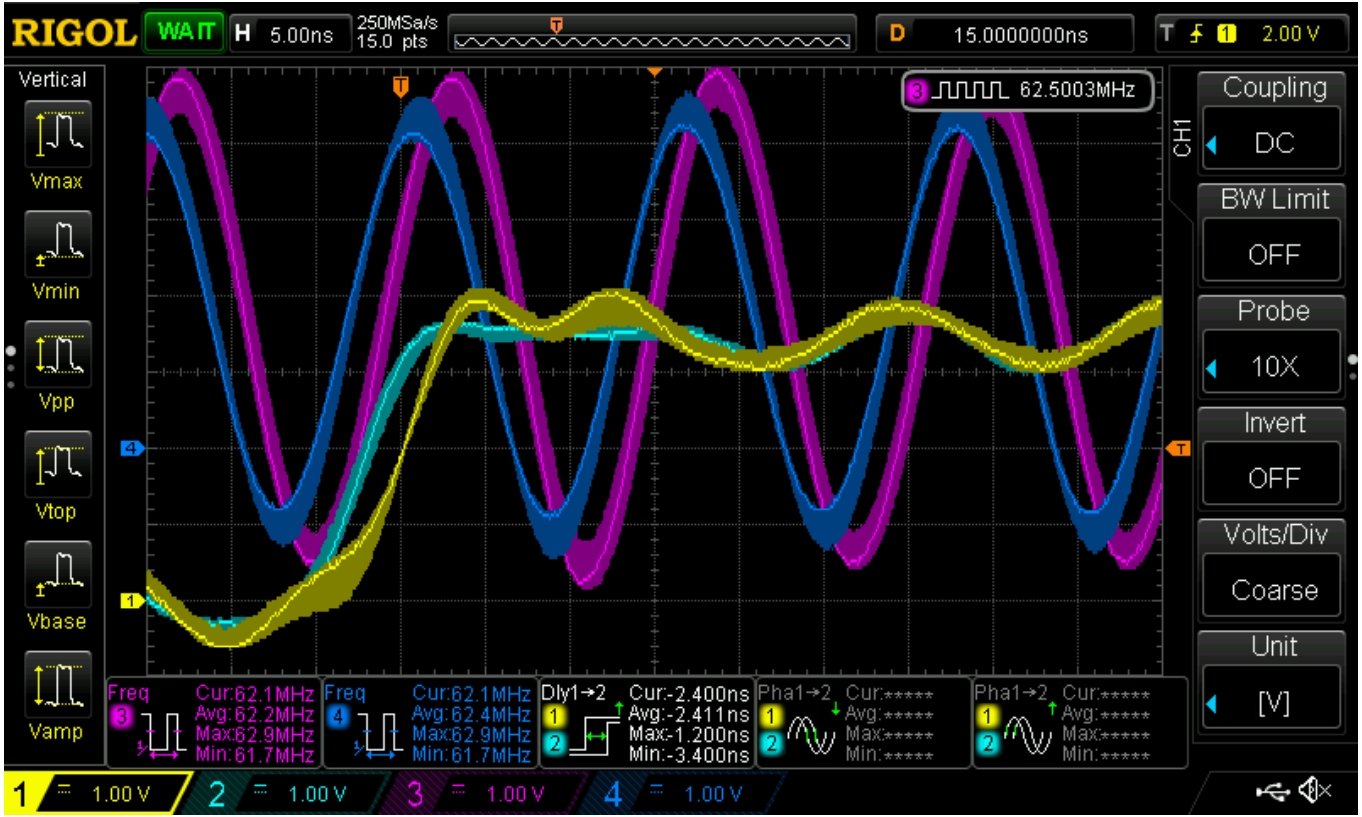


Histogram: QPLL-based



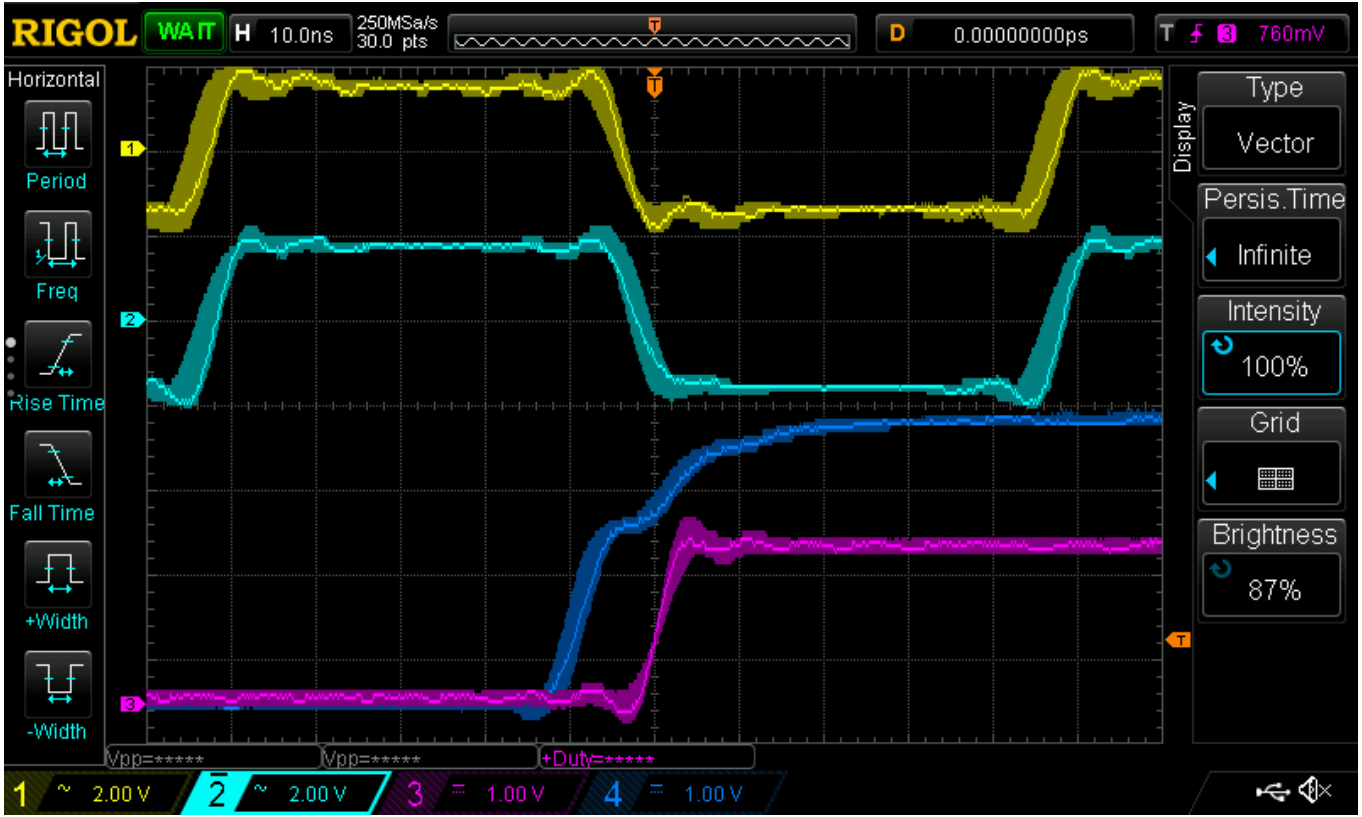


Dual ZCU102 MLE WR Nodes Directly Connected



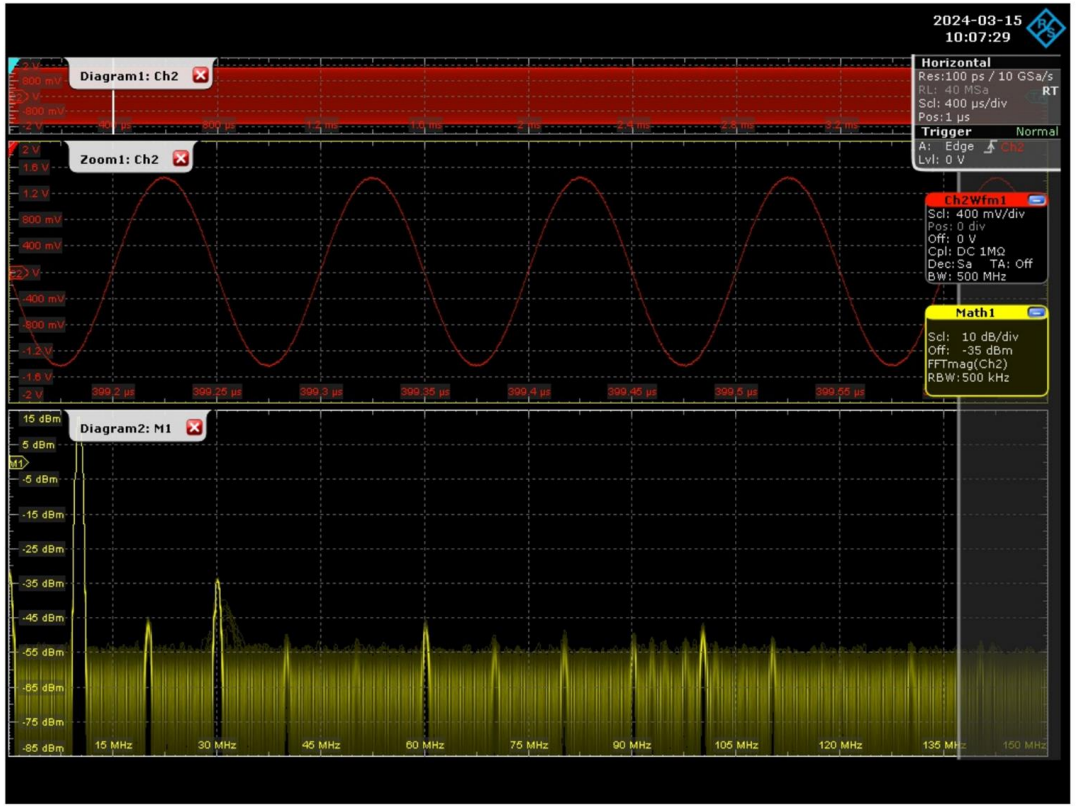
Rigol DS1074z

X310 WR Node Connected to WR Switch



Rigol DS1074z

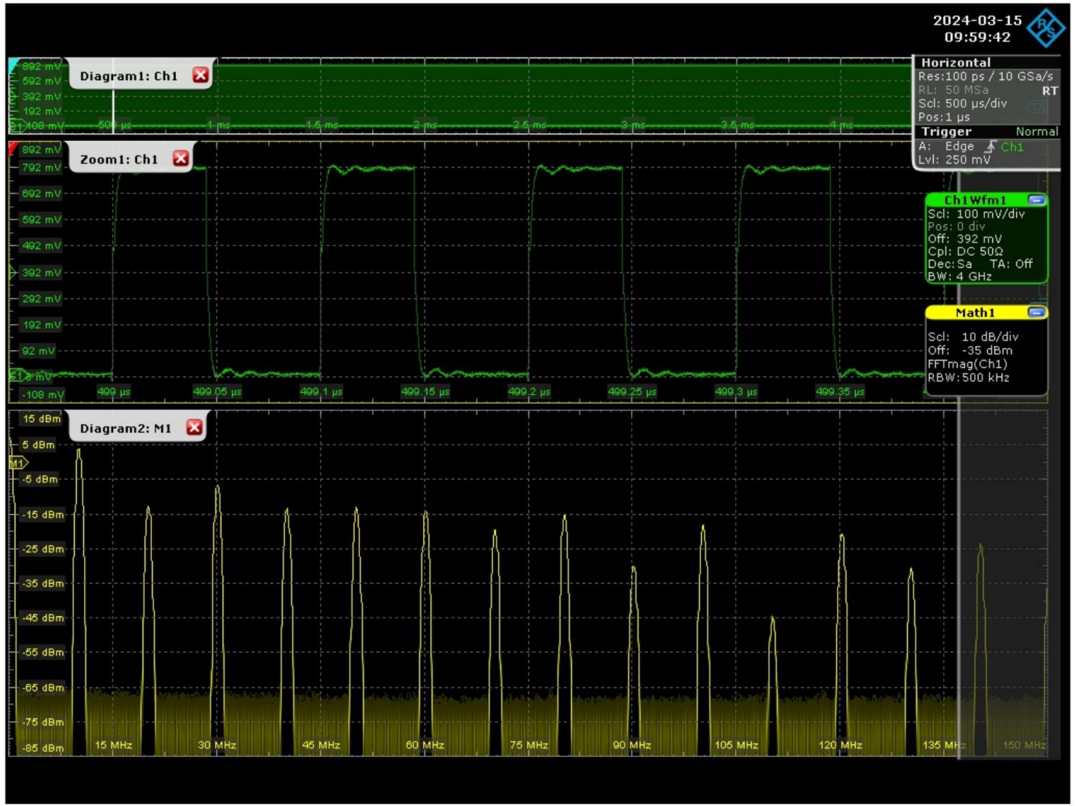
10 MHz Distribution (sine)



[26]

R&S FFT
R&S RTO1044

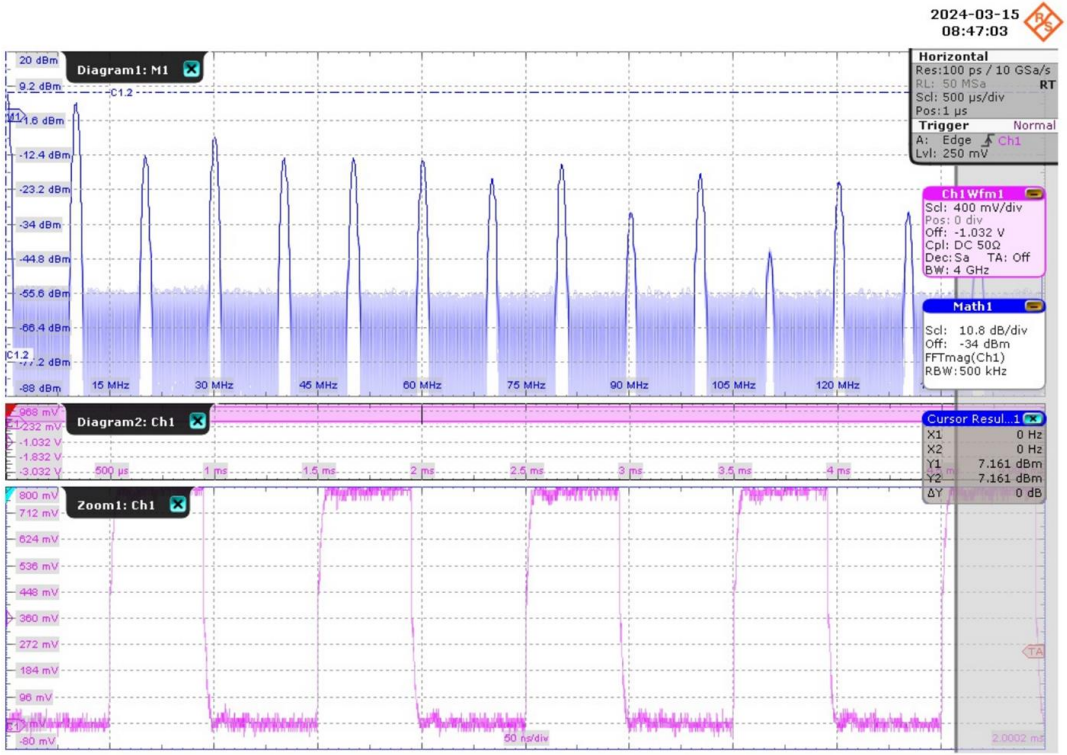
10 MHz Distribution (LVCMOS)



[26]

R&S FFT
R&S RTO1044

10 MHz Distribution (LVMCMOS)



R&S FFT
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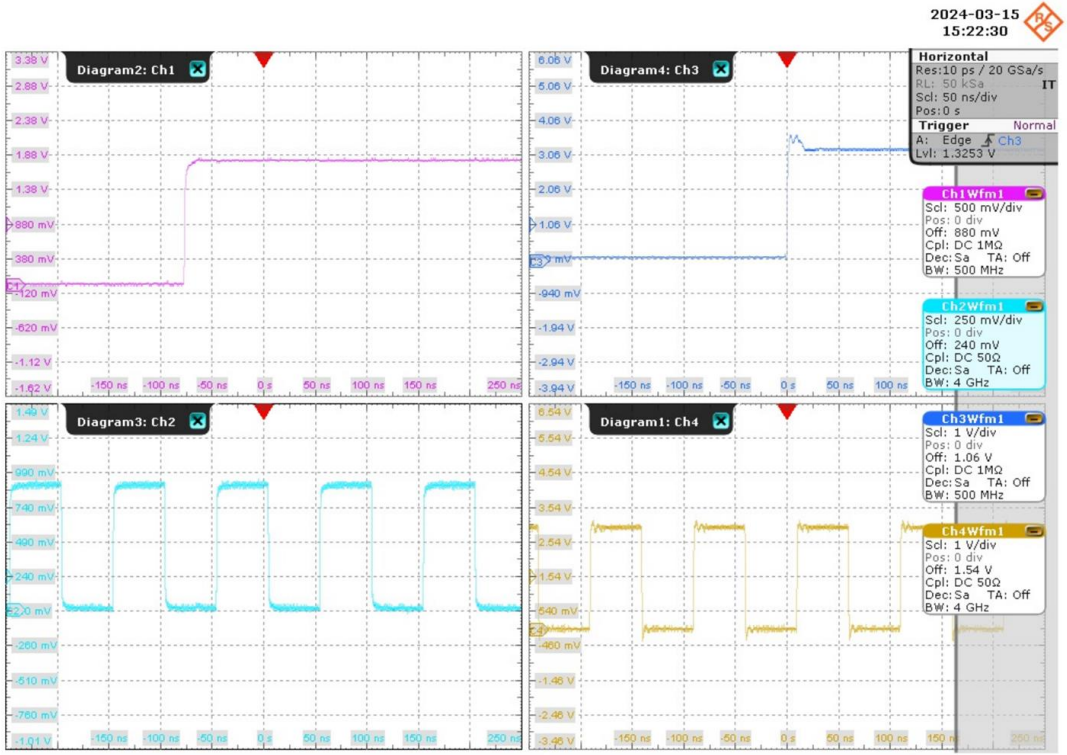
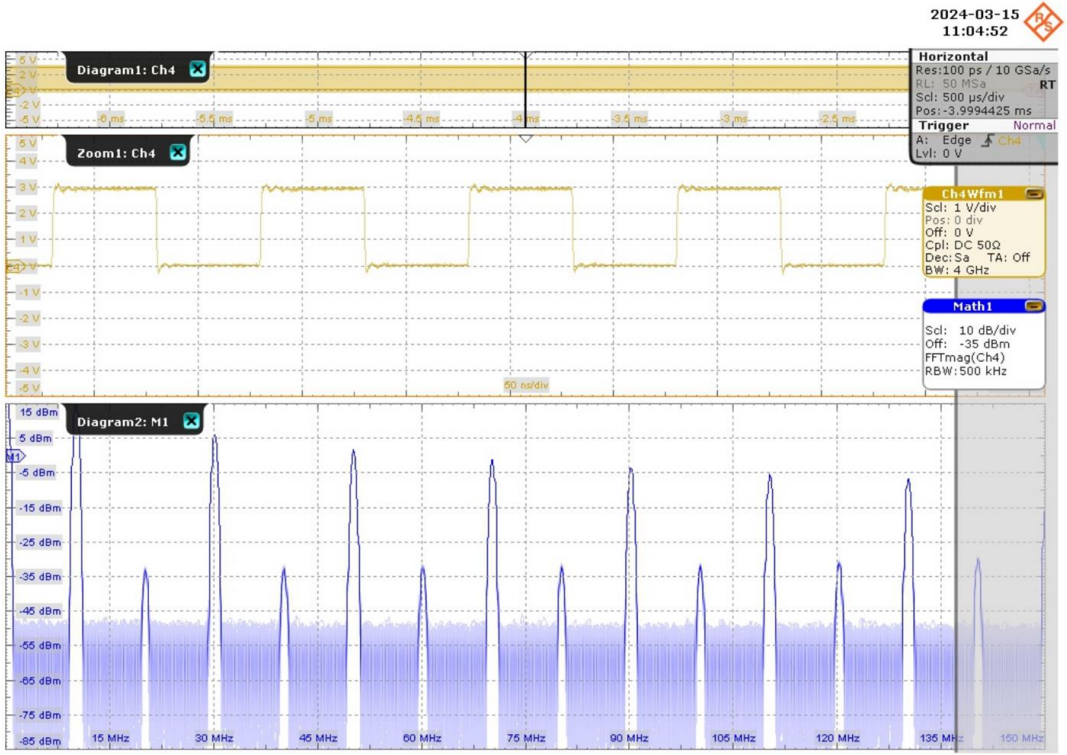
WR Switch vs. ZCU102: PPS and 10 MHz



R&S RTO1044

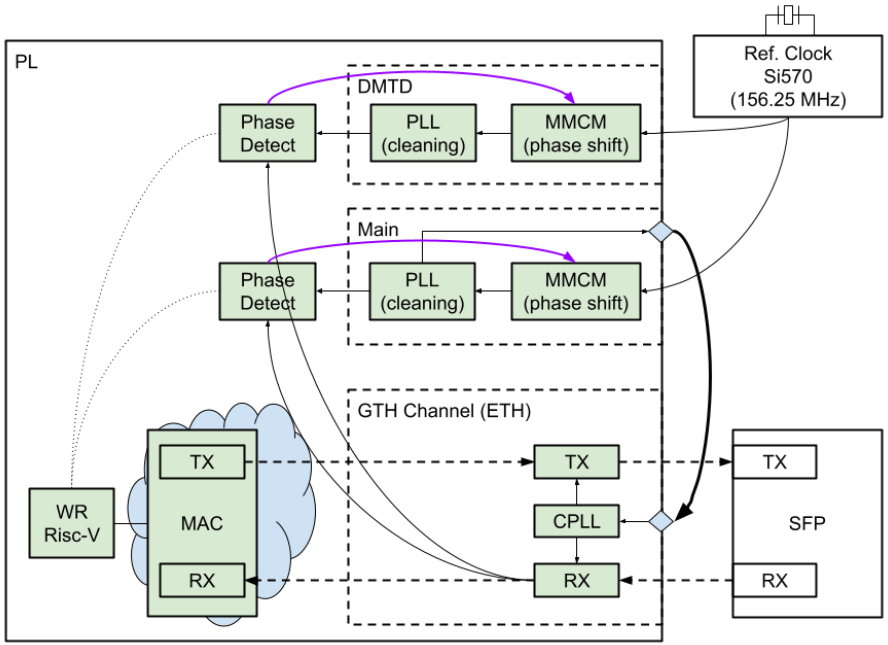
WR Switch 10 MHz



R&S FFT
R&S RTO1044

MMCM-based Implementation

- ZC706 using fabric MMCMs
- Clock oscillator can have any reasonable frequency
- Generated reference clock needs FPGA-external path to GTH reference clock pin (directly or through external PLL pass-through)
- Frequency is adjusted by repeated phase shifts



QPLL-based Implementation

- ZCU102 using GTH QPLLs
- Requires multiple GTH Quads
- Requires external fixed GTH reference clock slightly below (or above) 125 MHz
- Main and ETH QPLL are tuned equally and simultaneously
- QPLL output clock needs to pass through a channel TX to be available in fabric
- Frequency is adjusted using the QPLL “SDM” feature