White Rabbit Applications at CERN

E. Gousiou - CERN Representative to the WRC

WR Workshop #13

All Stars

The WR Team at CERN


Tom


Maciej


Andela


Quentin

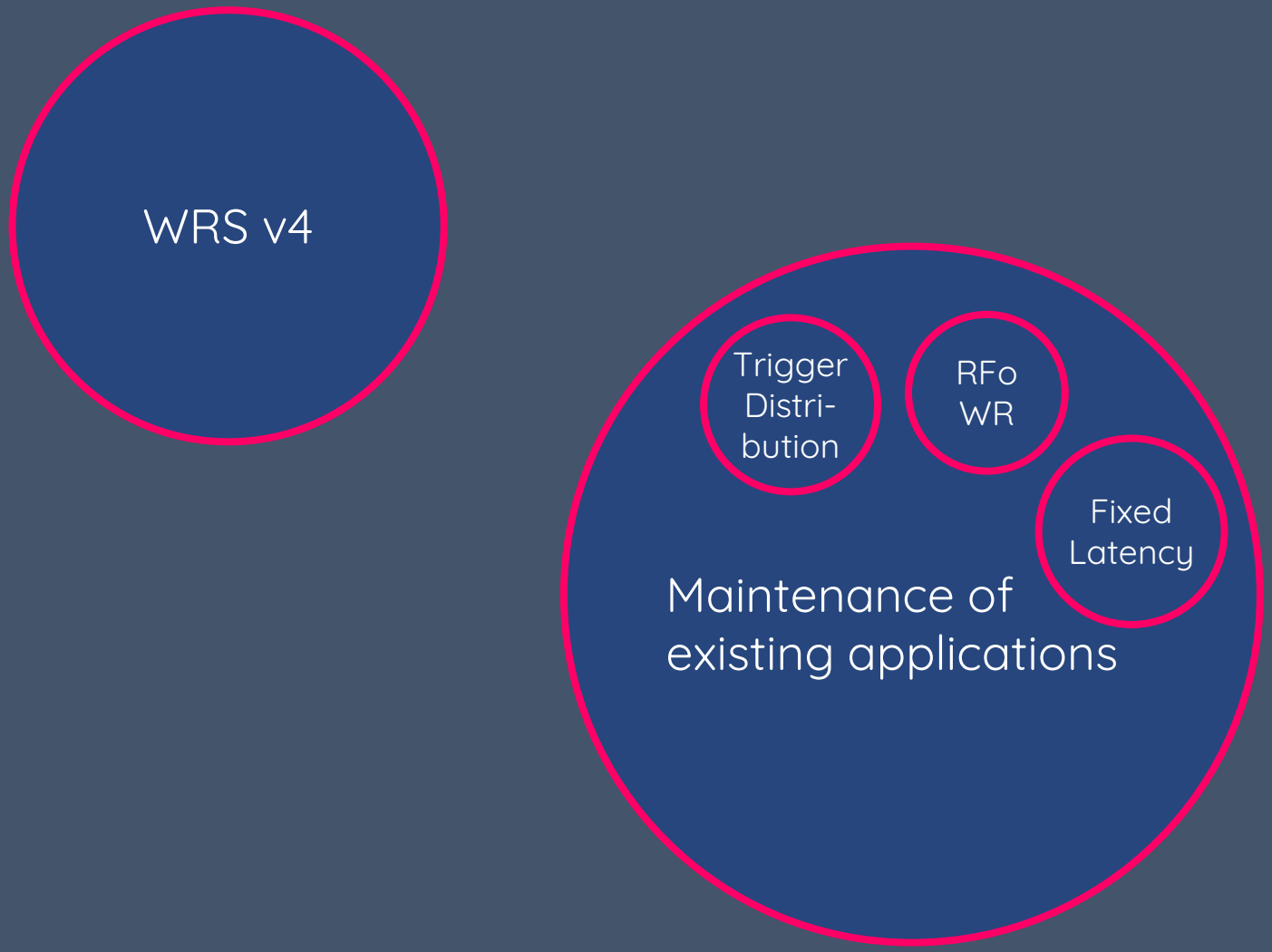

Tristan


Paul


Harvey

The Projects

The Projects



The Projects

WRS v4

Trigger Distri-bution

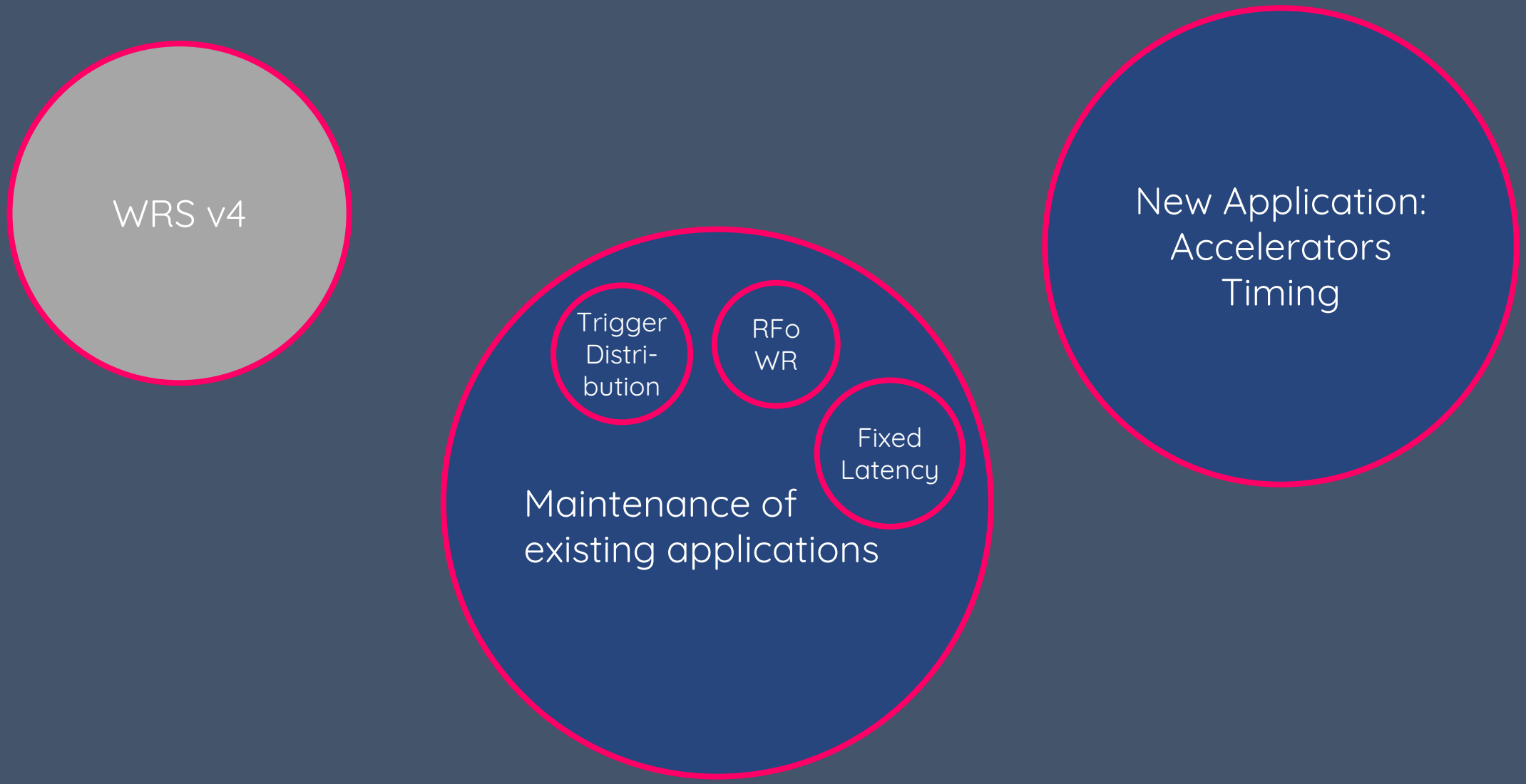
RFo WR

Fixed Latency

Maintenance of existing applications

New Application: Accelerators Timing

The Projects



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WR Application Taxonomy

Fixed Latency Data Transfer	Mitigation of the jitter of the network latency
RF transfer	Capture, transmission and reconstruction of RF signals
Trigger Distribution	Trigger -> Timestamp -> WR UDP frame -> Reproduction with a fixed delay
Time-based Control	General Machine Timing Systems
Precise Timestamping	KM3NET, LHAASO, ..
Time & Freq Transfer	National Time Labs

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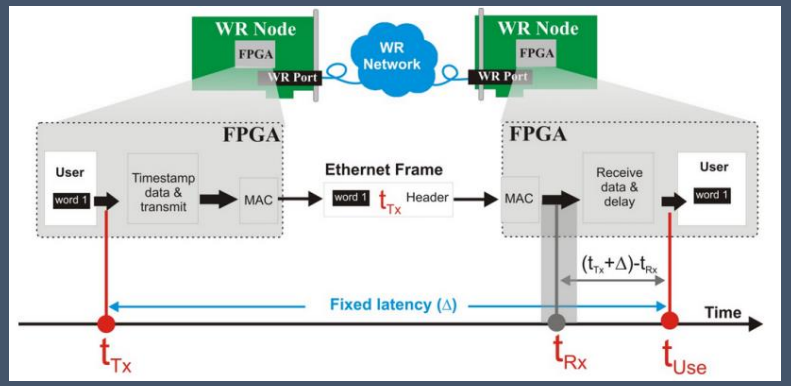
SNAPSHOT OF CURRENT USE

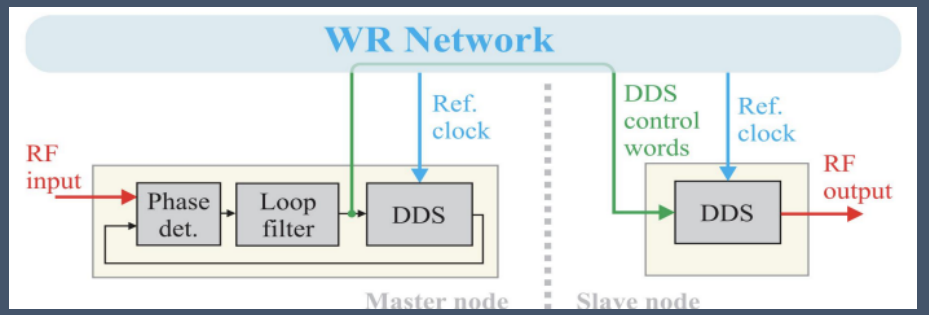
Fixed Latency Data Transfer

10 switches, 25 nodes
Fixed latency distribution of multiple B values



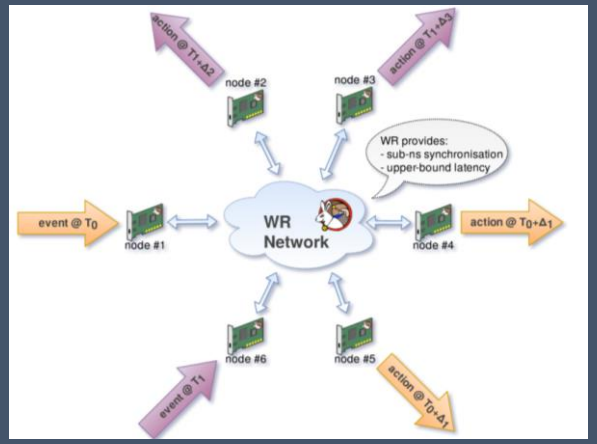
RFoWR

3 switches, 15 nodes
LJ switches and LPDC ports
Accuracy< 10ps, Precision <2ps

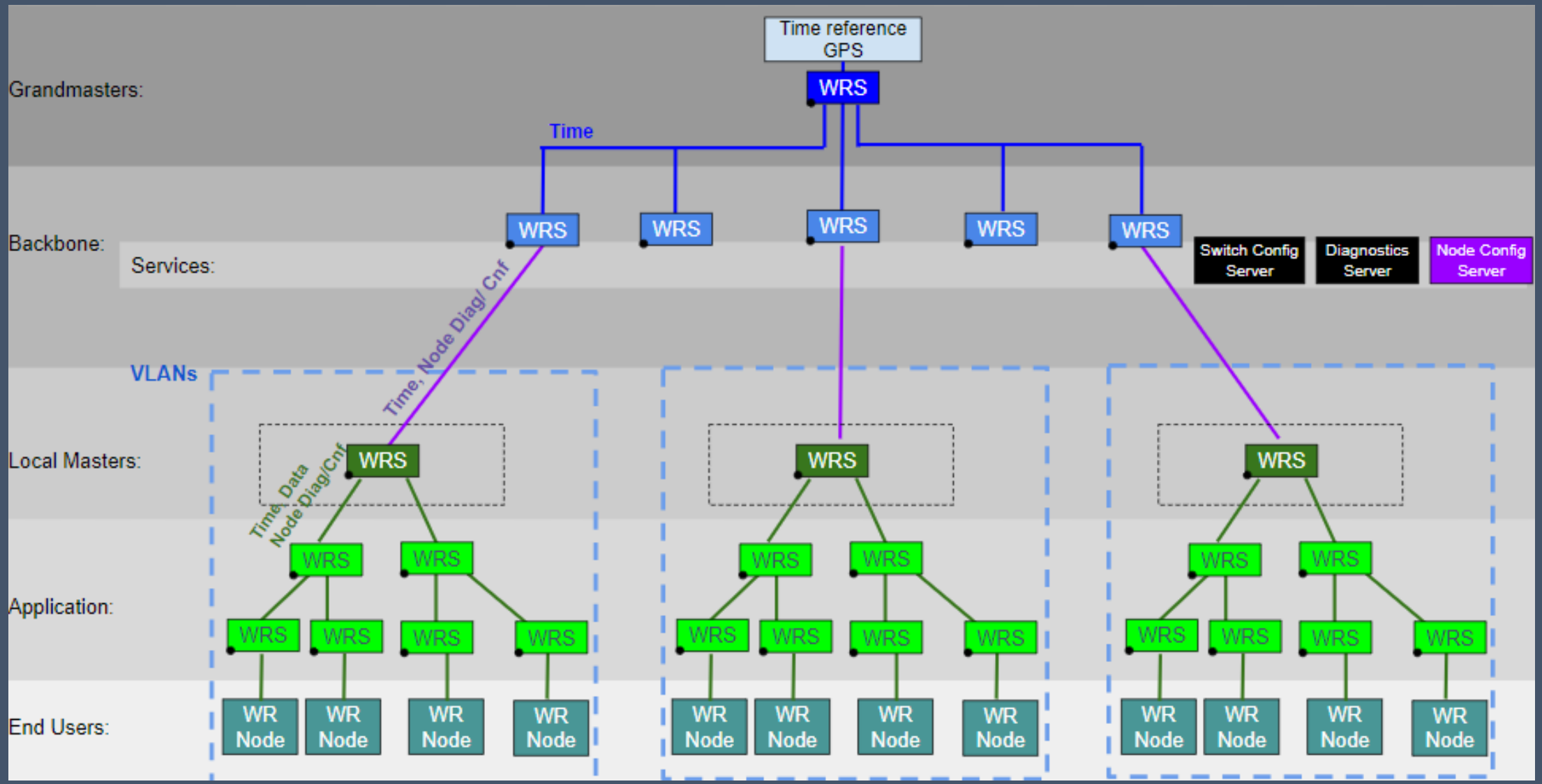


Trigger Distribution

1 switch, few nodes → 2024: 30 switches, 100 nodes
Generic framework for distributing triggers



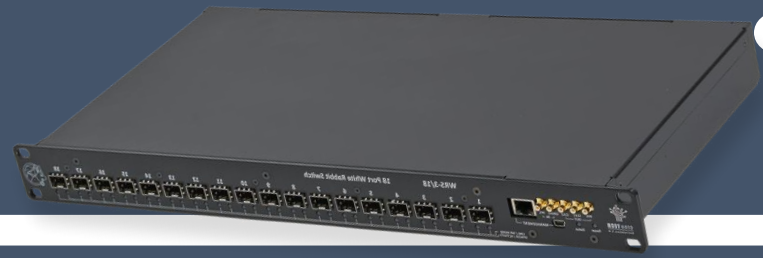
NETWORK ARCHITECTURE



HARDWARE

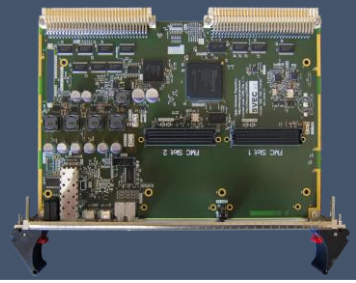
Switch

Mostly low-jitter

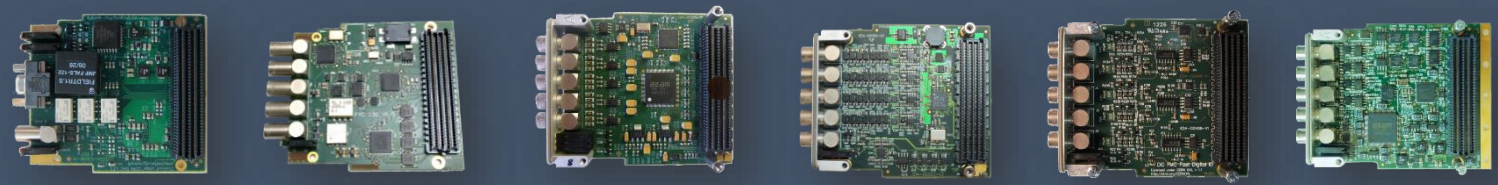


Nodes

Generic Carriers
PCIe, PXIe, uTCA, VME



App-specific Mezzanines



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WR Application Taxonomy

New Application: Accelerator Timing System

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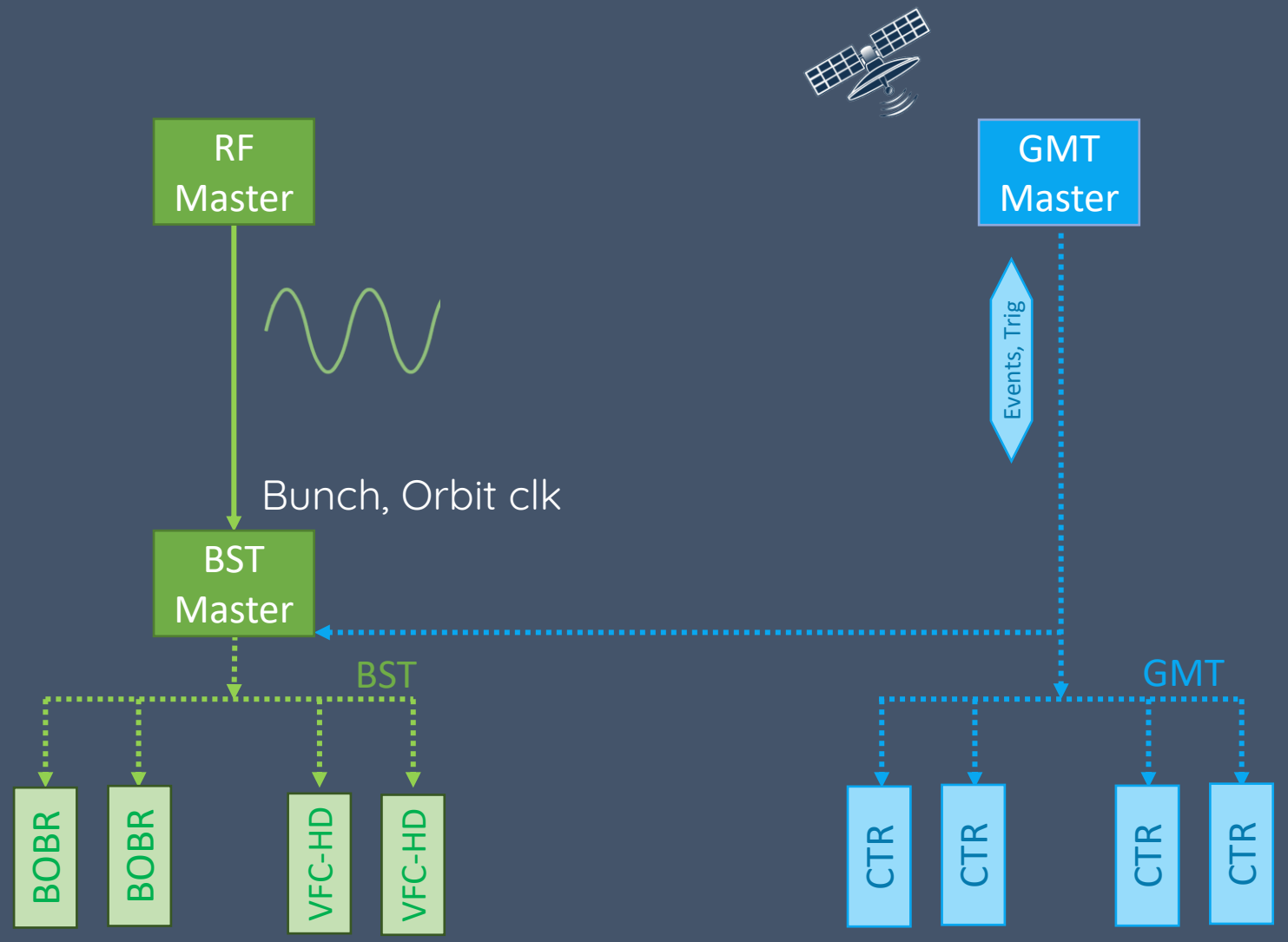
LHC CURRENT TIMING SYSTEMS (I)

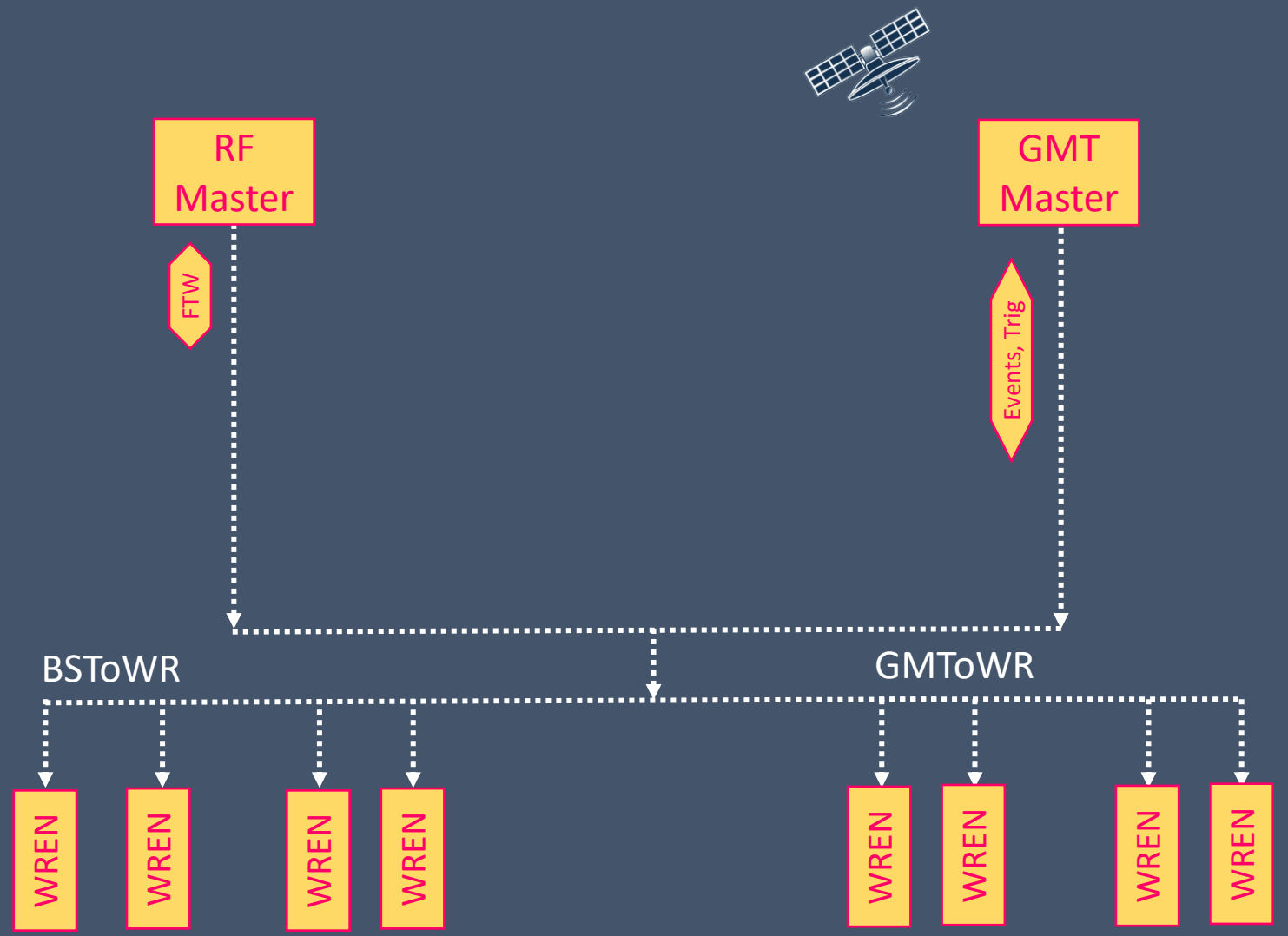
1. General Machine Timing _ GMT [UTC]
   - Event-based timing system
   - Distribution of events and triggers in real time
   - RS-485, Thousands of receivers
2. Beam Synchronous Timing _ BST [RF]
   - F_{rev} and Bunch clk distribution
   - Re-distribution of GMT events
   - Custom optical link, PLL_based receivers, Hundreds of receivers

LHC CURRENT TIMING SYSTEMS (II)



Analogue ——— Digital ·····

FUTURE UNIFIED TIMING SYSTEM



FUTURE UNIFIED TIMING SYSTEM

WR

- Synchronisation
- Data

GMT Data Master broadcasting

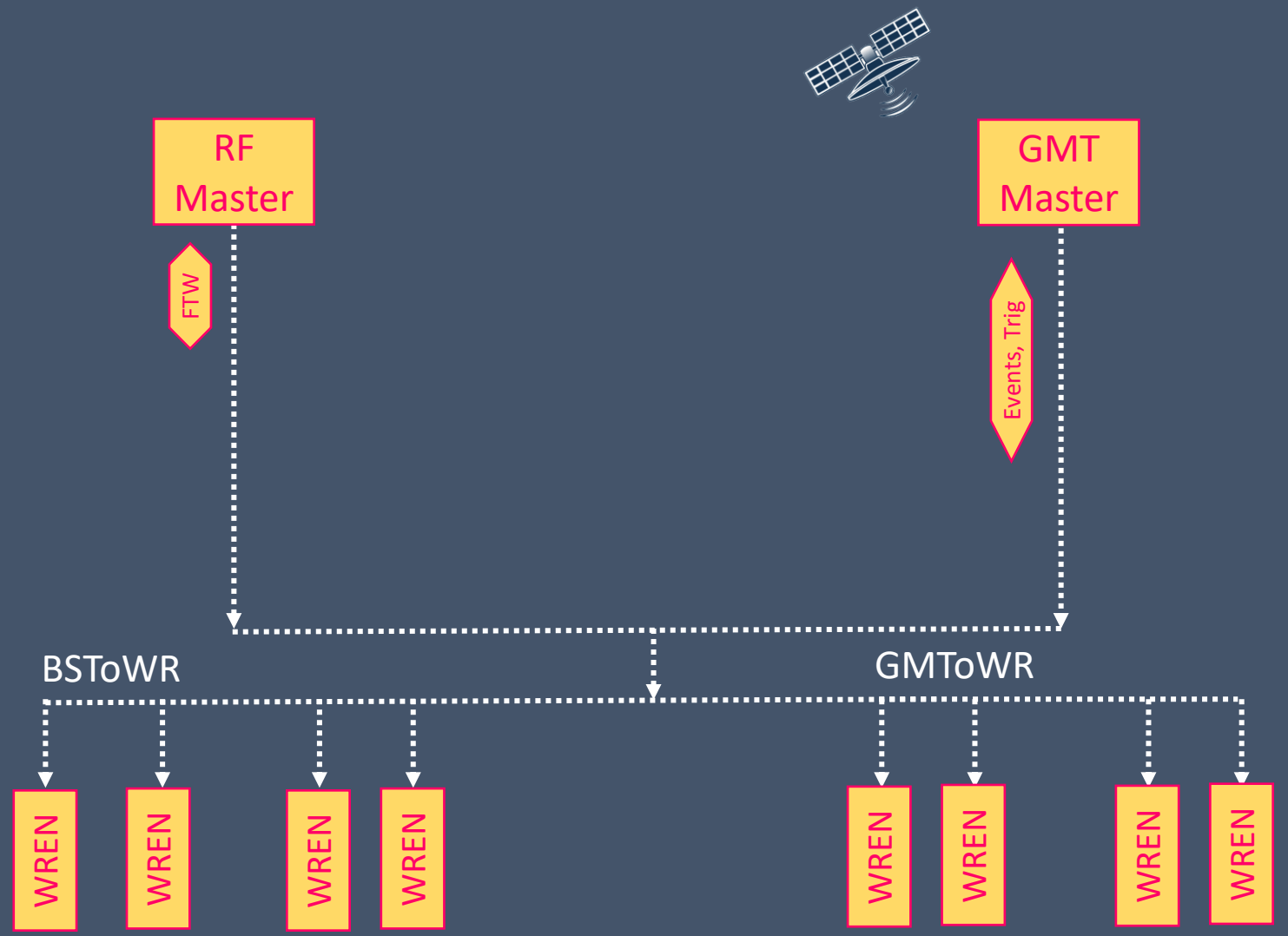
- Events with Absolute Due Time
- Parameters

RF Data Master broadcasting

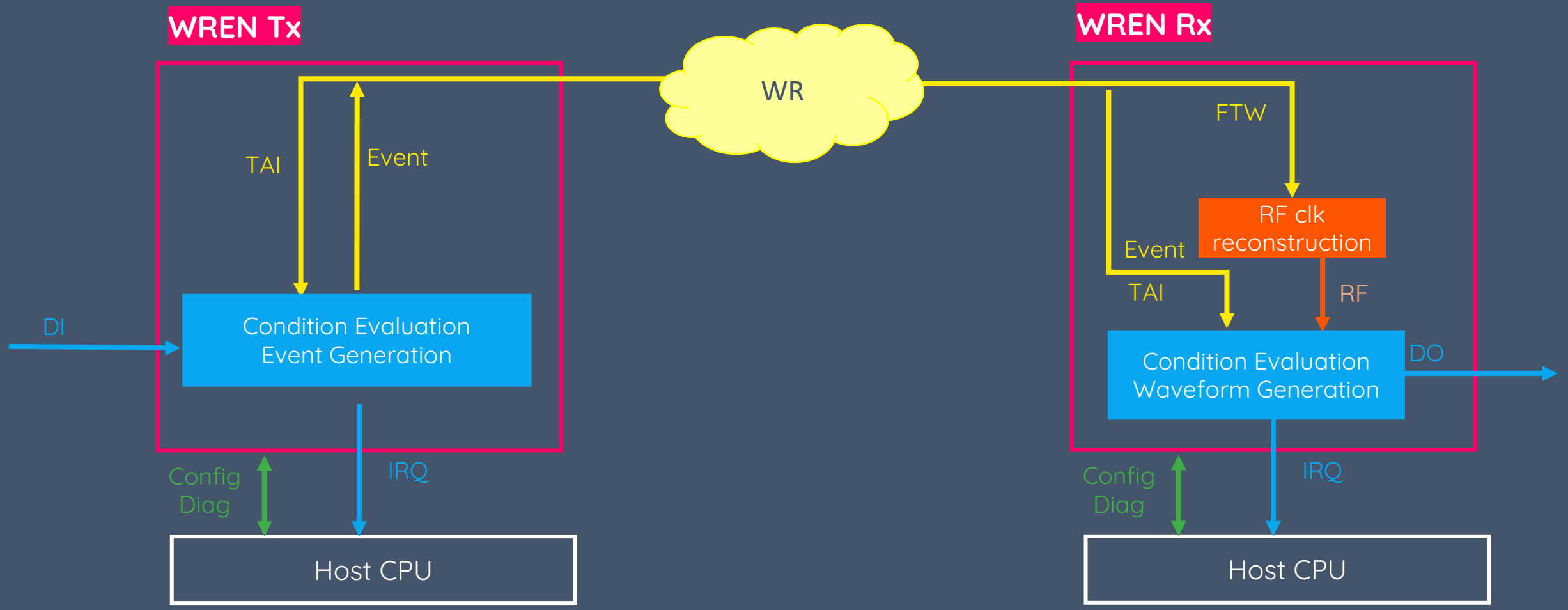
- Frequency Tuning Words

Nodes: WREN

- Two timescales: TAI, RF
- Matching conditions in event parameters
- Configurable generation of waveforms
- Traffic generation if needed



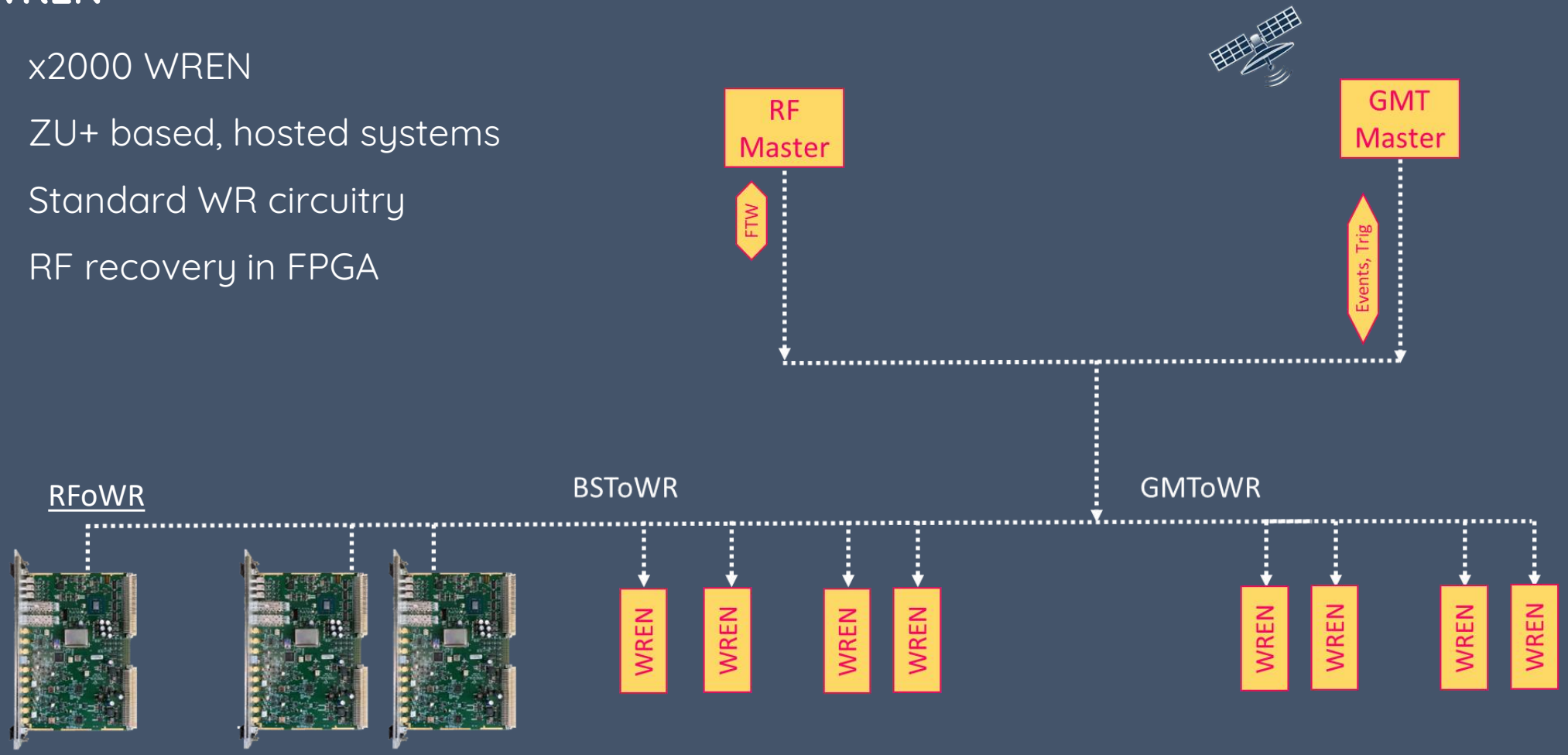
WREN: WR Event Node



Prototyping Phase

WREN

- x2000 WREN
- ZU+ based, hosted systems
- Standard WR circuitry
- RF recovery in FPGA



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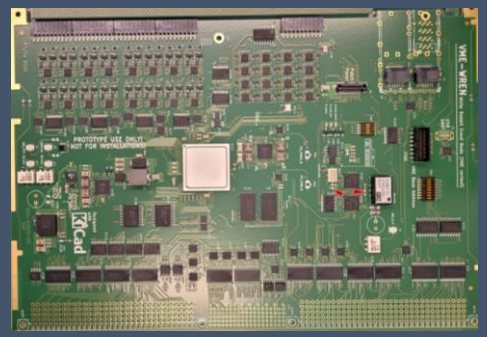
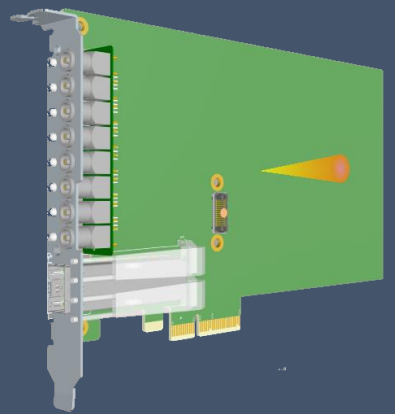
  - PXIe, VME, PCIe
- Dedicated team that adapts to the CERN needs





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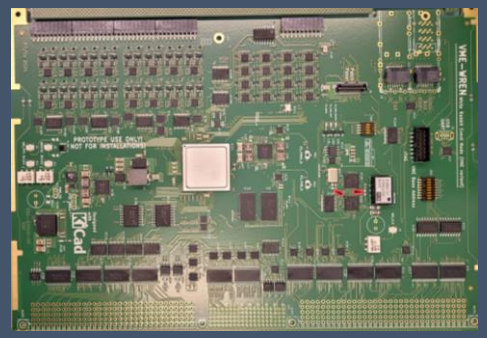
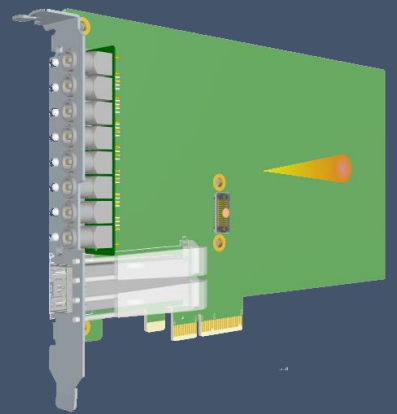
Network

- x200 WRSv3
- < 10km links, standard SFP
- Follow existing architecture rules
- Ongoing tests of synch performance after 6 layers of WRS-LJ;

  link down/up, reboots, constant

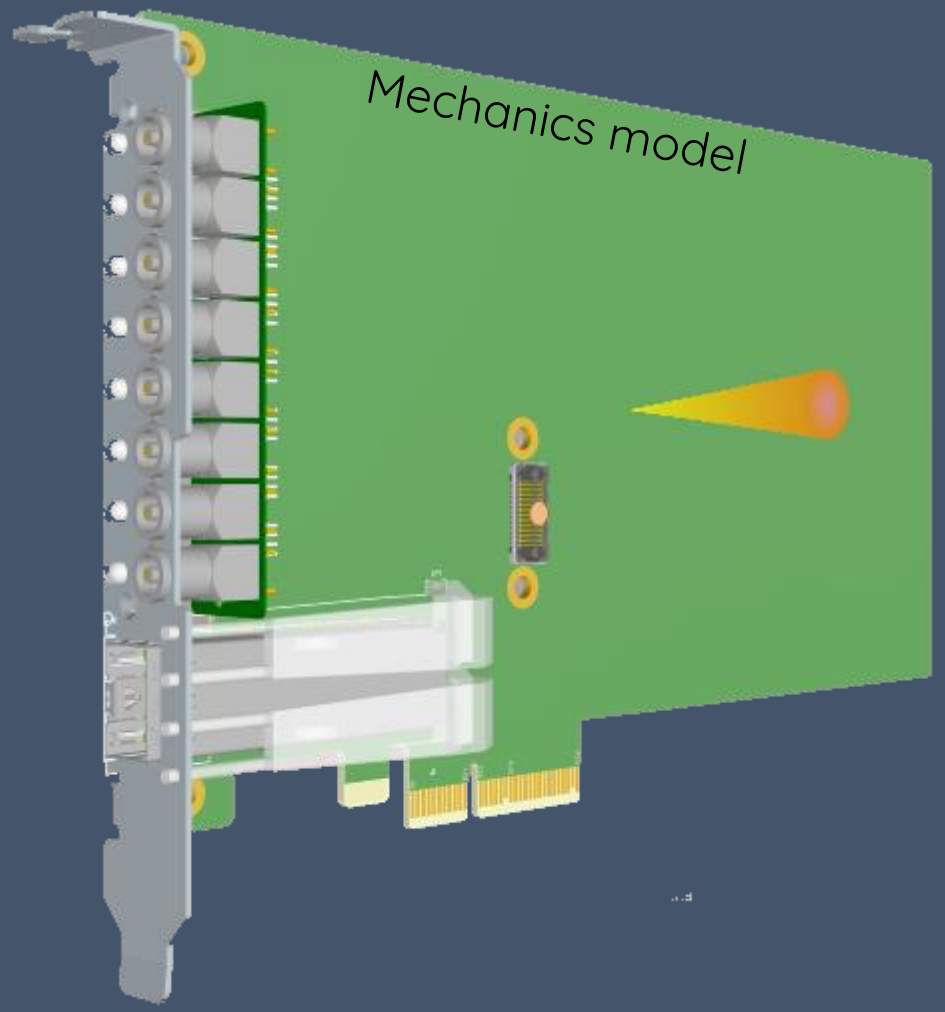




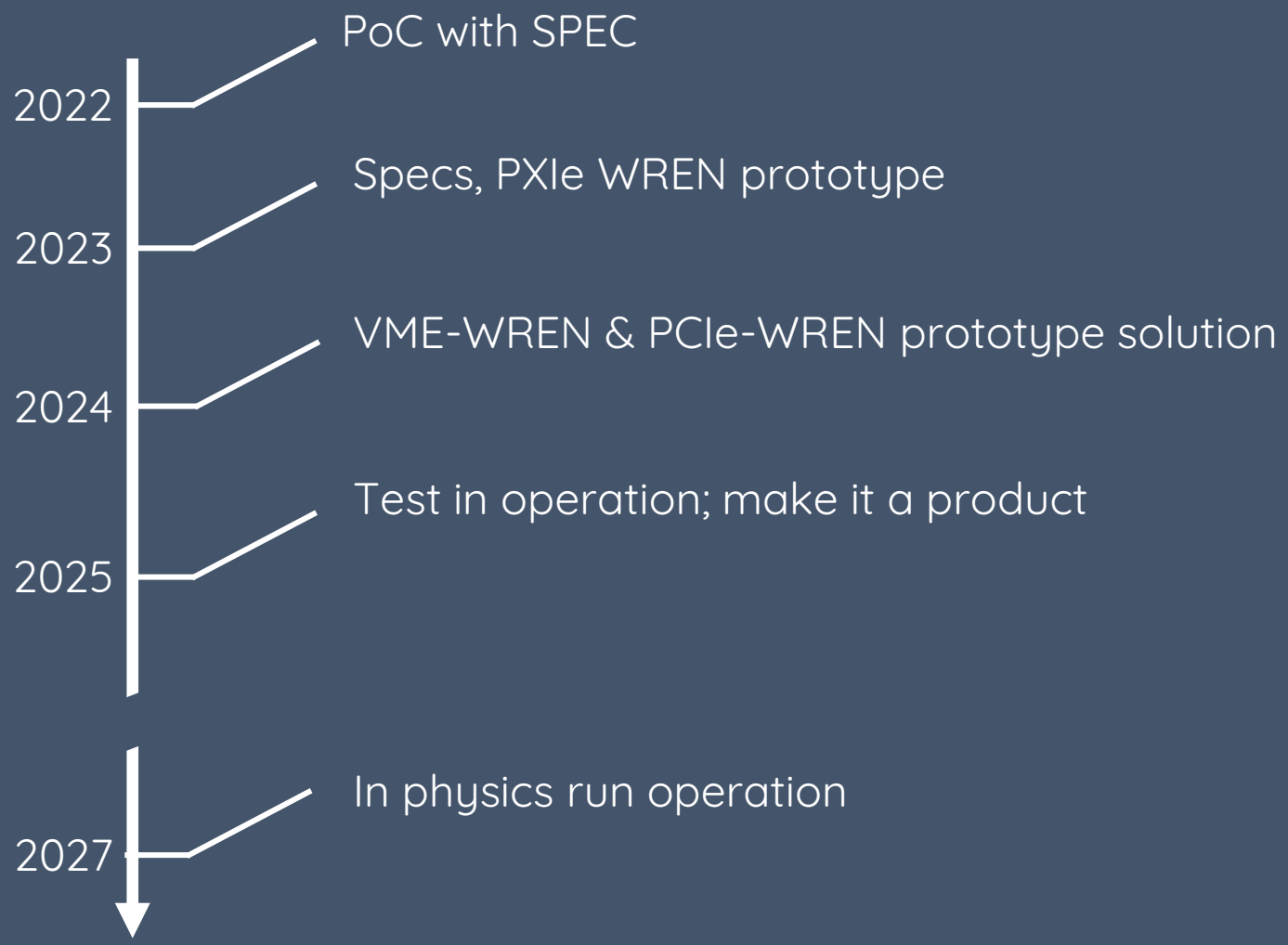
WR Starter-kit?

PCIe WREN

- Open source KiCad design
- WR synchronization
- Input signal timestamping
- Output signal: time-triggered pulse/ waveform
  - Modular front panel
- WR message generation
- Free resources for application-specific logic
- CERN-agnostic



Timeline & Next Steps

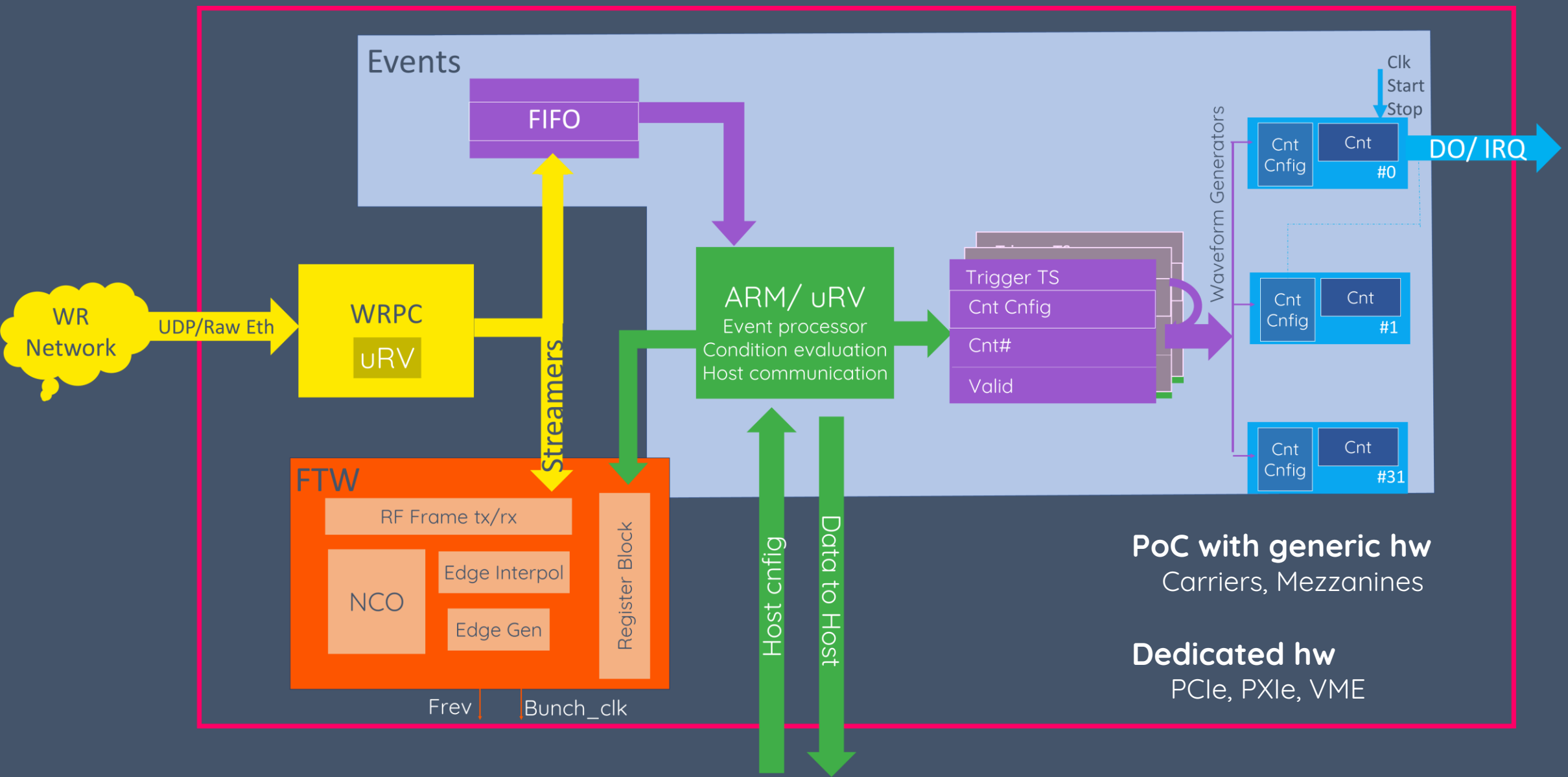


CONCLUSIONS

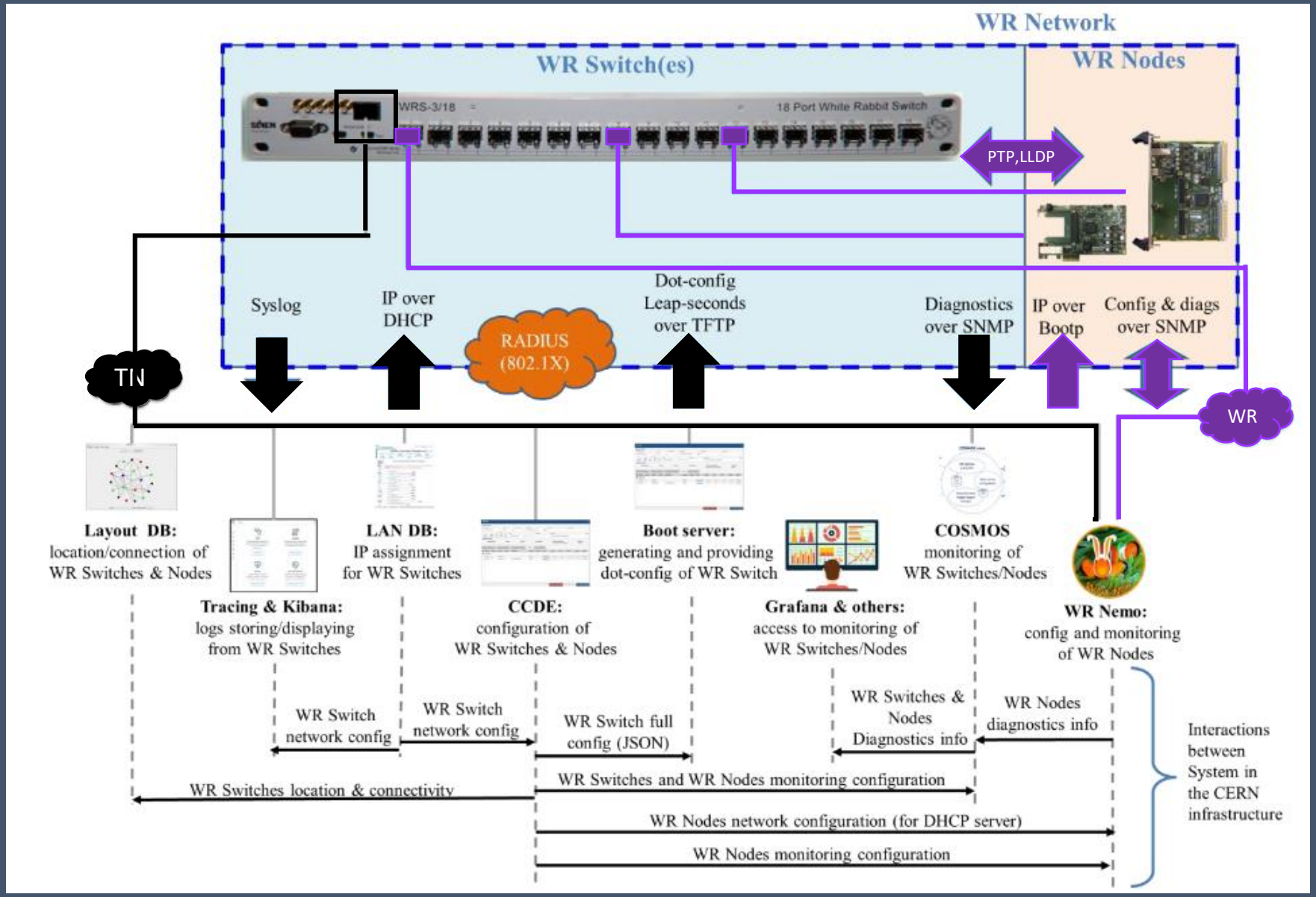
- Some critical WR installations and many more to come
- Reliable operation with Btrain, SPS LLRF, WRTD
- Clear installations strategy
- WRT: New Generic Timing System
- WREN: Generic WR Event Node

BACKUP

PoC


Events
FIFO
WR Network
UDP/Raw Eth
WRPC
uRV
Streamers
ARM/ uRV
Event processor
Condition evaluation
Host communication
Trigger TS
Cnt Cnfig
Cnt#
Valid
Waveform Generators
Clk
Start
Stop
Cnt Cnfig
Cnt
#0
#1
#31
DO/ IRQ
FTW
RF Frame tx/rx
NCO
Edge Interpol
Edge Gen
Register Block
Frev
Bunch_clk
Host cnfig
Data to Host
PoC with generic hw
Carriers, Mezzanines
Dedicated hw
PCIe, PXIe, VME

NETWORK ARCHITECTURE



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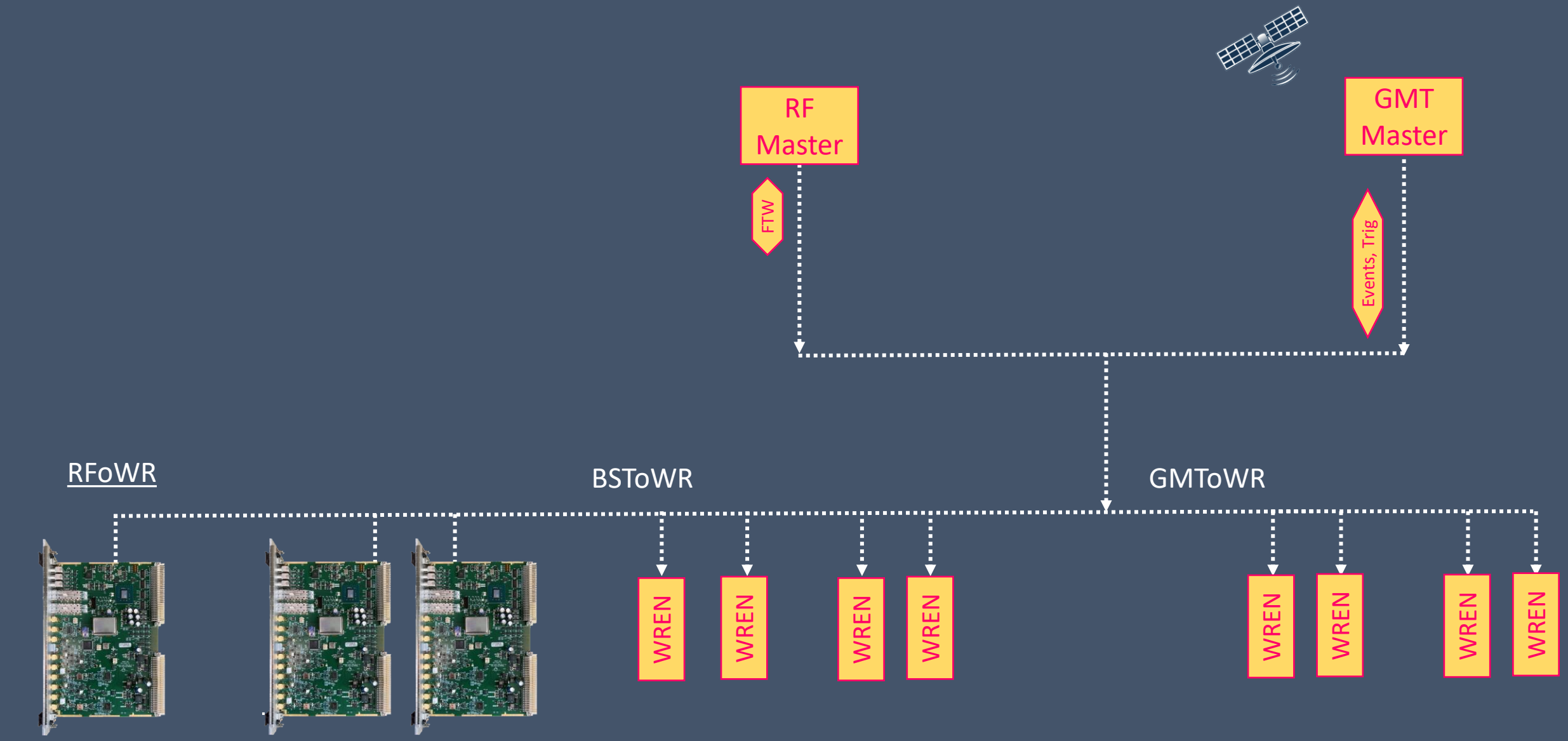

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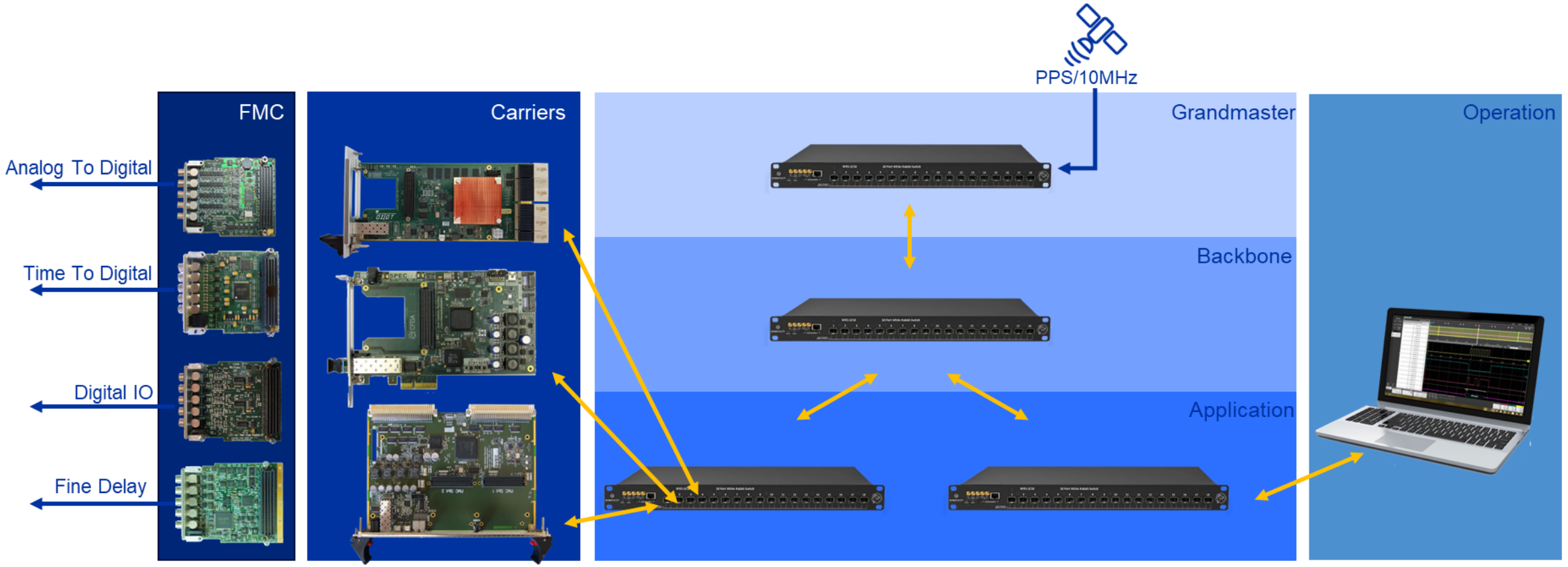
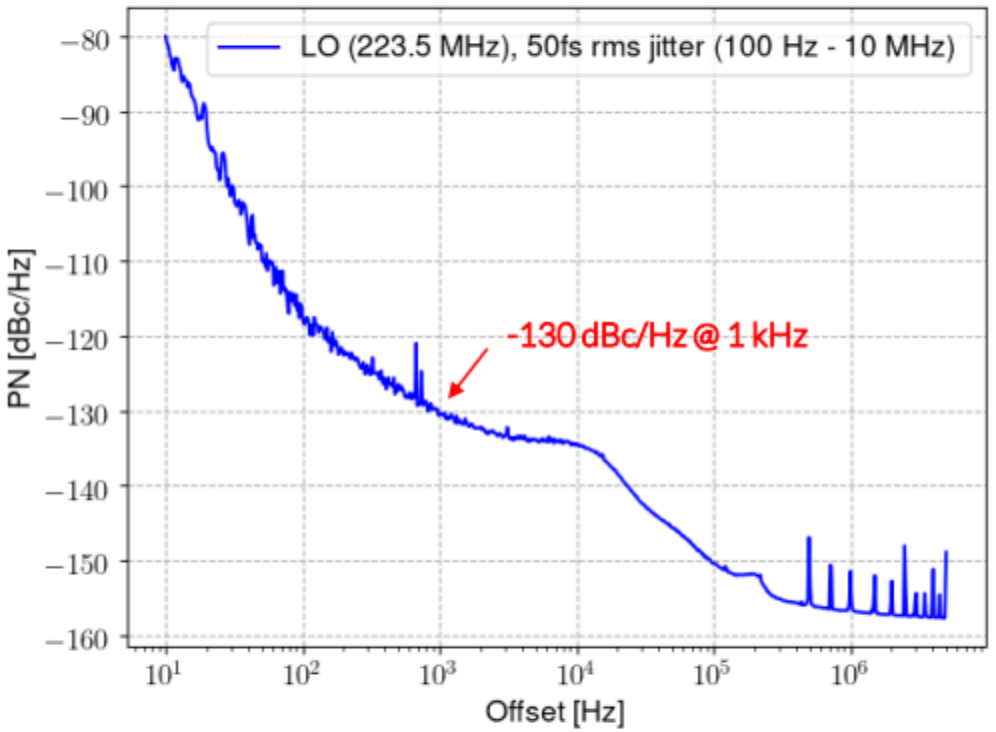
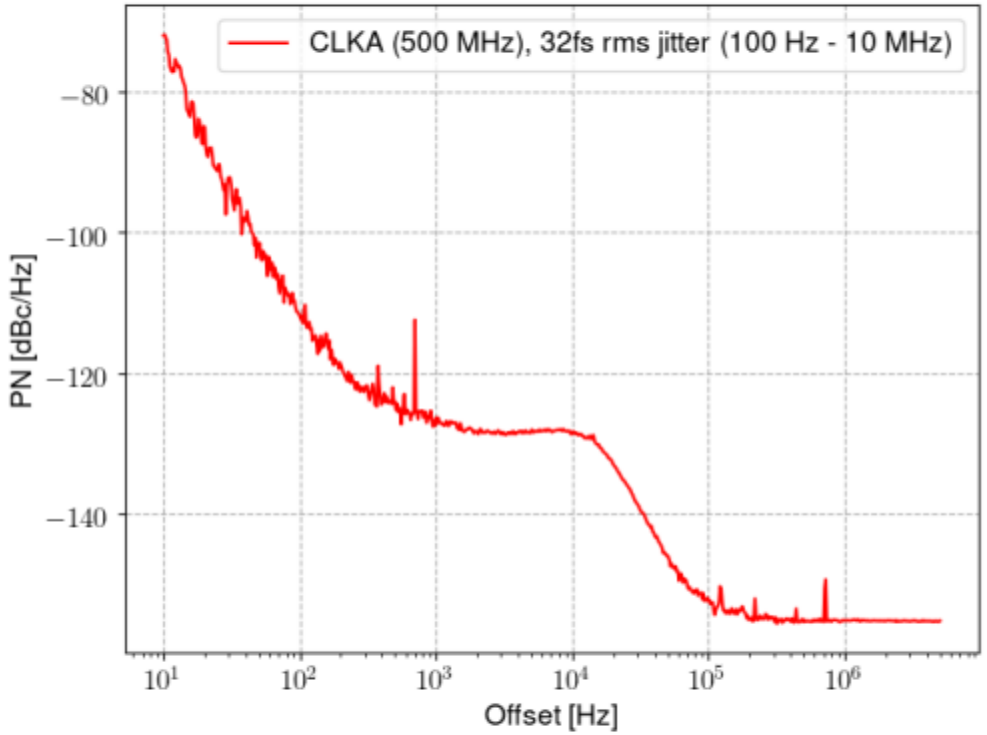


The eRTM14/15 PN measurements

LO (front panel) @ 223.5 MHz



CLKA (front panel) @ 500MHz



- DDS LO/REF PN of **-130.5 dBc/Hz** at 1 KHz (223.5 MHz), jitter **51 fs** (100 Hz – 10 MHz)
- CLKA PN of **-126 dBc/Hz** at 1 KHz (500 MHz), jitter **32 fs** (100 Hz – 10 MHz)
- Measured for front panel outputs of the eRTM14/15
- At these PN levels, even mechanical vibrations caused by cooling fans matter!