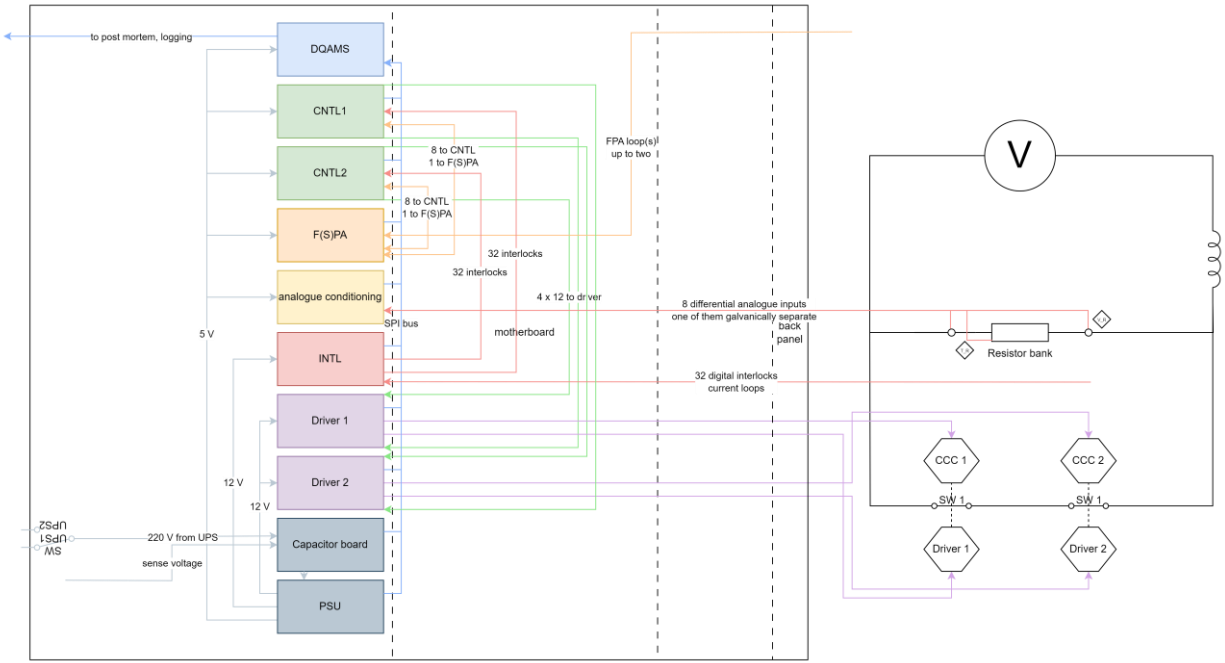
State of Study

Annotations following meeting

System Functional Diagram



Top-Level FMECA

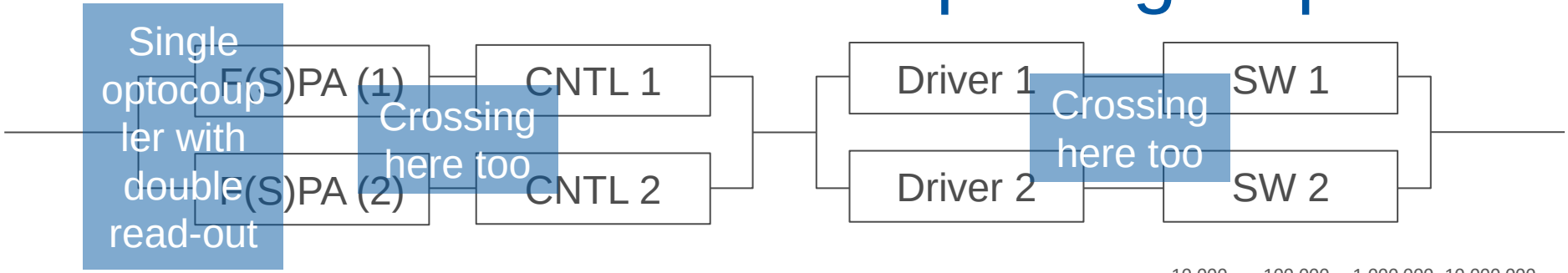
situation	function	failure mode	effect (worst case)	criticality/downtime	reliability target	comment
quench or powering failure	detect FPA loop open	fail to detect F		months	1/100y	
	drive switch opening	fail to drive sv		months	1/100y	
		successful ope				
	drive switch opening	preventing op		hours	1/y	
	collect data and transmit	fail to collect data and transmit (on time)	cannot restart machine until problem diagnosed	hours	1/y	
normal operation	detect FPA loop closed	fail to detect FPA loop closed	spurious dump or delay of fill	hours	1/y	
	continuously drive closed switch	spuriously open switch (with opening FPA loop)	spurious dump	hours	1/y	
		spuriously open switch (without opening FPA loop)	PC will trip and send FPA			
	collect data and transmit	fail to collect data and transmit (on time)	cannot restart machine until problem diagnosed	hours	1/y	
						there is no active protection of the switches by the EE controls in case of spurious opening, except vacuum switches
spurious opening of EE switches	detect switches opening	fail to detect switches opening (on time)	PC will trip and send FPA	hours	1/y	
	open FPA loop	fail to open FPA loop (on time)	PC will trip and send FPA	hours	1/y	
	open all other switches	(see above)				
	collect data and transmit	fail to collect data and transmit (on time)	cannot restart machine until problem diagnosed	hours	1/y	
interlock indicating unsafe operation	detect unsafe operation	fail to detect u			1/10y	better discuss on case by case
	open switches	fail to open sv			1/10y	better discuss on case by case
	open FPA loop	fail to open FP				
	collect data and transmit	fail to collect d		hours	1/y	
loss of mains power (opens switches)	open FPA loop	fail to open FP				
						there is no active protection of the switches by the EE controls in case of spurious opening, except vacuum switches
	open switches	fail to open sv				
	collect data and transmit	fail to collect d		hours	1/y	

1: open switch upon FPA loop opening

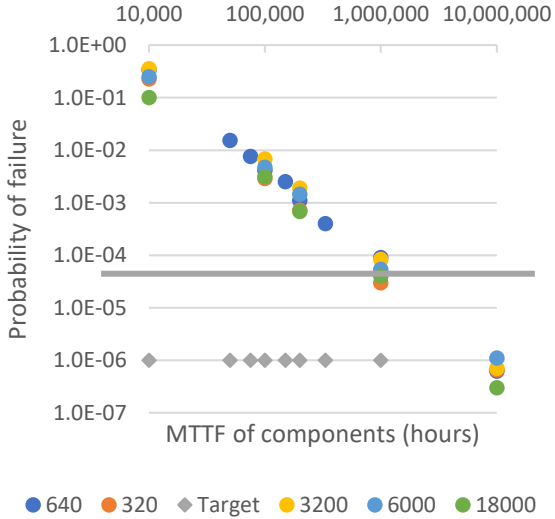
2: prevent operation if interlock detected

3: behaviour of new vacuum switches under loss of power

1: Simulation of switch opening request



- Simulation model of most critical function generated following last meeting
  - Failure if no path functional and demand (FPA open)
  - Considers that upon each demand, blind failures are discovered and fixed (e.g. if CNTL stopped triggering Driver 1)
- Used to estimate failure rate requirement for the “”boxes”
  - Demand interval varied between 13 and 750 days
  - Based on initial Top-level requirement, failure rate per box ~few hundred FITS (1E6 – 1E7 hours MTTF)
    - FITS: failures in 10^9 hours, example: single discrete components have <10 FITS



1: Simulation of switch opening request

Next steps

- Finalize top-level requirements
- Based on requirements, estimate whether boards fulfill them based on component prediction
  - To so so, would need design files (processed by design office) – so far: G:\Departments\TE\Projects\EnergyExtraction\UniversalElectronics\GLAB
  - Possibly: FMECA for selected boards to get components on critical path

Id	AlternatePN	Description	Category	PartNumber	Quantity	CategoryDescription	Page	failure_mode	Alpha	End Effect - User Permit	Comments
1.1	C2	~±10% 50V X7R SMD Multila	217-CA	CC0603_100NF_50V_10%_X7R	1	Capacitor	Critical Permit A	Open	6	False dump	
1.1	C2	~±10% 50V X7R SMD Multila	217-CA	CC0603_100NF_50V_10%_X7R	1	Capacitor	Critical Permit A	Parameter change	61	No effect	
1.1	C2	~±10% 50V X7R SMD Multila	217-CA	CC0603_100NF_50V_10%_X7R	1	Capacitor	Critical Permit A	Short	30	False dump	
1.1	C2	~±10% 50V X7R SMD Multila	217-CA	CC0603_100NF_50V_10%_X7R	1	Capacitor	Critical Permit A	Other	3	No effect	
10.1	C3	~±10% 50V X7R SMD Multila	217-CA	CC0603_100NF_50V_10%_X7R	1	Capacitor	Test & monitor	Open	6	False dump	
10.1	C3	~±10% 50V X7R SMD Multila	217-CA	CC0603_100NF_50V_10%_X7R	1	Capacitor	Test & monitor	Parameter change	61	No effect	
10.1	C3	~±10% 50V X7R SMD Multila	217-CA	CC0603_100NF_50V_10%_X7R	1	Capacitor	Test & monitor	Short	30	False dump	

End Effect	Definition
Blind failure - CIBF	both channels fail
Blind failure - path	a single channel fa
False dump	tranmission of a sp
Maintenance	allows the current
No effect	having no effect o

2: Critical interlocks?

- Document and clarify
  - Discussed e.g. interlock based on dump resistor temperature

3: Behavior of new vacuum switches under loss of power

- Clarify and document
  - New vacuum switches have to be latched not to re-close
  - Clarify and check whether failure rate estimation also necessary

Notes (raw)

- Bozhidar - state of EE
  - chassis electronics able to serve all (beyond HL LHC)
    - vacuum, IGBT, FRESCA, Prevessin test station
    - programming of control cards different
    - only connectors different (chassis backpanel)
    - PSU & capacitor boards may still change
    - universal motherboard
    - backpanel connected to other side of motherboard; connectors adapted to system
- current progress
  - made prototype for vacuum switch (most urgent)
  - launched pre series of ten systems for testing in poland and in charm
  - series design -> little changes by end of sept
    - have tester for PCBs
    - boards are not testable yet
  - launch production Jan/Feb next year
    - go to design office with big order

Notes (raw)

- our state of study
  - slide 4: neach FPA channel is actually going to both
    - depending on system different situation
      - vacuum system
    - focus on vacuum switches
      - needs power upon loss
- next steps
  - link to GLAB
  - vacuum switch critical path
    - FPA
    - critical interlock
    - no electricity
  - use a single optocoupler with two outputs
  - driver card
    - can be optocoupler (13KA) or relays (600A)
    - vacuum sw
      - three operations
        - open switch
          - pre charged capacitor
          - done by two fibers
          - same for sw2
        - kill the arc
          - pre charged capactiro
          - after delay activated
          - two fibers
            - same for sw2
        - trigger CC in opposite direction
          - kill the arc in the other direction
          - (mainly needed for D1 & D2)
        - all done in microseconds
        - keep non vacuum switches with relays in mind
    - other switches
      - always two relays in series
      - EM switches
        - cut current - switch opens (slow due to magnetization) - controlled by two relays
        - transistor to push opening - faster than relay
        - both fast enough (redundant)
    - bozhidar prepares diagram for vacuum specifically
    - meanwhile we get the full schematics
    - electricity
      - UPS 1&2
      - distribution box
        - regular circuit breakers
        - emergency stop
      - transfer switch
        - single line goes to cluster of outlets
      - monitor the output line + line to each vacuum drivers is monitored as well --> fiber to interlock board + 24V transformed -> two PSUs redundant - also monitored (four wires)