Universal EE Controls Reliability Study

Progress Meeting #2

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Study workflow
Steps followed in the reliability analyses in BISv2

Failure Rate prediction

- 217Plus standard
- Completed with automated tools & Isograph.

Outcomes:
Estimation of failure likelihoods for individual components, system and sub-systems.

Failure Modes apportionment

- Sources:
  - FMD-91 (after MIL-HDBK-338B [1])
  - FMD-2016 [2]
  - Expert knowledge
- Final table in [3]

Outcomes:
Failure modes (e.g., capacitor open, short) with assigned probabilities.

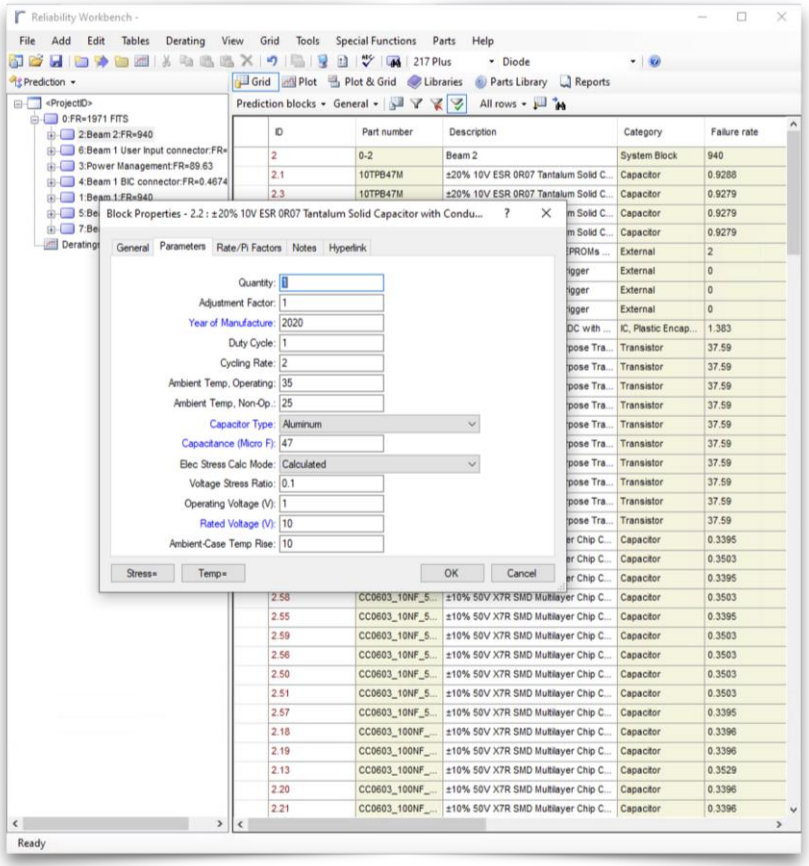
End-effects assignment

- Provided by system expert.
- Discussed with reliability expert

Outcomes:
Establishing probability for each failure end-effect (that are then comparable with risk matrices).

Failure rate prediction
217Plus standard & Isograph

- **Objective:** establishing probabilities of failure for individual components.
- **217Plus: 2015 & Isograph:** completed by using 217Plus models [4] in Isograph [5], aided by automated scripts processing design files [6].
- **Failure models:** combine empirical data with physics-of-failure models, being adjustable for specific environmental and operational conditions.
  - Factors like temperature, voltage, environment adjustable for components depending on the category
  - Certain parameters can be set globally to apply to all components (see next slide).



Screenshot of Isograph Reliability Workbench [2] (tool used for FMECA analysis)

Assumptions
Global parameters and mission profile

Year of manufacture: 2020

Duty cycle: 1 (i.e., always on)

Cycling rate: 2 (i.e., two power cycles in a year)

Ambient temperature, operating: 35

Ambient temperature, non-operating: 25

Relative humidity: 0.5

2.2.1.1 Global Constants

Several variables are common to all 217Plus™ component models. These are known as global parameters. These global parameters are as follows:

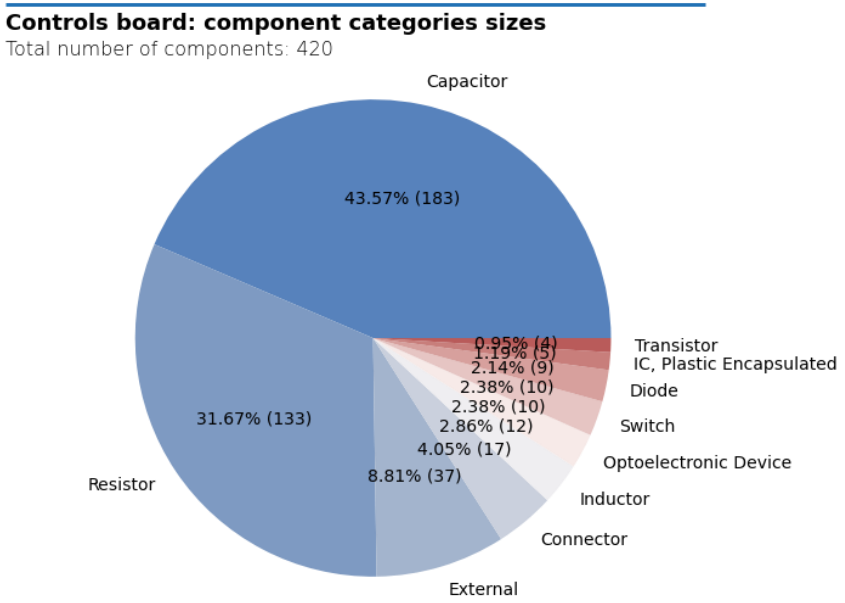
Y	=	Year of manufacture
D	=	Duty cycle (the percent of calendar time that the system in which the component is operating is in an operational state)
T_{AO}	=	Ambient temperature, operating (in degrees C)
T_{AE}	=	Ambient temperature, nonoperating (in degrees C)
CR	=	Cycling rate (the number of power cycles per year to which the system is exposed). In this case, it is assumed that the system transitions from a nonoperating environment to an operating environment at the same time that the power is applied.
RH	=	Relative humidity

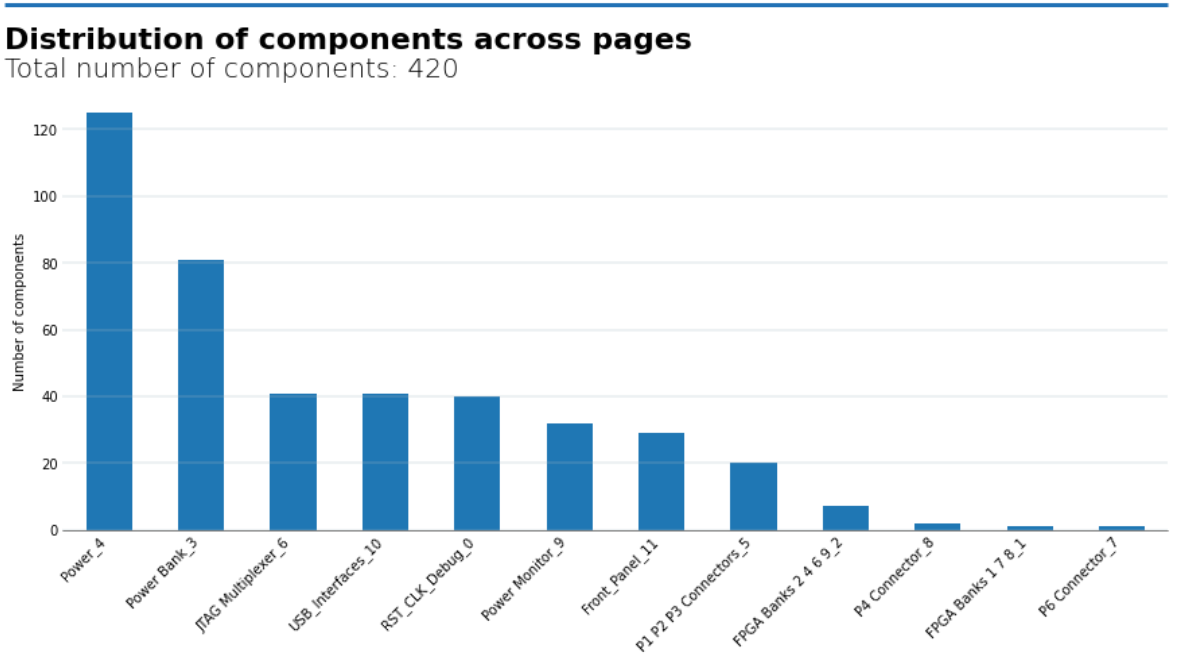
Excerpt from the 217Plus document [7]

Parts assumed to be used within their ratings, no modifications made to quality and process factors (217Plus standard assumed).

Controls board
Statistics

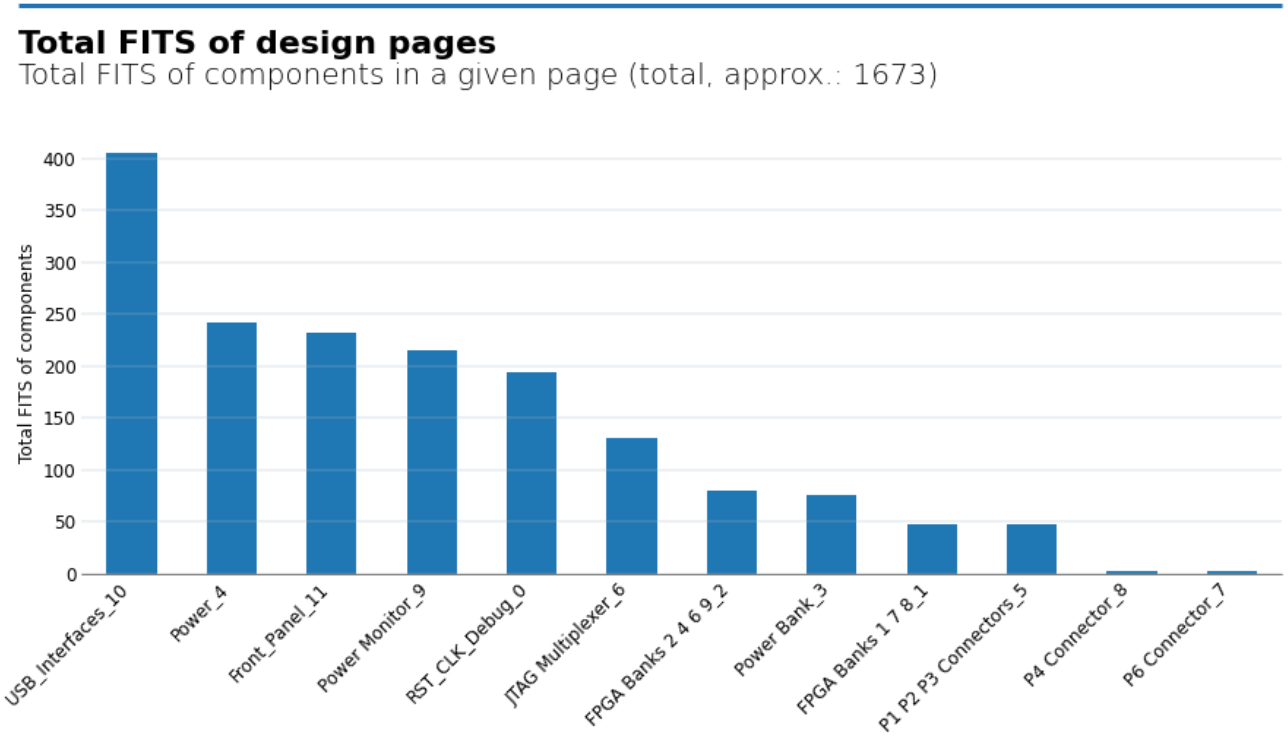
- **133 resistors and 183 capacitors**
- **37 “external” category components**
  - Mix of various components, such as fuse, DCDC converter, multiplexers, FPGA, etc.
- **Components distributed unevenly across pages**
  - Power – 125
  - Power bank– 81
  - JTAG Multiplexer, USB Interfaces, RST CLK Debug – ~40
  - Power Monitor – 32
  - Front Panel – 29
  - P1 P2 P3 connectors – 20

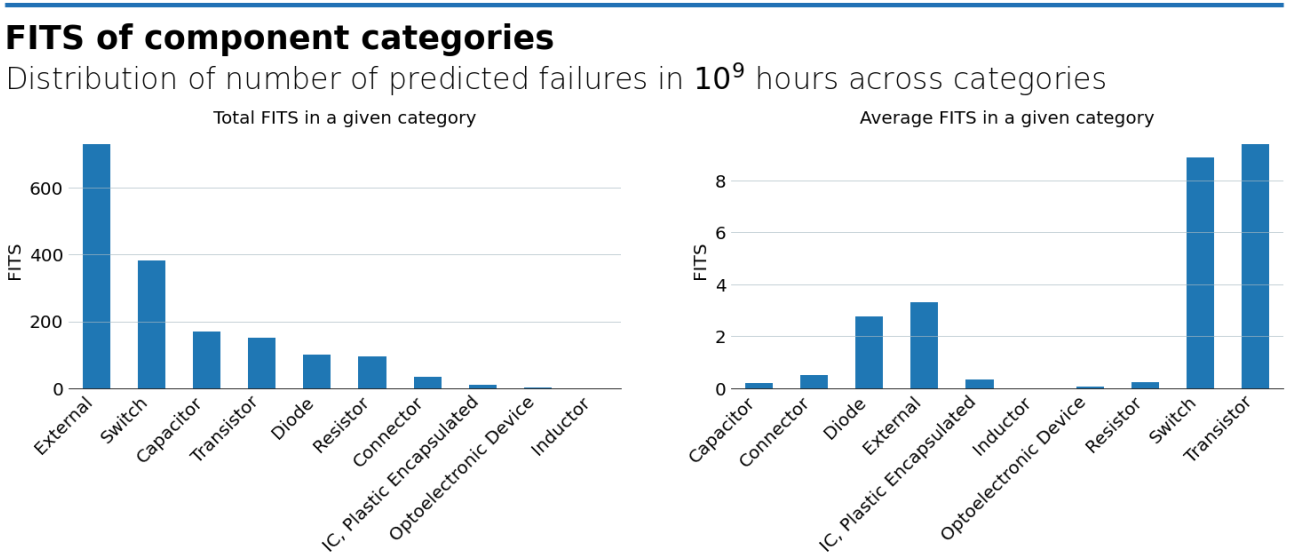




Controls board
Failure rates

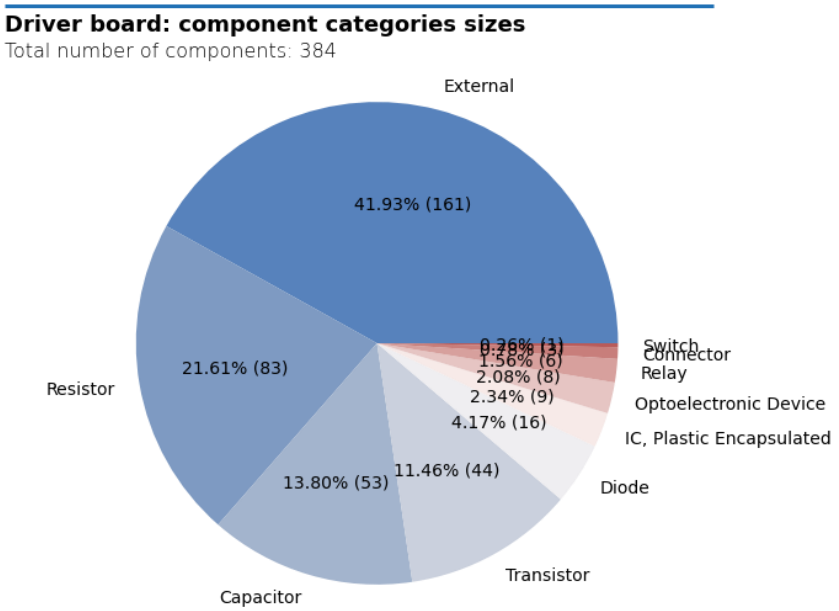
- **Total failure rate: 1,673 FITs**
- **Externals change the results**
  - Total contribution very small: 731 FITs
  - Test points, Through Hole Pads, Fiducial Targets **all assigned 0 FITs**
  - Remaining ones: assigned failure rates from the manufacturers data
- **Top contributors:**
  - EconoReset and 6 switches: 52 FITs each
  - Quartz Crystal: 48 FITs (MIL-HDBK-217F)
  - 4 Op Amps: 37 FITs
  - 2 TVS diodes: 31 FITs
  - FPGA: 8 FITs
  - Oscillator IQD: 7.76 FITs

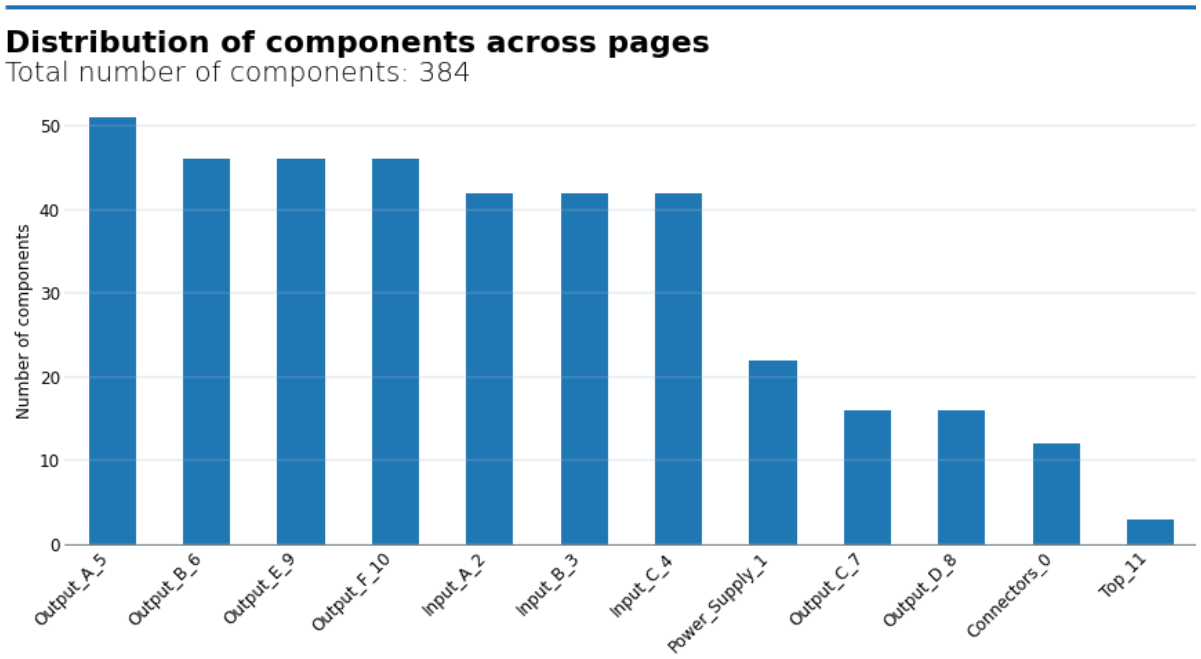




Driver board Statistics

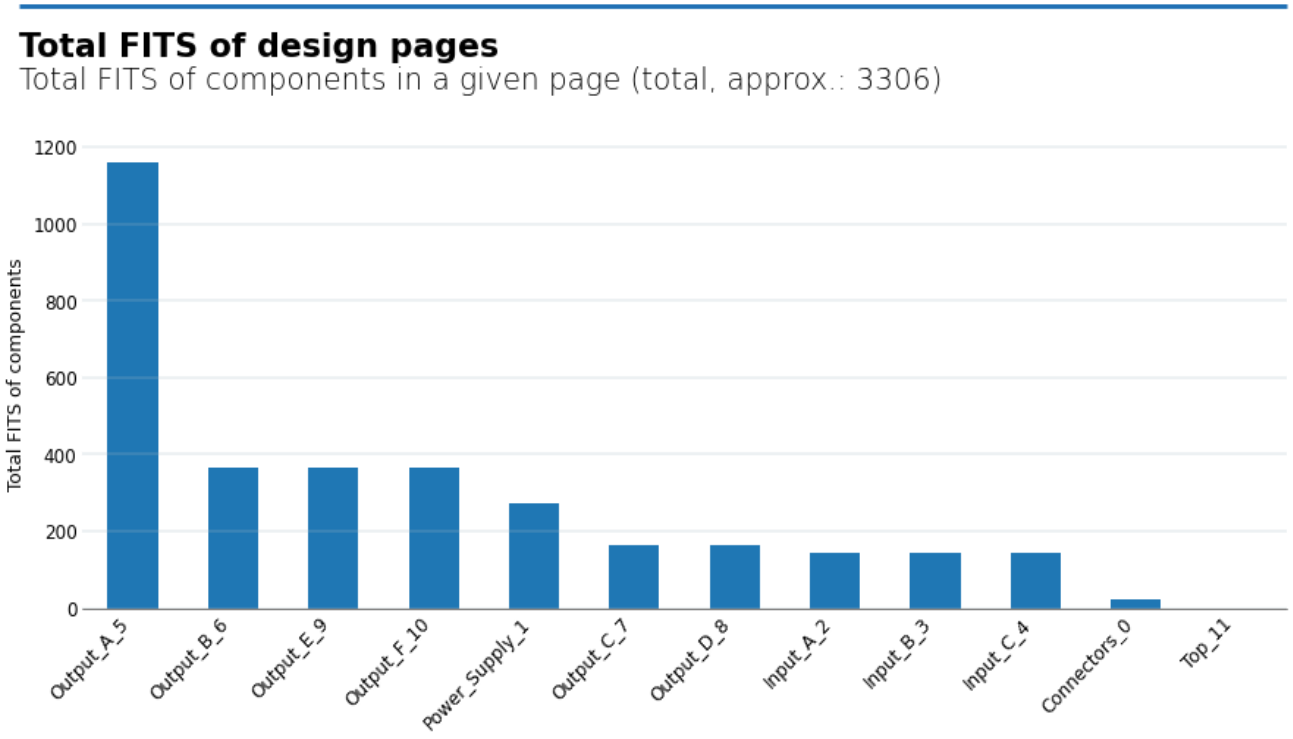
- **Large share of externals**
  - Mostly:
    - Test points
    - Through Hole Pads
    - Fiducial Targets
  - Remaining ones: EEPROM (IC1) and two regulators (IC2 & IC3) and Fuse (F1 & F2)
- **83 resistors and 53 capacitors**
- Components distributed across pages
  - Output A: 51
  - Outputs B, E, and F: 46
  - Output C, D: 16
  - Input A, B, C: 42
  - Power Supply: 22

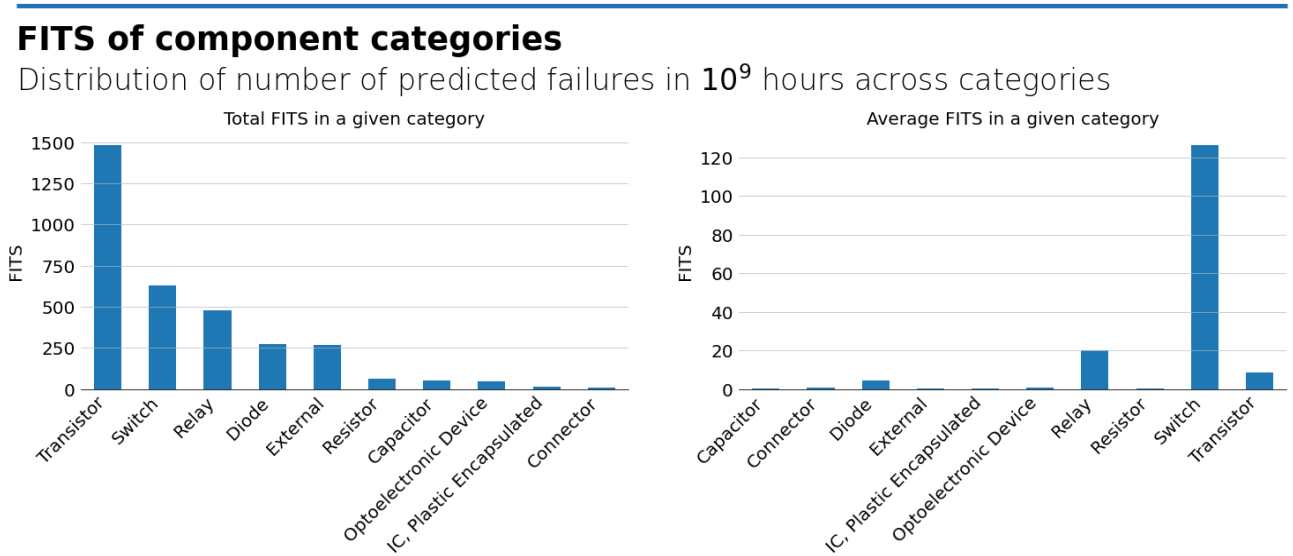




Driver board
Failure rates

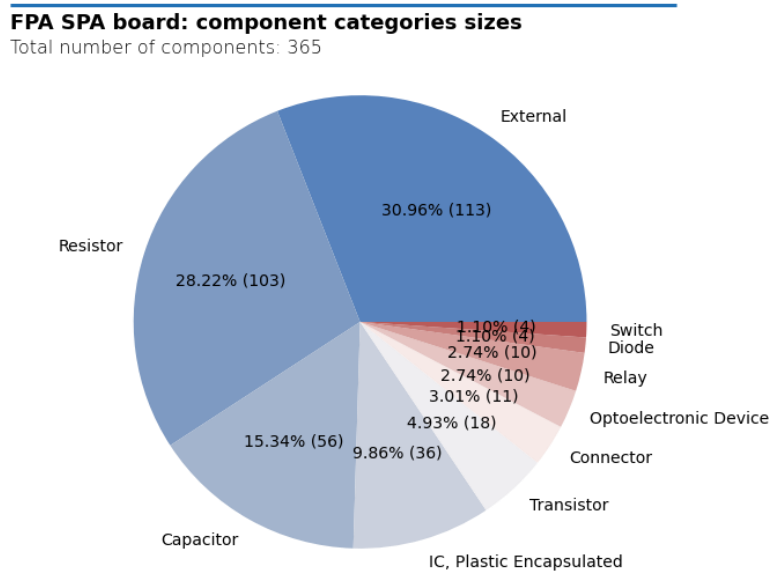
- **Total failure rate: 3,306 FITs**
- **Externals total contribution: 266.4 FITs**
  - Test points, Through Hole Pads, Fiducial Targets all assigned 0 FITs
  - Remaining ones:
    - Fuse – 2 x 20 FIT x 6 modes
    - EEPROM (IC48): 2 FIT x 6 modes
    - Two regulators (IC26 & IC29): 2 x 1.2 FITx 6 modes
- **Top contributors:**
  - 1 switch: 630 FITs
  - 6 relays: 80 FITs each
  - 16 PNP transistors: 37 FITs each
  - 8 TVS diodes: 31 FITs each (because of overrating; operating voltage – default 3.3V)
  - 28 NPN transistors: 31 FITs each

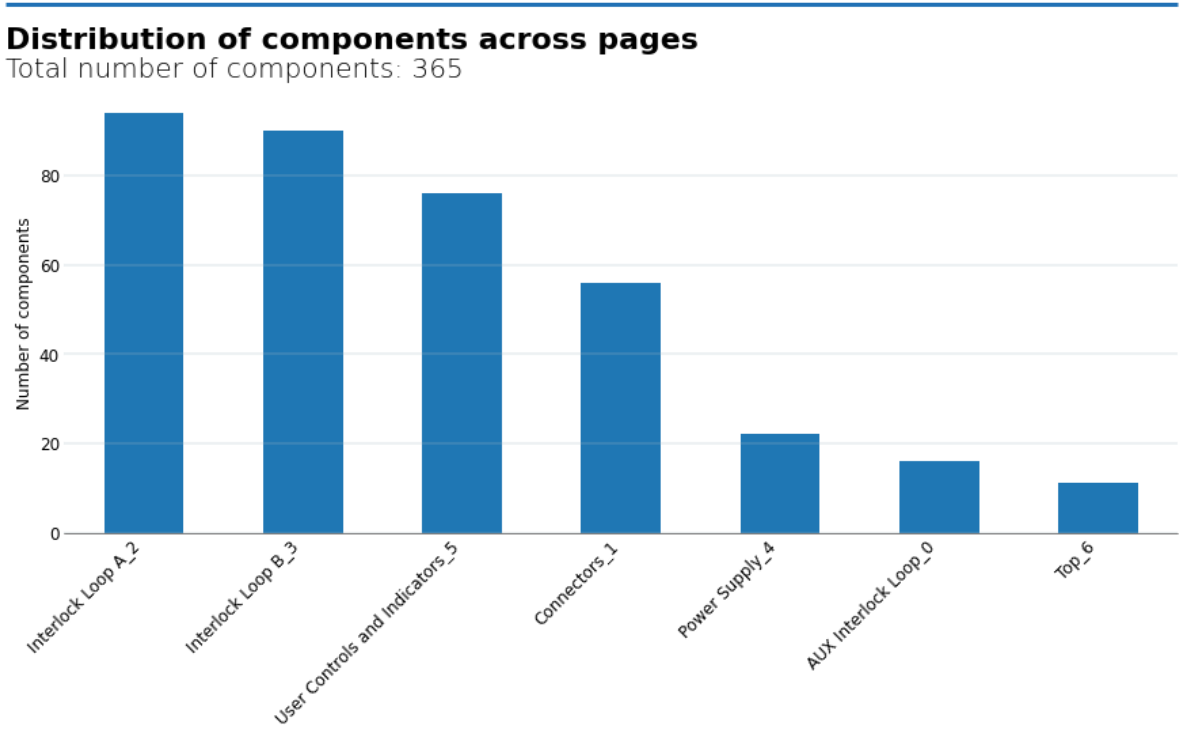




FPA SPA board Statistics

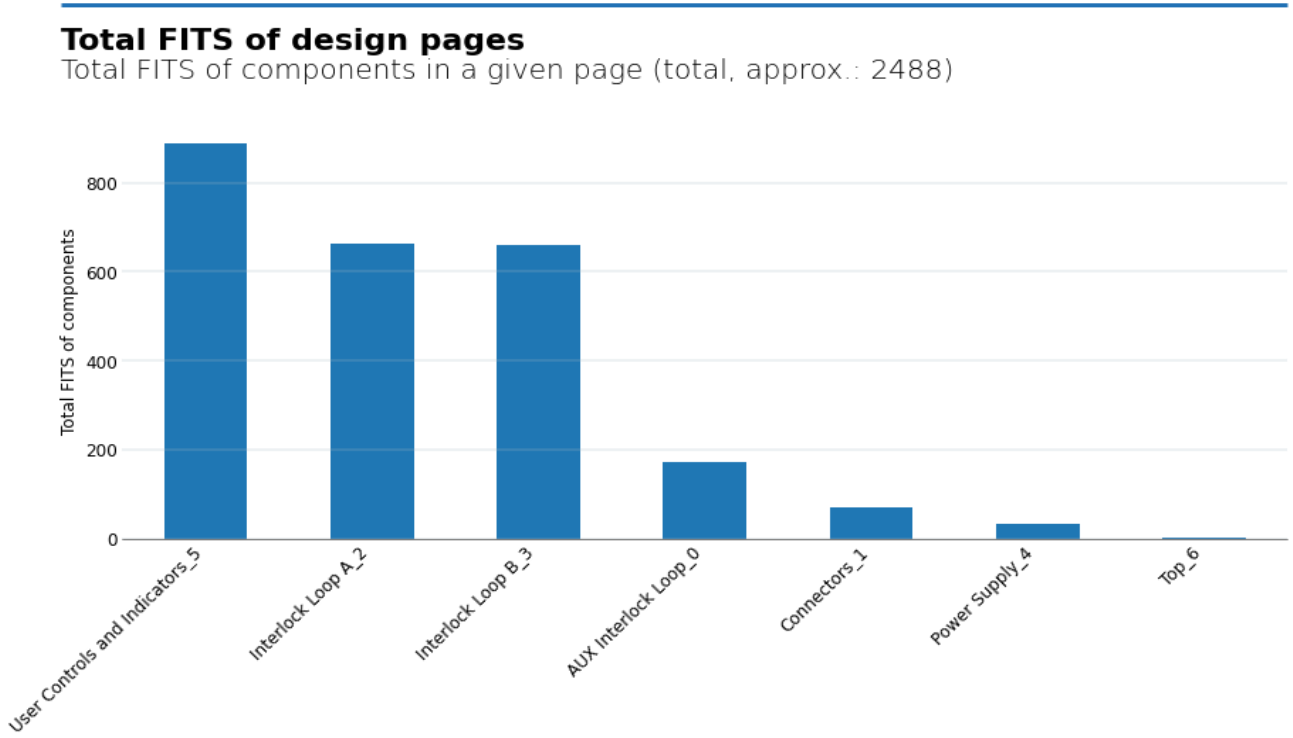
- **Large share of externals**
  - Mostly:
    - Test points
    - Through Hole Pads
    - Fiducial Targets
  - Remaining ones: EEPROM (IC48) and two regulators (IC26 & IC29)
- **103 resistors and 56 capacitors**
- Components distributed across pages
  - Interlock Loops more than 80 – difference between A and B?
  - User Controls and Indicators – 76
  - Connectors – 56

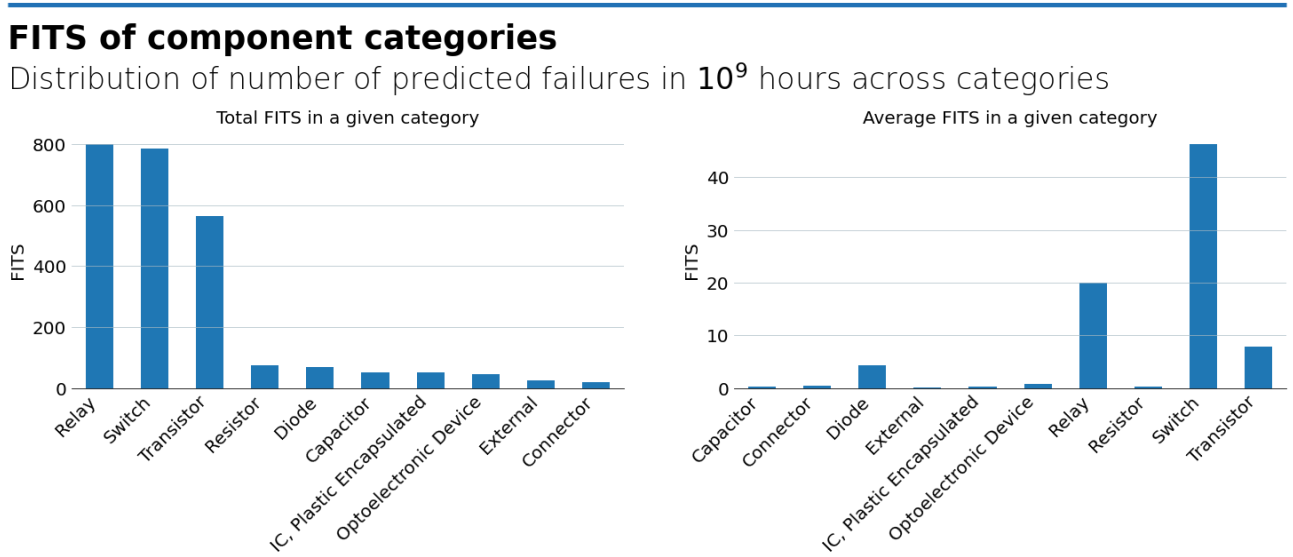




FPA SPA board
Failure rates

- **Total failure rate: 2,488 FITs**
- **Externals do not change the results much**
  - Total contribution very small: 26 FITs
  - Test points, Through Hole Pads, Fiducial Targets all assigned 0 FITs
  - Remaining ones:
    - EEPROM (IC48): 2 FIT x 6 modes
    - Two regulators (IC26 & IC29): 1.2 FITx 6 modes
- **Top contributors:**
  - 10 relays: 80 FITs each
  - 3 push buttons: 52 FITs each
  - 18 NPN transistors: 31 FITs each
  - 2 TVS diodes: 31 FITs each (because of overrating; operating voltage – default 3.3V)



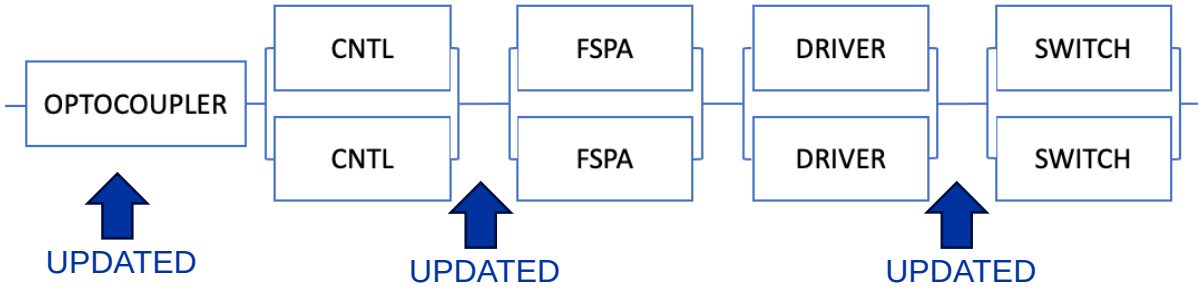


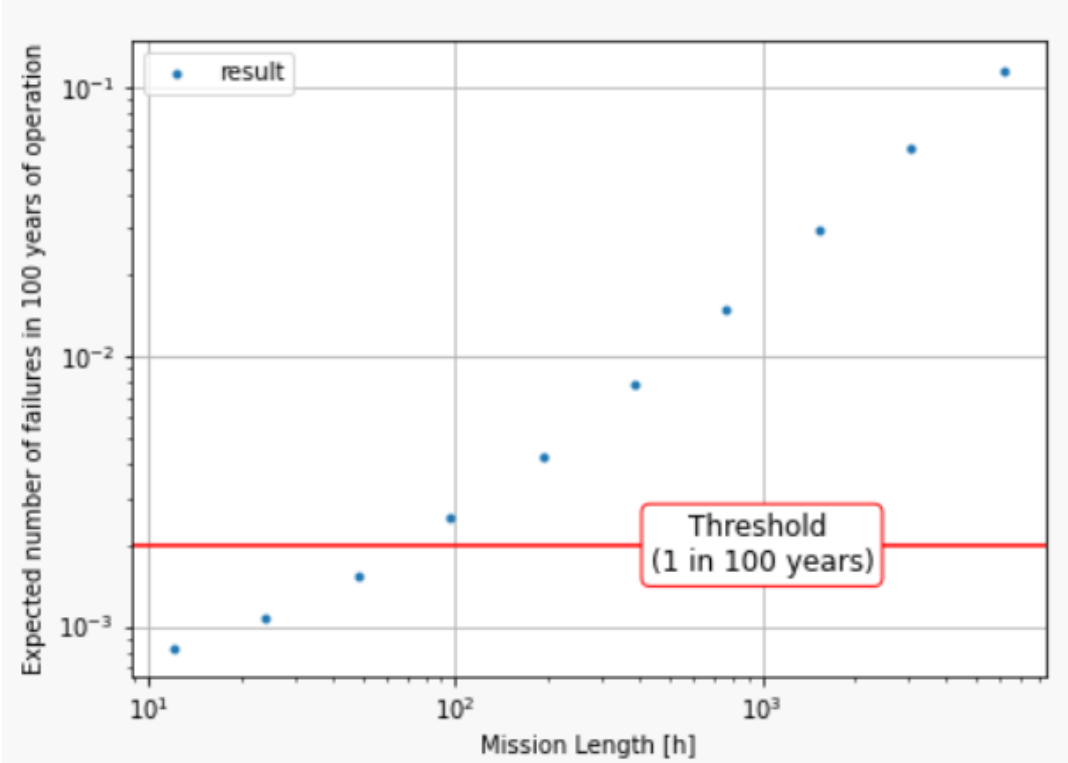
Bottom-up prediction
Preliminary simulations

Bottom-up prediction of the failure rate:

- Assumptions about system elements are written in the table.
- Critical path requirements model updated according to the discussions.
- **Every failure is considered critical** – which is clearly not the case.

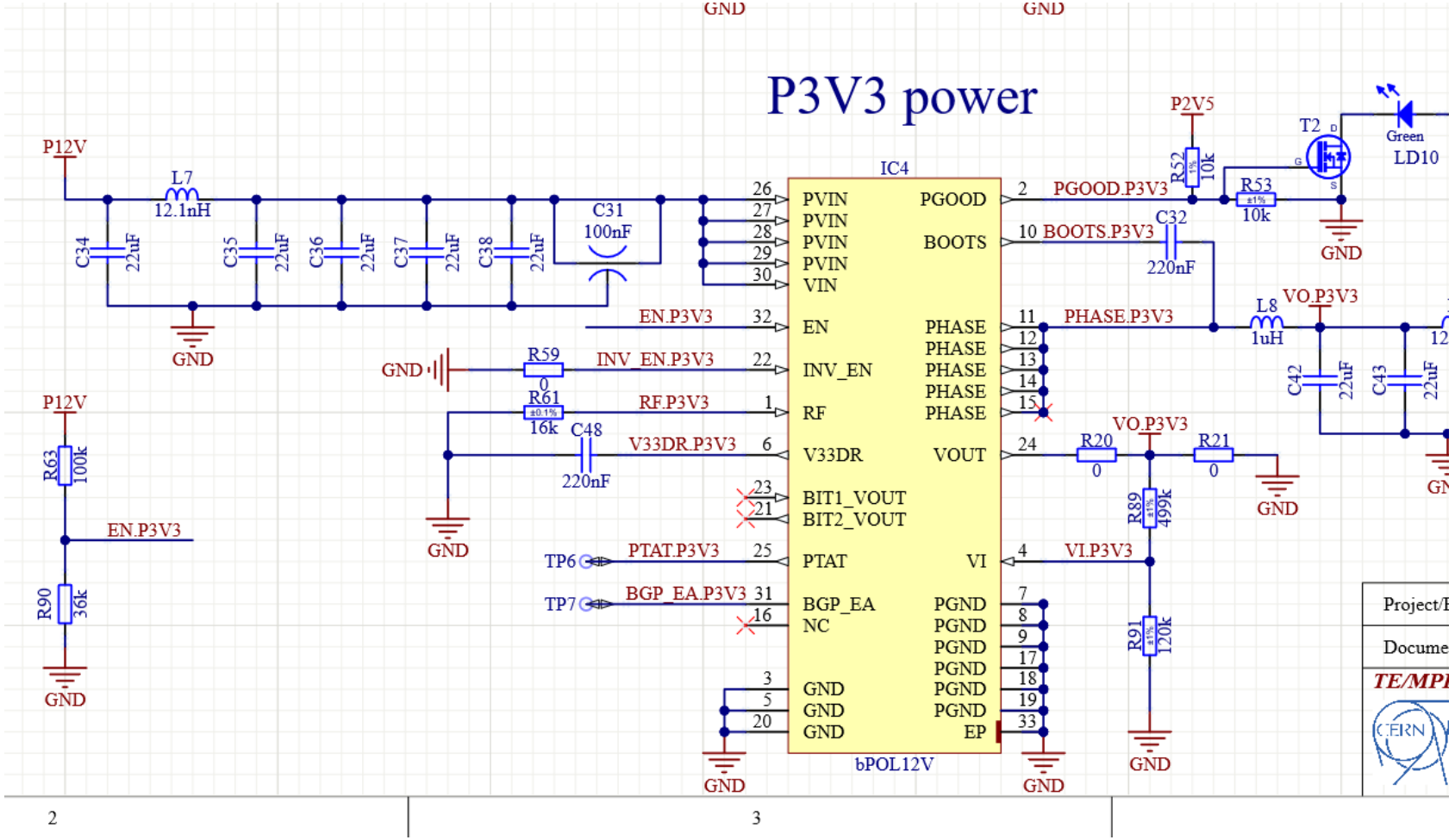
Simulations with these **overly pessimistic** assumptions lead **to not meeting** the targets, unless the EE systems would be checked **every few LHC fills**.





Parameter	Value [FIT/failures in 10^9 hours]	Source
CNTL	1000	Schematics
FPA	2500	Schematics
Driver	3000	Schematics
Switch/ Hardware	100	https://edms.cern.ch/document/2684812/12
Optocoupler	1	(read out of FPA loop)

CERN bPOL12V
Schematic excerpt



CERN bPOL12V
Reliability studies

bPOL12V_V6 datasheet: “Input voltage – Pvin, Vin: max 11V”

- datasheet link

In “The bPOL12V DCDC converter for HL-LHC trackers: towards production readiness” presentation by F. Faccio et al. (CERN – EP/ESE)

- “During long-term stresses, failures were observed starting from Vin=12-13V” *slide 16*,
- ”During long-term stresses, samples seem to run without failures at 12V - but we have 1 or 2 debatable exceptions with the V4” *slide 19*
- “De-rating the Vin is a wise idea: take as much margin as possible” *slide 19*
- presentation link

bPOL12V_V4 datasheet: “Power Input Voltage Pvin -0.3V to +10.0V, 11V max Pvin under reliability tests”

- datasheet link
- In another part, it says “10V recommended strongly”

In “The bPOL12V DCDC converter for HL-LHC trackers: towards production readiness” paper by F. Faccio et al. (CERN – EP/ESE):

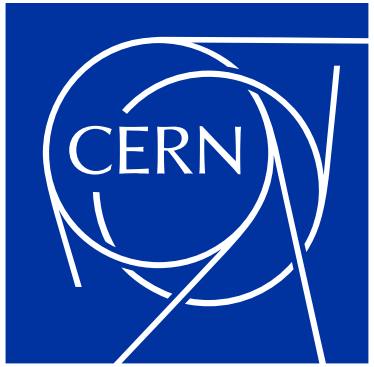
- “Based on the results of long-term stresses, it is strongly recommended to avoid using the converters at the maximum input voltage of 12 V. “
- “the input voltage is a fundamental parameter in determining the reliability of bPOL12V, therefore we strongly recommend in the application the use of the minimum Vin compatible with the requirements (...).”
- paper link

Tantalum capacitors
Derating

- **Derating is generally maintained at below 50% level**
  - I.e., ratio of operating voltage to rated voltage
  - Operating voltage is read from nets names (i.e.,)
- **In the Controls board, some tantalum capacitors have it at 60%: IC25, IC26.**
- **“Derating Of Surge Currents For Tantalum Capacitors” A. Teverovsky, link:**
  - “Typical derating requirements for solid tantalum capacitors limit the maximum applied voltage to 50% of the rated voltage (VR) and the inrush currents are bounded by additional resistors used in series with the capacitors.”
- **“Solid Tantalum Capcitors (With MnO2 Electrolyte) Voltage Derating” Vishay Intertechnology, Inc., link:**
  - Table p. 3: derating of 50% or more above 12V voltage rail.

Next steps

- **Failure rate estimation improvements:**
  - TVS diodes – operating or rated voltage assignment
  - Operating voltage for capacitors with the following nets: P_LDO, VCORE, P_JTAG, VBUS, VPUMP, SCANSTA_nRST and capacitors connected to nets with default names.
- **Obtaining the more realistic of the failure rate**
  - Classic end-effects analysis on the level of individual failure modes.
  - Alternatively, a page-level end-effect analysis.



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