Model Iteration

Energy Extraction Universal Controls #5

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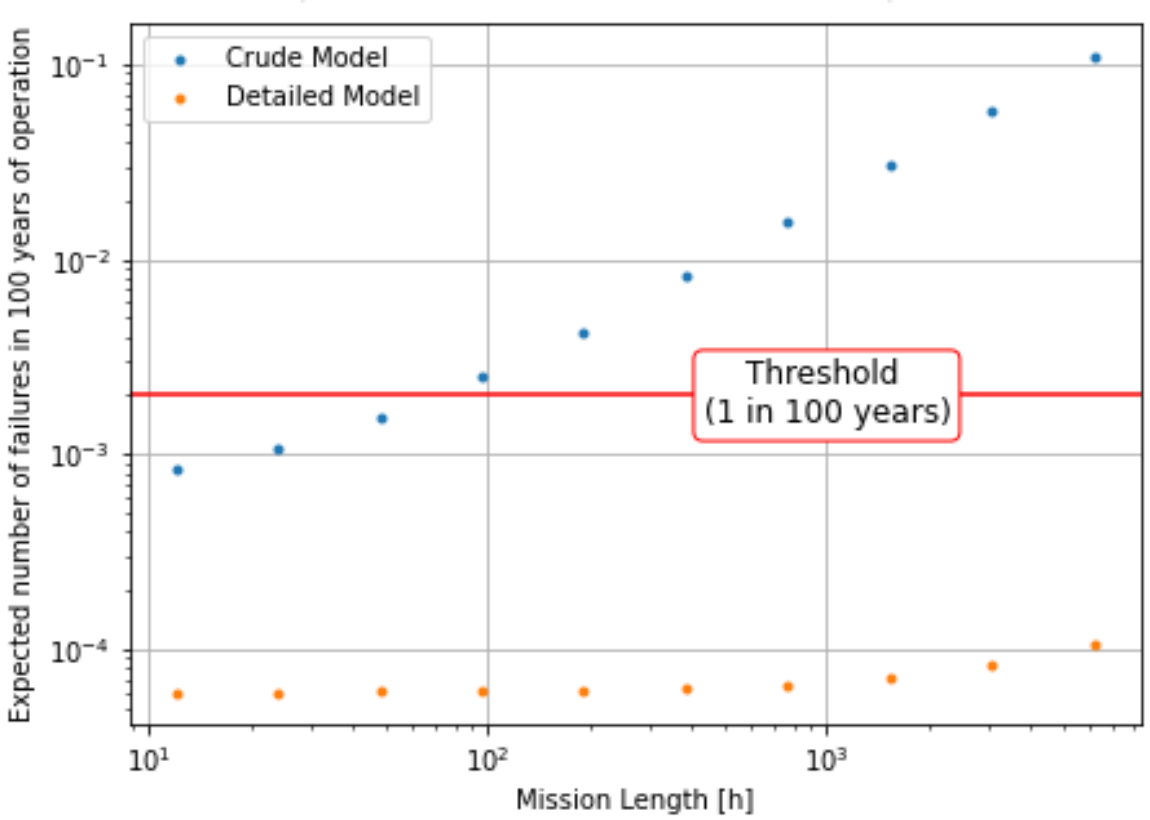
Results after changes
Refining blind failure model



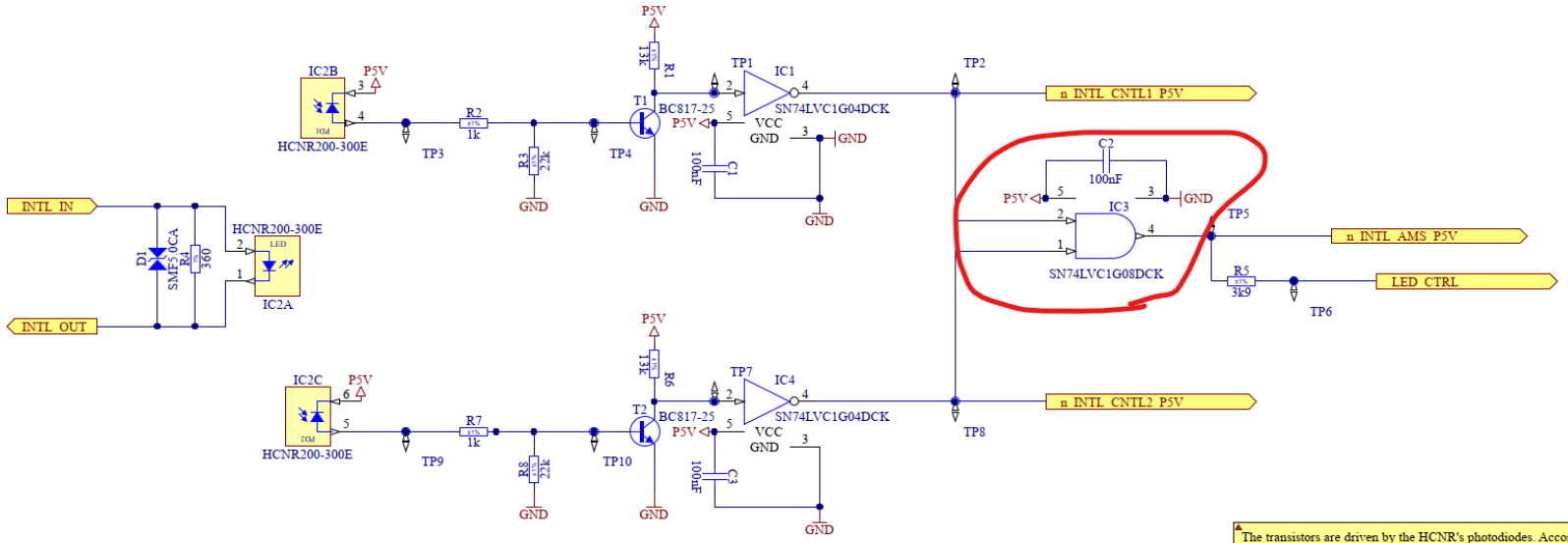
- Results for 1 year mission length:
  - Reliability for the **initial** FPA/SPA model
    - 2.03e-05 failures per year
  - **After removing P3 connector**
    - No blind failure possible at FPA loop connector)
    - 8.29e-06 failures per year
  - After **restricting** IC22's failure modes to **stuck high:**
    - only stuck high leads to blind failure on path A and B
    - 9e-07 failures per year.

Can satisfy requirements, but component remains singular point of failure on critical path.

Details of critical components
IC22 Stuck High

- **8-Bit Dual-Supply Bus Transceiver With Configurable Voltage Translation and 3-State Outputs**
  - Texas Instruments
  - Failure rate: 0.5 FITS (at 60% CI; around 1 FIT at 90%).
- **FMD-2016 on IC: Integrated Circuit, Digital, Transceiver, Bus**
  - Vendor Defect 28.6%, Bent 14%, Induced Failure 14%, Short 14%, Slipping 14%, Functional Failure 7%, Parametric Failure 7%
  - ”Stuck high” - mentioned in the “Induced Failure” from a proprietary source.
- **FMD-91 on Microcircuit, Digital, MOS:**
  - Output Stuck High: 8%
- **Other sources: suggestions of 10-15% referring to “common failure modes for ICs”.**

Interlock card
Potential single point of failure?



INTL Current Loop	n_INTL_CNTL1_P5V	n_INTL_CNTL2_P5V	n_INTL_AMS_P5V	LED Light
1	1	1	1	OFF
0	0	0	0	ON

Remark : Attention must be payed whether the connected interlock signal is active high or active low.

The transistors are driven by the HCNR's photodiodes. According to the datasheet, 0.25 % < Current Transfer Ratio (CTR) < 0.75 %. To account for any decrease due to TID, the minimum CTR will be set at 0.2 %.

The FPA loop current will be from 5 mA to 50 mA. Because there are two HCNRs in parallel, the current will be divided between them approximately 50:50.

Ibase_min = Iled_min * CTR_min = 2.5E-3 * 2E-3 = 5 uA
Ibase_max = Iled_max * CTR_max = 25E-3 * 7.5E-3 = 188 uA

According to the BC817-25 datasheet, 160 < Hfe < 400. To account for any decrease due to TID, the minimum Hfe will be set at 80.

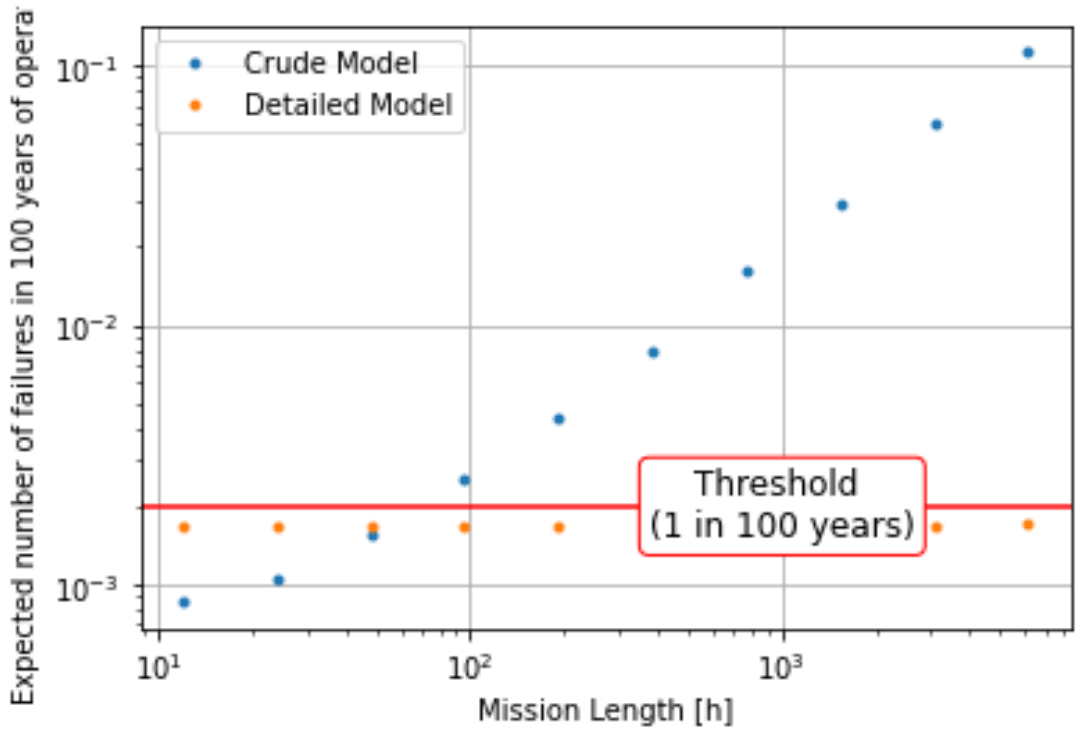
Icollector_min = Ibase_min * Hfe_min = 5E-6 * 80 = 0.4 mA
Icollector_max = Ibase_max * Hfe_max = 188 uA * 400 = 75.2 mA

Minimum pull-up resistor value to drop 5V:

Rpull-up_min = 5 / Icollector_min = 5 / 0.4E-3 = 12.5 kOhm

Interlock card
Schematics

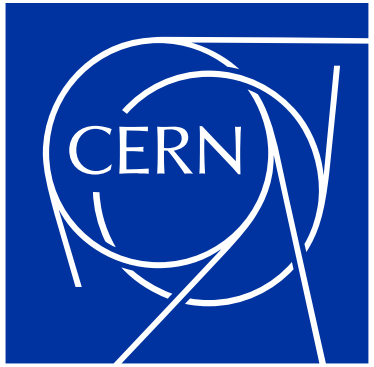
Model with the interlock



- **Results show high number of failures**
  - Lots of components in the non-redundant part
- **Simulation with only 1 interlock (while there are 15)**

Details of critical components
IC8 Input Stuck High

- **Single 2-Input AND Gate**
  - Texas Instruments
  - Failure rate: 0.5 FITS (at 60% CI; probably around 1 FIT at 90%, can be checked).
- **No info in FMD-2016 about inputs stuck (neither high nor low).**



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