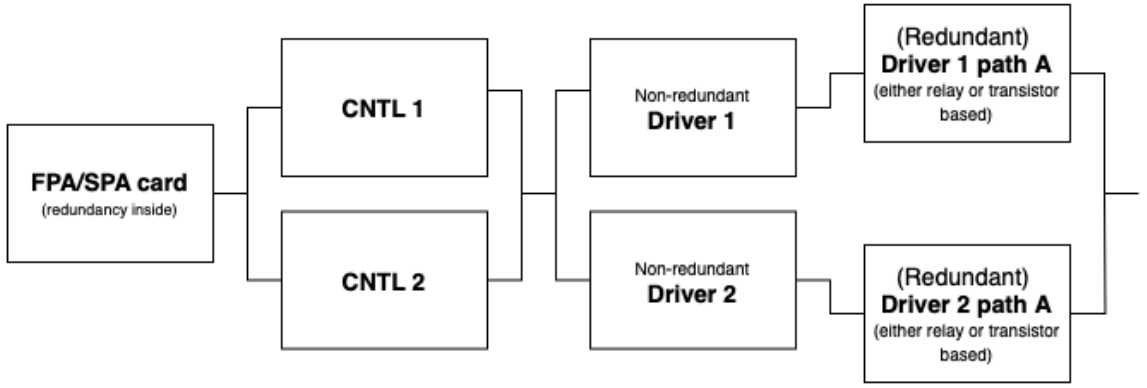
Models for FPA/SPA and Interlocks

Energy Extraction Universal Controls #6

Model with the FSPA card
Description



FSPA card has internal redundancy leading to complete crossing of the output signals inside:

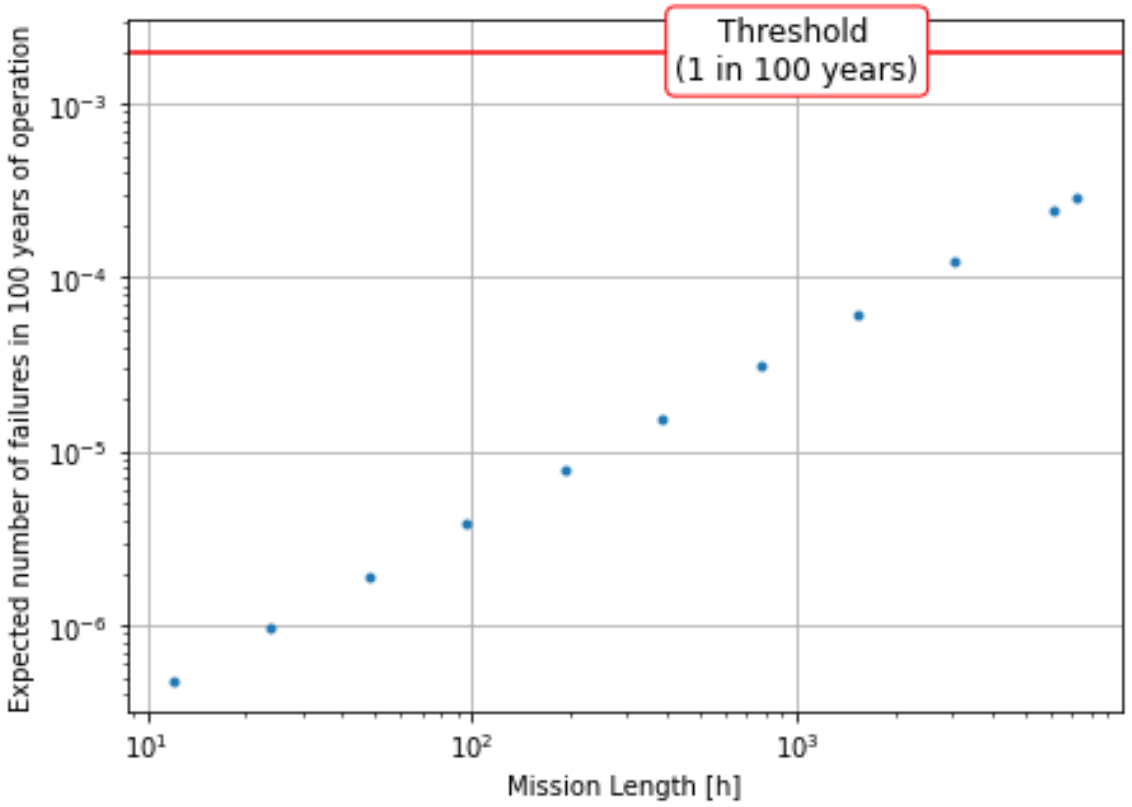
- Signals **ST LOOP A 1** and **ST LOOP A 2** going to **CNTL 1**
- Signals **ST LOOP A 1R** and **ST LOOP A 2R** going to **CNTL 2**

Control boards inputs are coming from two redundant paths of the **FSPA card**; outputs are provided to two **driver cards**.

The **driver cards** have a redundant and non-reduntant paths.

Given the model, we pessimistically assume that there is just one path (i.e., as if the card was non-redundant).

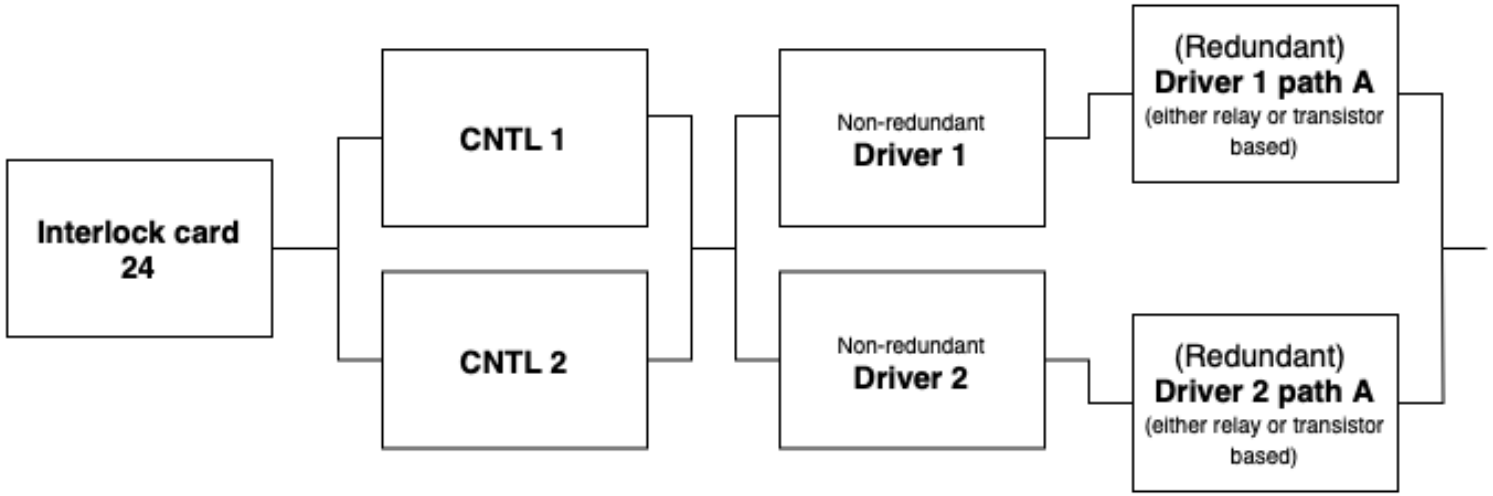
Model with the FSPA card
Results



Assumptions:

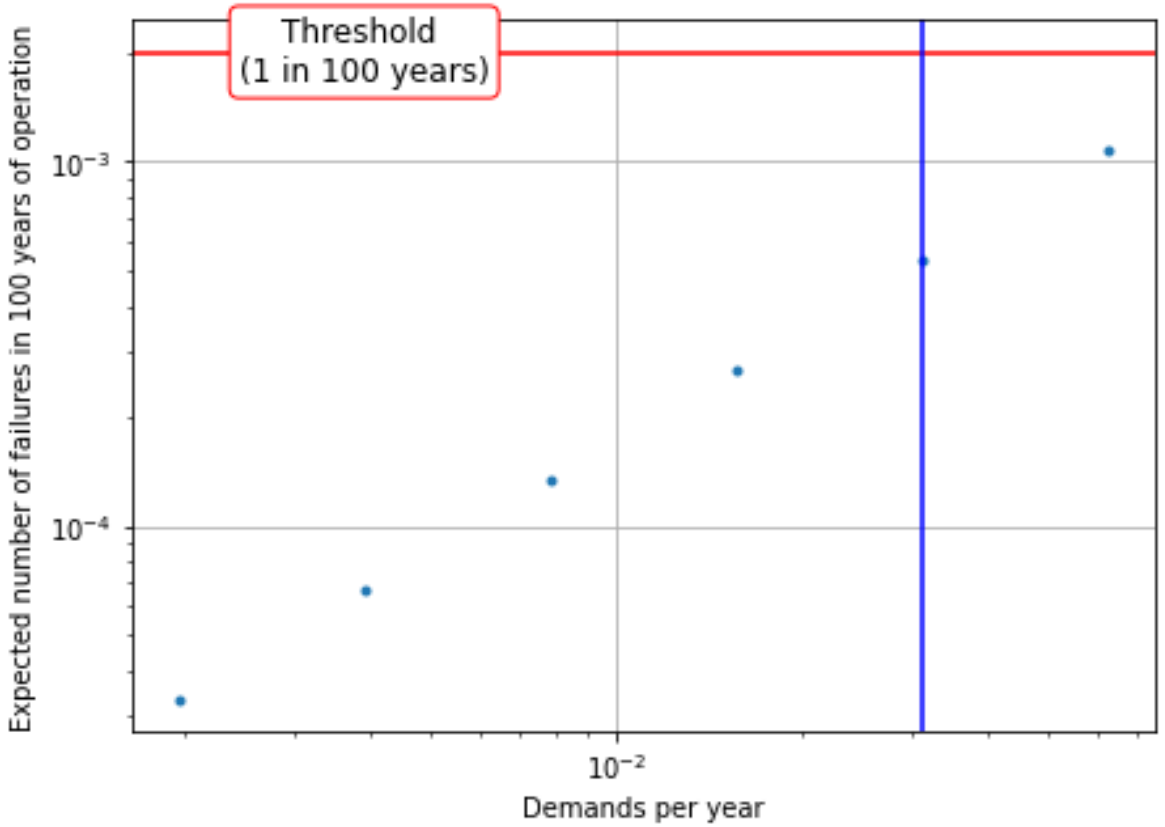
- One FSPA card per system
- Simplified models for calculations:
  - driver model with just 1oo2 redundant path
  - FSPA card without additional internal redundancies
- **→ with yearly testing & two fully redundant paths for switch opening, the reliability requirements are met**

Model with interlocks
Description



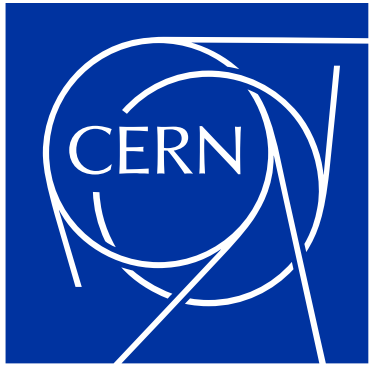
X 24

Model with interlocks
Results



Assumptions:

- Between 600A and 13kA case, 13kA considered more critical
  - Taken as baseline and results scaled to all EE systems
  - Demand parameter scan (blue line is one demand per 32 systems per year)
  - 24 critical interlocks assumed
  - Test every three years
- → with yearly tests, and critical interlock rates <= 1 per 32 EE systems, the reliability requirements are met
  - Further gains possible if possible single points of failure in interlock card mitigated (last meeting)
  - Yearly testing of interlocks



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