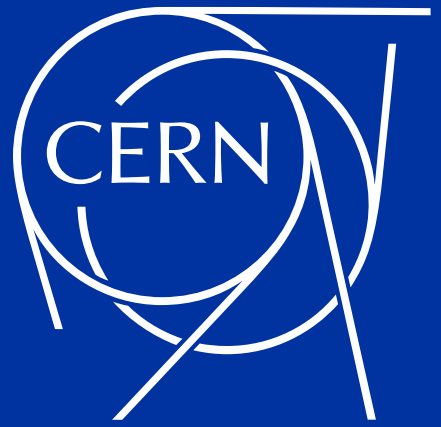

Update on SoC activities in the CERN AT Sector

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08/03/2023

Outline

- **Introduction**
- **Inventory of SoC Applications in ATS**
- **Summary of the SoC taskforce recommendation**
- **Outlook**

AT Sector and CTTB

ATS: Accelerators and Technology sector at CERN

- Beam (BE) → Controls groups (CEM & CSS): central services and support
- Engineering (EN)
- Accelerator Systems (SY)
- Technology (TE)

Big variety of electronics and software systems integrated in the same accelerator control infrastructure

CTTB: Common Hardware & Software Technologies Technical Board (2021, indico)

- Analyses common hardware & software activities to **avoid duplication of work or services**
- Stimulates a common approach & **strengthens standardisation effort** of hardware & software solutions

→ SoC technology identified as target for fruitful standardization

Taskforce for SoC Framework (from 31st CTTB)

- **Goal**
  - Starting from the current SoC applications in ATS and future needs identify a generic architecture, common services and a proper integration in the accelerator control system to converge towards a common SoC framework
- **Scope**
  - All the ATS SoC applications and users in radiation free environment
- **Timeline**
  - Intermediate reporting at 34th CTTB (24/11/2023)
  - Final reporting at CTTB January/February 2024 (23/02/2024)

Taskforce for SoC Framework (from 31st CTTB)

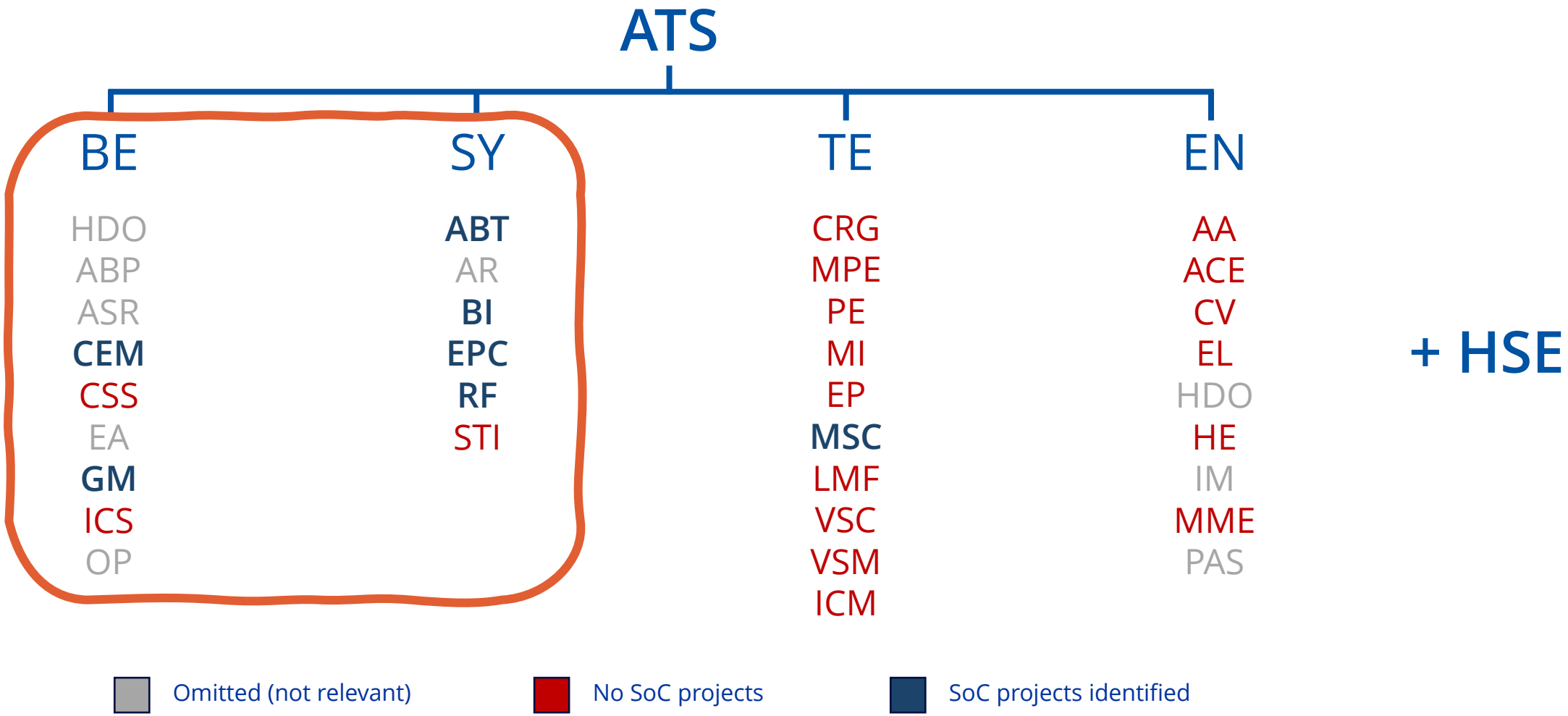
- **Deliverables**

1. Inventory of the existing SoC applications and future (LS3) needs within ATS
2. Identification of commonalities and their potential to converge to a common solution:
    - SoC family/families standardisation
    - SoC architecture and reference design (i.e. PS/PL generic gateware interfaces)
    - Common services (i.e. Diagnostics / monitoring / configuration services, safe booting, RT environment for user defined tasks)
    - Embedded Linux support
    - Proper integration in the accelerator control system:
        - FEC like support vs FEC-PS additional communication layer
        - Availability of special services (i.e. Post-mortem, timing)
    - High bandwidth data link
    - Standardised workflows
    - Generic framework to easy the programming and exploitation of the SoC architecture
3. Strategy and roadmap towards a common and unified solution with identification of domains for collaboration
4. Estimation of resources, timeline, risk and return on investment for the proposed strategy

Inventory of SoC Applications in ATS

Commented summary of the survey results

Inventory


ATS
BE
HDO
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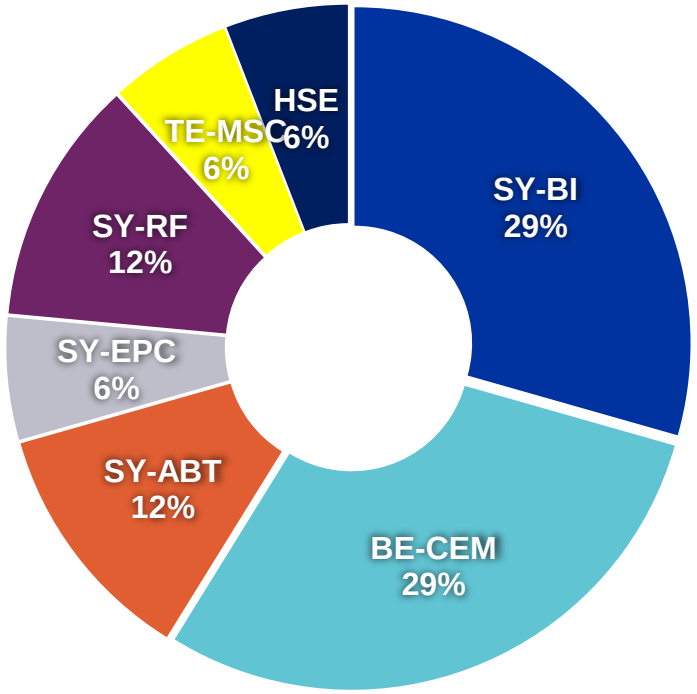
MSC
LMF
VSC
VSM
ICM
EN
AA
ACE
CV
EL
HDO
HE
IM
MME
PAS
+ HSE
Omitted (not relevant)
No SoC projects
SoC projects identified

Inventory

#	Group	Project	Survey
1	SY-ABT	DKFC	Yes
2	SY-ABT	FIDS	Yes
3	SY-BI	HL-LHC BPM / AWAKE	Yes
4	SY-BI	LHC BPM Cons	Yes
5	SY-BI	BIPXL Readout	Yes
6	SY-BI	MIM	Comments[1]
7	SY-BI	MCOI	Yes
8	SY-EPC	FGC4	Yes
9	SY-RF	- (FBM section)	Comments [2]
10	SY-RF	SPS RF Beam Control	Yes
11	BE-CEM	FSI	Yes
12	BE-CEM	Sambuca	Yes
13	BE-CEM	Sambuca Motor Driver	Yes
14	BE-CEM	White Rabbit WREN	Yes
15	BE-CEM	White Rabbit WRS	Yes
16	TE-MSC	New MSC platform	Yes
17	HSE	CROME	Yes

17 SoC projects

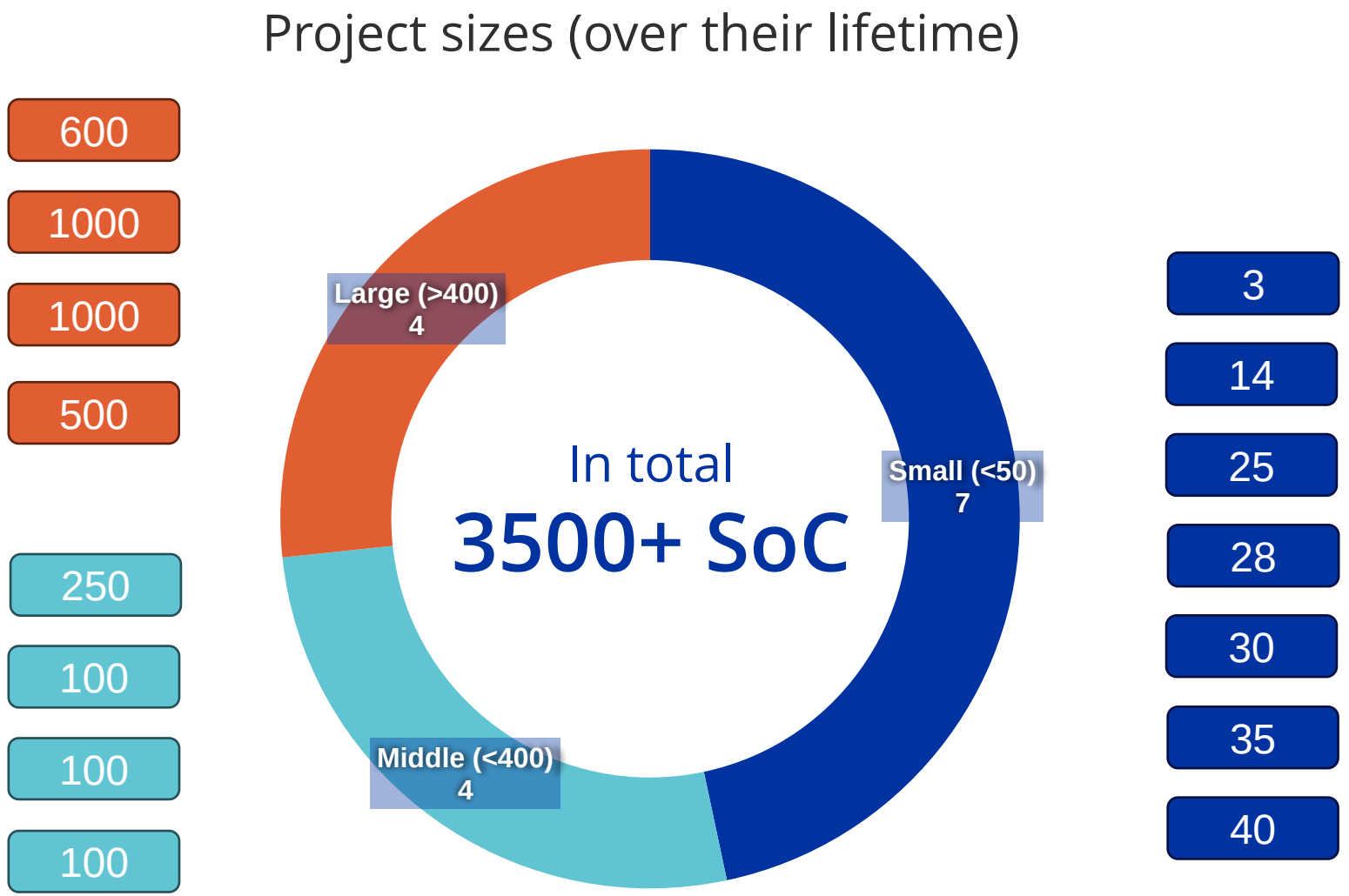
15 surveys were received



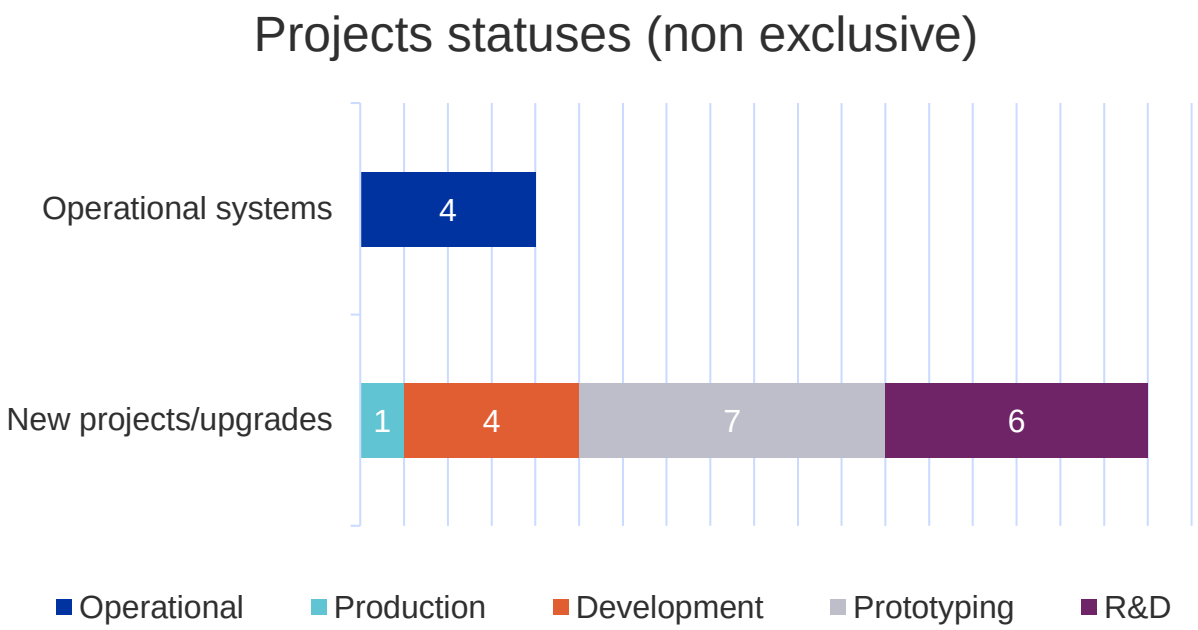
Notes:

[1] Legacy system with two units.
[2] Will use AMD Zynq UltraScale+ RFSoC and uTCA architecture.

Estimated number of SoC



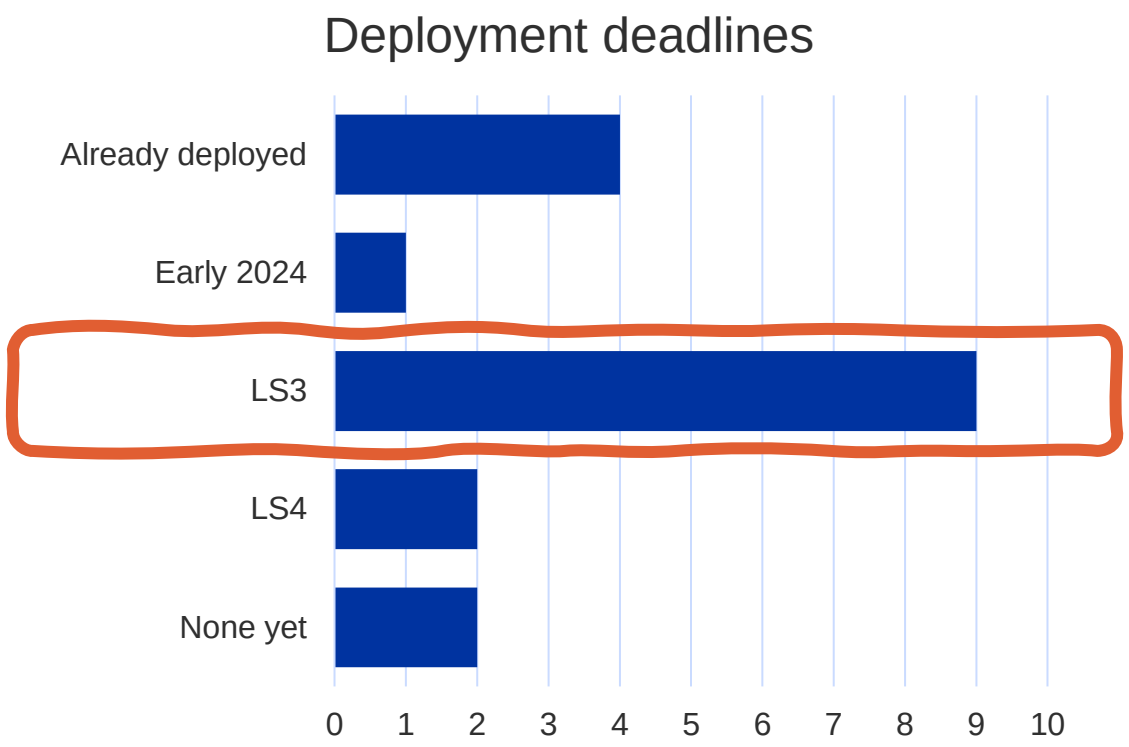
Status and deadlines



- **Already 4 operational systems are using SoCs**
- **Majority of SoC activities regard new projects and upgrades**

- ***High adoption potential of a common SoC framework for projects in R&D and prototyping stage***
- ***Some tools potentially useful for advanced projects as well***

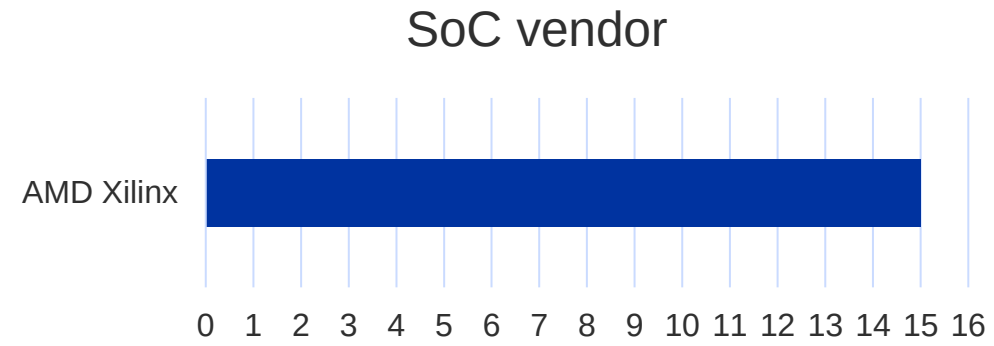
Status and deadlines

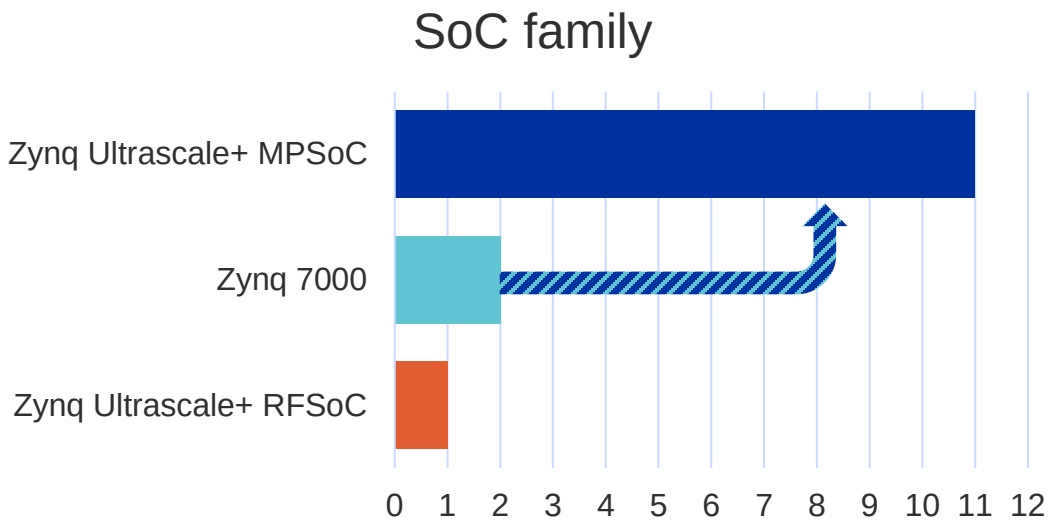


Most projects target LS3 for deployment

LS3 confirmed as time horizon for the ATS SoC Common framework

SoC vendor and family





All projects on AMD Xilinx SoCs

Most of projects using US+ MPSoC (or planning to)

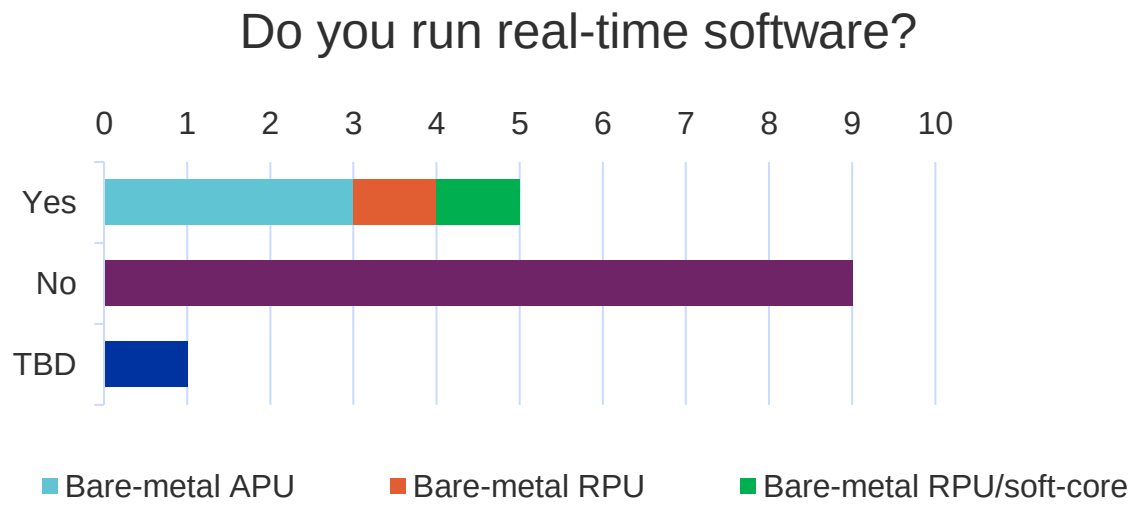
1-2 RFSoC projects, SoC with same Processing System cores as US+ MPSoC
(identical from the software stack point of view)

Xilinx Zynq US+ family candidate for common framework support

Software and Operating System

Some real-time software:

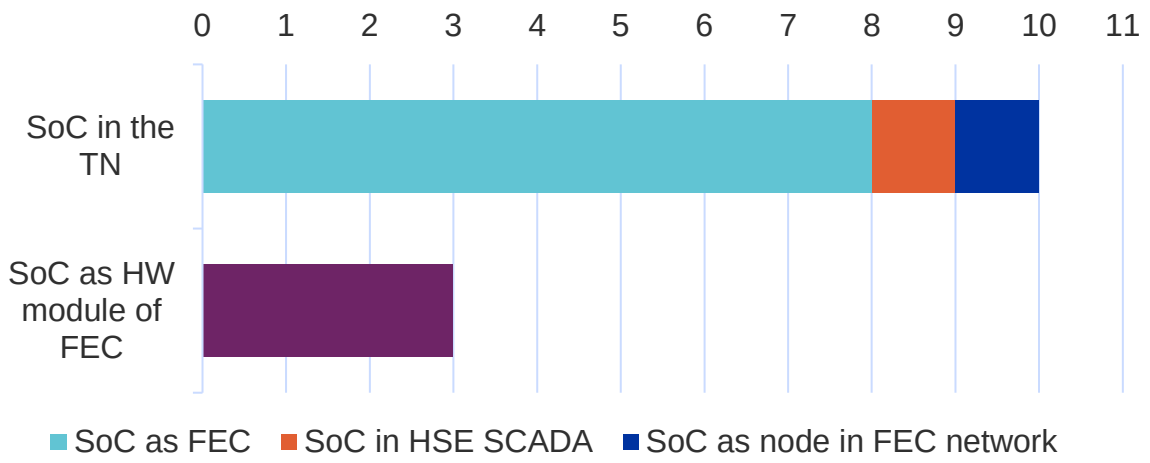
- All bare-metal code (no RT OS)



Operating System for Application Processing Unit:

- All projects using an OS in their APU interested in adopting **FEC-OS**
  - FEC-OS on SoC: same distribution as for new FEC model
  - All new projects have the same Processing System (ARM Cortex-A53 core based)
  - *Potential alignment between SoC Common framework and new FEC model*

Integration with accelerator control system



SoC as HW modules (no OS):

- Integration through FEC
- SPEXI7U model, RF uTCA systems

FEC-OS → FEC-like services libraries potentially available to SoCs if required

- Configuration, databases, layout
- FESA, or other FEC SW frameworks
- Drivers (EDGE)
- System monitoring and diagnostics
- Network booting with fall-back strategy
- CMW/RDA
- Post-mortem
- Remote console and tools
- General Machine Timing

Programmable Logic

Bus: Large use of AXI and Wishbone

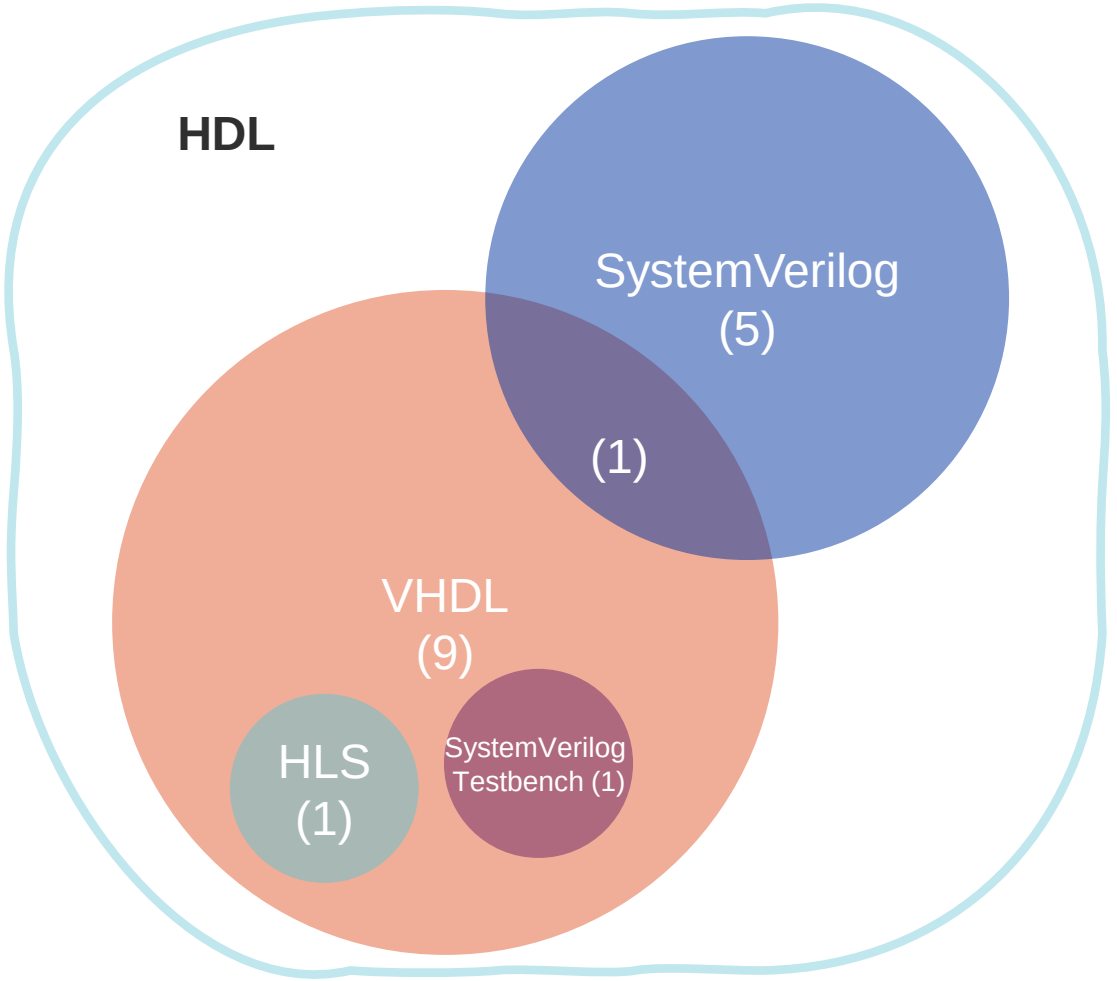
IP integration: combination of TCL scripting and graphical block design for most

DMA: mainly application specific use

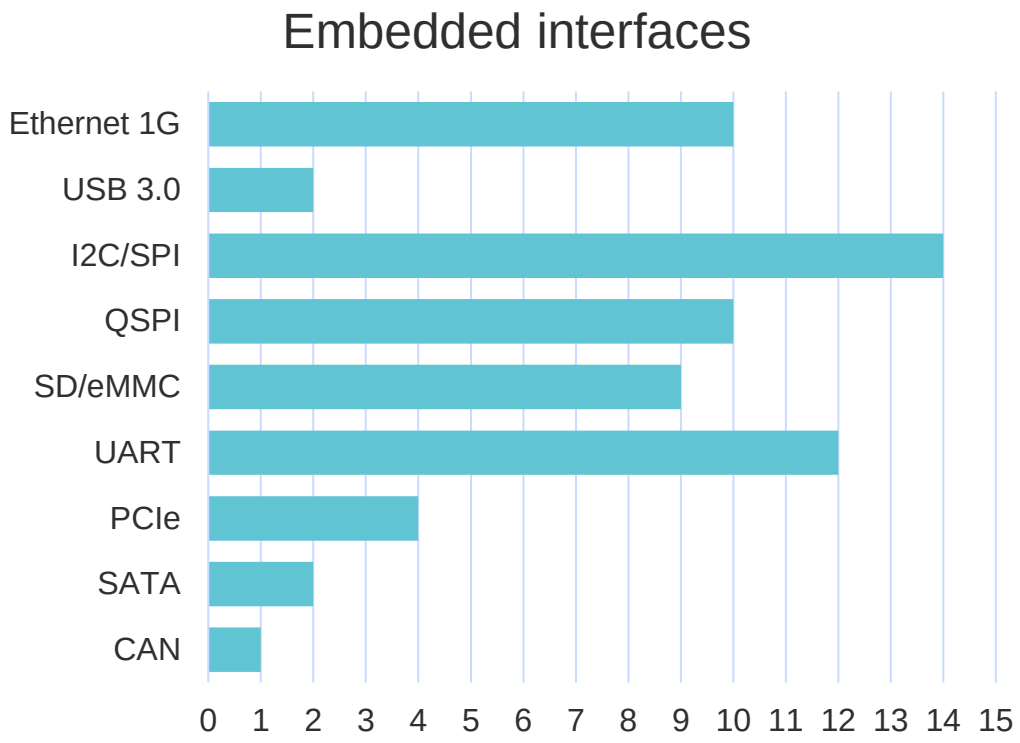
- PS DDR memory – Linux driver
- PL-controlled DMA to inject data in PS DDR

Others:

- Common gw-sw co-simulation framework
- CI support
- Cheby with EDGE compatibility
- Partial reconfiguration



Interfaces



High-bandwidth data read-out 10G ETH:

- 2 use cases, but interesting for common framework

Data acquisition protocol: GBTx/LpGBT

SoC to SoC/FPGA: few cases, Aurora protocol

Slow control FEC → SoC over 1G Ethernet:

- Fewer use cases if SoC as FEC
- SILECS
- ROMULUSlib
- REST
- IPbus
- Custom protocol over Ethernet

Hardware platforms

General interest for common hardware solutions

- Few projects designing custom SoC PCBs (WR, FIDS, Sambuca)
- Several projects in the eco-system of **DI/OT**
- Large interest into generic-purpose System-on-Module (**SoM**) with application specific carriers

Hardware standardization facilitates framework standardization

Opportunities for shared procurement and step-pricing

Summary of the recommendation

Extract from the taskforce report to 37th CTTB

Hardware

- ***Vendor:* AMD Xilinx**
  - supported development tools and environment, community
- ***SoC Family:* Zynq UltraScale+**
  - support for the full software stack, under fulfilling of HW requirements (WIP: e.g. Ethernet PHY, DDR memories, remote console tools)
- ***SoC model:* Zynq UltraScale+ XCZU17EG-1FFVC1760E (WR and DI/OT)**
  - access to advantageous step-pricing, compatibility with reference design
- ***Reference PCB design:* DI/OT System board v3**
  - schematic sheets of main blocks, Board Support Package and reference framework project

Low-level Software

- ***Operating System (OS):*** **Linux-Xilinx kernel, Debian (FEC-OS)**
  - OS support, basis for tools and services as FECs
  - Kernel and device-tree support model under discussion
- ***Booting:***
  - *Bootloader:* U-Boot + GRUB (FEC-OS)
  - *Source:* Network booting with fall-back source in FLASH, fail-over mechanism WIP
- ***Hypervisors:*** **OpenAMP (Xilinx support), Bmboot (CERN-EPC tool)**
- ***Real-time code:*** **baremetal (R5 if possible) and programmable logic**
  - No support for OS RT-patches

High-level Software

- ***External monitoring:*** **FEC-like tools (WIP)**
  - access to system metrics from central service/server identical to FECs
- ***Internal monitoring:*** **DI/OT library**
  - access to platform metrics from the SoC applications in Linux
  - Configurable and extendible version under discussion
- ***Time synchronization:*** **NTP (ms, default)**
  - If more precision required: PTP (us), WR (ns)
- ***Software framework:*** **FESA**
  - supported software framework and integration in control system, BUT SoC solution for timing and no RT

Common software blocks and strategies

- ***Monitoring library interface:* DI/OT utils**
  - Command line interface to the DI/OT monitoring library (reading local monitoring values, reading configuration, executing power-cycle command)
  - Generalization to other SoC platform depends on hardware and additional resources
- ***Software, firmware and bitstream distribution:* Debian packages**
  - Distribution and version management of the software tools, firmware and FPGA bitstreams
  - In-line with the phase 2 of the FEC-OS project
  - Will require establishing a central repository for Debian packages
  - Alternative and only solution for FESA: NFS

Common gateware blocks and strategies

- **Push toward sharing and reusability of gateware modules:**
  - Collection of pointers to repositories in SoC applications inventory
  - Shared IP repository: starting from CEM-EPC shared repo, following Electronics Forum initiative
  - AXI4 bus and Wishbone bus as light alternative
  - Reference project + Board Support Packages for DI/OT v3 based reference schematics
- **Common interest in-house HDL modules under investigation:**
  - High bandwidth data transfer module to DDR Memory controller, controlled by PL
  - CMS TCP/IP Fast data link over 10Gb Ethernet, available only inside CERN
- **Development tools:**
  - Cheby for memory map generation and EDGE tools integration
  - Continuous Integration guidelines and infrastructure (following Electronics Forum initiative)
  - Guidelines on sw-gw co-simulation based on QEMU and Questa and CROME framework

CERN Control System Integration

- ***Communication:*** **CMW/RDA**
  - Standard for FEC communication and natively supported in FESA
  - Integration with upper layers of CERN control system without introducing new protocols
- ***Timing events distribution:*** **through CMW/RDA**
  - Light SW timing event distribution implementation, cheaper alternative to timing receiver
- ***Configuration storage:*** **CCS (DB + API + UI Editor)**
- ***Monitoring server:*** **COSMOS**
- ***Start-up services:*** **LUMENS**

Outlook

Open-points and outlook of future activities

Open points

FEC-OS:

- It is the fundamental basis, still open discussion on support model to define feasibility
- Proposal: single standard kernel and device tree supported by sysadmin, with project specific overlays under responsibility of the projects
  - Device-tree and overlay mechanism to be tested
  - Remote console tools to be identified
  - Drafting list of HW requirements for standardized kernel
- WARNING: SoC with OS in TN comes with risk of forced update of the gateware development environment when forced to apply certain security patches
- Alternative (and only solution for not UltraScale+): kernel maintained by the SoC team
  - Zynq 7000 legacy systems example: collaboration for single kernel and build tools adaptation, shared resource between ABT, HSE and sysadmin

Open points

FESA on SoC:

- First tests are ongoing
  - New timing class to be developed
  - No Real-time patches in theory OK, to be tested
- Early-access to equipment groups for tests in Q4 2024

Reference design platform:

- IP Repository setting up, in the frame of Electronics Forum initiative
- DI/OT utils generalization and extension (depending on new SoC HW)
- Co-simulation GW-SW environment, possible collaboration with HSE

Challenging support model: cross-departments, need of a coordination and support body

Summary

Two feasible ways of using SoCs in the sector:

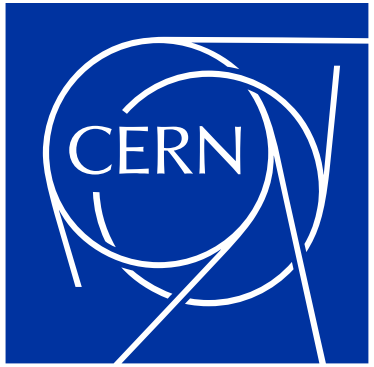
- As FEC hardware accelerator: part of a crate, OS discouraged
- As integrated system with FEC-like capability: FEC-like software stack is recommended

FEC-like support for SoCs seems a feasible but tight target for LS3 systems

Formalization of the recommendation as document to be approved by the stakeholders

Fundamental for sustainability on the long term:

- Kernel and SoC knowledge retention/acquisition
- Hardware standardization
- Code sharing
- System diagnostics improvement
- Coordination



Contact us: ats-soc-taskforce@cern.ch
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