Contribution ID: **4** Type: **not specified**

Best practices to open-source FPGA designs

Tuesday 11 June 2024 14:40 (30 minutes)

Open Source revolutionised software development by promoting collaboration, innovation, and openness. As FPGA designers, you can leverage this approach and share your HDL designs with the world.
In this presentation, we will discuss a step-by-step process to help you open-source your HDL designs effectively. We will begin by addressing the key question of where to host your HDL. We will then provide guidance on selecting an appropriate licence. Essential elements to ensure a smooth collaboration experience include setting up version control, issue management, documentation, verification and testing procedures. After a brief description of these best practices, we will show how adopting them can encourage contributions, and help maintain high quality in your project. Lastly, we will examine the role of your employer in open-sourcing FPGA designs, using CERN as an example and describing how its newly-established Open Source Program Office (OSPO) can help in this process.

Talk's Q&A

During the talk

Talk duration

20'+10'

Will you be able to present in person?

Yes

Primary author: SERRANO, Javier (CERN)

Presenter: SERRANO, Javier (CERN)

Session Classification: Introduction

Track Classification: HDL verification and simulation tools