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Fast Monitoring of FPGA algorithms using SpyBuffers

Tuesday, 11 June 2024 17:20 (30 minutes)

The development, testing and operation of FPGA algorithms require the implementation of flexible and efficient real-time monitoring. This can be achieved via the insertion of dedicated buffers between the logical blocks of the FPGA firmware. These buffers are implemented in the firmware to spy the dataflow between the internal blocks (Spybuffers). They must provide configurable size and are equipped with a playback feature that allows to inject simulated data into the firmware path. A dedicated control software sets the Spybuffer mode (monitoring or playback), performs memory readout and analyses the results. In this talk we discuss the SpyBuffer design for monitoring and playback operations, the interface of the SpyBuffer with the AXI Chip to Chip interface, as well as the software layer to control the SpyBuffers and their operating modes.
1

Talk's Q&A

During the talk

Talk duration

20'+10'

Will you be able to present in person?

Yes

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