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Convenient and reliable clock domain crossings, using scoped constraints and reusable blocks

Tuesday 11 June 2024 15:40 (40 minutes)

Despite being used regularly by all FPGA designers, very few people know how to properly and reliably constrain a clock domain crossing (CDC). Timing constraints are indeed one of the hardest parts of FPGA design. It is an elusive art that is impossible to google and impossible to verify.

In this session we will discuss a few common CDC topologies. Analyze them, discuss some common mistakes, and discover their error modes. Most importantly, we will discuss how to make them robust using timing constraints. We will also discuss how scoped constraint files enable reusable CDC blocks, so the user never has to write a single line of TCL/XDC.

We will introduce the library of generic and reusable CDC blocks available in the open-source hdl-modules project. Peer-reviewed, proven in use, and constructed after thorough discussion and analysis, to give as reliable operation as possible.

Talk's Q&A

During the talk

Talk duration

20'+10'

Will you be able to present in person?

Yes

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Session Classification: Sharable HDL Cores

Track Classification: Sharable HDL cores