Contribution ID: **58** Type: **not specified**

Fine-grained hierarchical placement constraining for timing closure (and more)

Wednesday 12 June 2024 09:00 (25 minutes)

Timing closure is possibly the most challenging task in the FPGA algorithms design, with the placer quickly becoming the limiting factor at higher frequencies. AMD encourages to do hierarchical placement and turn to gate-level placement as a last resort. I would like to discuss a methodology to do fine-grained hierarchical placement, based on python generation of constraint files, and that allows replicating the layout in different areas of the FPGA. The script takes into account the target FPGA architecture and the resource utilization of each design block, and allows the user to easily place the design to optimize the data flow, with arbitrarily fine-grained detail on the challenging paths, putting focus on design maintainability.

Other solutions to common development problems will be presented, such as a methodology to implement record-to-vector and vector-to-record converters for data storage in RAM, and a means to help with the arbitration of data delivery between related clocks.

Talk's Q&A

During the talk

Talk duration

15'+7'

Will you be able to present in person?

Yes

Author: NAVARRO TOBAR, Alvaro (CIEMAT - Centro de Investigaciones Energéticas Medioambientales y Tec. (ES))

Presenter: NAVARRO TOBAR, Alvaro (CIEMAT - Centro de Investigaciones Energéticas Medioambientales y Tec. (ES))

Session Classification: Solutions to everyday digital design problems

Track Classification: Solutions to everyday digital design problems