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From C to Routed Circuits for FPGAs in Seconds

Wednesday 12 June 2024 09:25 (20 minutes)

Advancements in design automation technologies, such as high-level synthesis (HLS), have raised the input abstraction level and made the design entry process for FPGAs more friendly to software programmers.
In contrast, the backend compilation process for implementing designs on FPGAs is considerably more lengthy compared to software compilation.
While software code compilation may take just a few seconds, FPGA compilation times can often span from several minutes to hours due to the complexity of the underlying toolchain and the ever-growing device capacity.
In this presentation, we provide an overview of the current advancements in fast compilation techniques for FPGAs.
Furthermore, We present a very fast compilation methodology that generates in a matter of seconds placed-and-routed kernel designs for AMD FPGAs.
This approach accelerates the C-to-FPGA implementation process by up to 33x with only 0.9x of degradation in Fmax compared to a conventional implementation flow.

Talk's Q&A

End of talk

Talk duration

15'+7'

Will you be able to present in person?

Yes

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