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Method for achieving phase determinism in the transmission side of AMD transceivers

Wednesday 12 June 2024 09:45 (25 minutes)

Phase determinism in timing distribution systems is often a requirement in detectors for High Energy Physics. Because of the new goals of high-luminosity, the rate of particle collisions is increasing. To distinguish almost superposed collisions it is required a very accurate timing signal, in the order of a few picoseconds. Commercial components do not met by default this stringent requirement. However, it is possible to find solutions for a cutting-edge phase determinism. This presentation is focussed on the transmitter of the AMD transceiver. Since the transmission is not frame aligned to its reference clock, at each startup the data stream has a random phase delay. The proposed solution consists in configuring a particular clocking architecture in the transceiver IP Core, allowing for monitoring the phase of interest and for implementing a correction, all within the FPGA. The result is a data stream with a fixed phase relation its reference clock, with picosecond-grade precision.

Talk's Q&A

End of talk

Talk duration

20'+10'

Will you be able to present in person?

Yes

Author: ORZES, Edoardo

Presenter: ORZES, Edoardo

Session Classification: Solutions to everyday digital design problems

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