Prospects of RFSoC technology in astroparticle physics experiments

Alexander (Sasha) Novikov

Bartol Research Institute, University of Delaware.
novikov@udel.edu

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FDF

Dela... where?

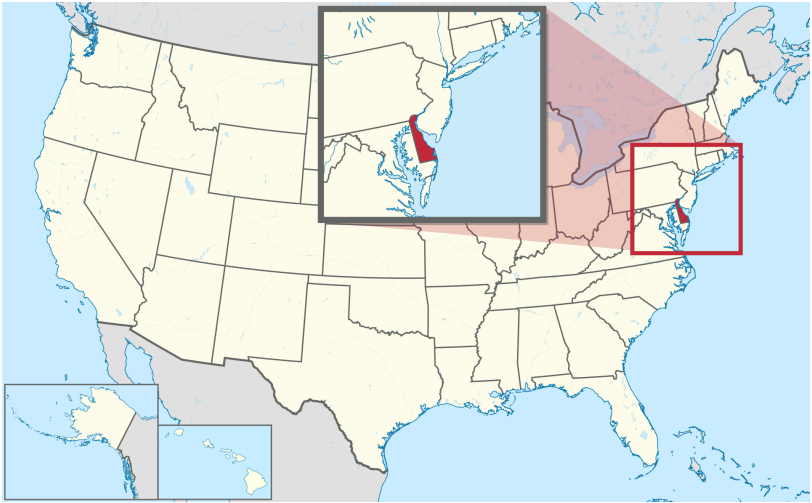


image from wikipedia

Outline

Motivation

Various astroparticle experiments (e.g. IceCube (gen2), PUEO, RNO-G, and others) especially (but not limited to) the ones detecting RF signals (Askaryan and/or Geomagnetic) often share common requirements:

- Multichannel DAQ with $\sim (100MHz - 2GHz)$ bandwidth and long/multiple buffers;
- Multichannel Tx (arbitrary signal generator):
  - In-situ calibration and medium (e.g. ice) studies;
  - Building a 'test-bench' for DAQ: simulated signals and noise in various configurations and various phases;
- Beam forming.

An RFSoC technology by AMD (Xilinx) may be a possible **flexible** solution for both DAQ and Tx parts.

In this *very general* talk I'll try to summarize what we've learnt so far when working with RFSoC devices and corresponding tools/IPs.

RFSoC General Idea: ADC+DAC, FPGA, PS in one chip

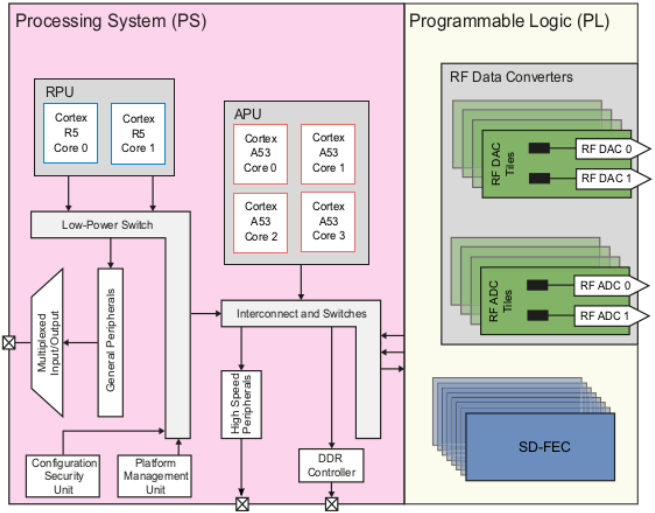


Figure from RFSoC Book

- RF Data Converters:
  - ADCs (up to 16): 12/14-bit up to 5.0 GSa/s;
  - DACs (up to 16): 14-bit up to 9.85 GSa/s;
- PL – FPGA (various options, next slide)
- PS:
  - Quad-core Arm Cortex-A53 – Operating System (PetaLinux, PYNQ);
  - Dual-core Arm Cortex-R5 Real-Rime Processor – Low-Level Real Control.

RFSoC: Versions

		Device Name	ZU21DR	ZU25DR	ZU27DR	ZU28DR	ZU29DR	ZU39DR	ZU42DR	ZU43DR	ZU46DR	ZU47DR	ZU48DR	ZU49DR
			Gen 1					Gen 2	Gen 3					
PS			**Quad-core** Arm® Cortex®-A53 MPCore™ up to 1.3GHz, **Dual-core** Arm Cortex-R5F MPCore up to 533MHz											
RF Data Converter	12-bit RF-ADC w/DDC	# of ADCs	0	8	8	8	16	16	–	–	–	–	–	–
RF Data Converter	12-bit RF-ADC w/DDC	Max Rate (GSPS)	0	4.096	4.096	4.096	2.058	2.220	–	–	–	–	–	–
RF Data Converter	14-bit RF-ADC w/DDC	# of ADCs	–	–	–	–	–	–	8 2	4	8 4	8	8	16
RF Data Converter	14-bit RF-ADC w/DDC	Max Rate (GSPS)	–	–	–	–	–	–	2.5 5.0	5.0	2.5 5.0	5.0	5.0	2.5
RF Data Converter	14-bit RF-DAC w/DUC	# of DACs	0	8	8	8	16	16	8	4	12	8	8	16
RF Data Converter	14-bit RF-DAC w/DUC	Max Rate (GSPS)	0	6.554	6.554	6.554	6.554	6.554	9.85(3)	9.85(3)	9.85(3)	9.85(3)	9.85(3)	9.85(3)
RF Data Converter		SD-FEC	8	0	0	8	0	0	0	0	8	0	8	0
RF Data Converter		Digital Front-End (DFE)	–	–	–	–	–	–	–	–	–	–	–	–
RF Data Converter		Number of DDCs per RF-ADC(1)	0	1	1	1	1	1	1	2	1	1	1	1
RF Data Converter		RF input Freq max. GHz	4					5	6					
RF Data Converter		Decimation / Interpolation	1x, 2x, 4x, 8x					1x, 2x, 4x, 8x	1x, 2x, 3x, 4x, 5x, 6x, 8x, 10x, 12x, 16x, 20x, 24x, 40x					
Programmable Logic (PL)		System Logic Cells (K)	930	678	930	930	930	930	489	930	930	930	930	930
Programmable Logic (PL)		CLB LUTs (K)	425	310	425	425	425	425	224	425	425	425	425	425
Programmable Logic (PL)		Max. Dist. RAM (Mb)	13.0	9.6	13.0	13.0	13.0	13.0	6.8	13.0	13.0	13.0	13.0	13.0
Programmable Logic (PL)		Total Block RAM (Mb)	38.0	27.8	38.0	38.0	38.0	38.0	22.8	38.0	38.0	38.0	38.0	38.0
Programmable Logic (PL)		UltraRAM (Mb)	22.5	13.5	22.5	22.5	22.5	22.5	45.0	22.5	22.5	22.5	22.5	22.5
Programmable Logic (PL)		DSP Slices	4,272	3,145	4,272	4,272	4,272	4,272	1,872	4,272	4,272	4,272	4,272	4,272
Programmable Logic (PL)		GTY Transceivers	16	8	16	16	16	16	8	16	16	16	16	16
Programmable Logic (PL)		PCIe® Gen3 x16	2	1	2	2	2	2	–	–	–	–	–	–
Programmable Logic (PL)		PCIe® Gen3 x16/Gen4 x8 / CCIX(2)	–	–	–	–	–	–	0	2	2	2	2	2
Programmable Logic (PL)		150G Interlaken	1	1	1	1	1	1	0	1	1	1	1	1
Programmable Logic (PL)		100G Ethernet MAC/PCS w/RS-FEC	2	1	2	2	2	2	0	2	2	2	2	2
Programmable Logic (PL)		System Monitor	2	2	2	2	2	2	2	2	2 2	2	2	2
Programmable Logic (PL)		Speed Grades	-1E, -1I, -1LI, -2E, -2LE, -2I, -2LI	-1E, -1I, -1LI, -2E, -2LE, -2I, -2LI	-1E, -1I, -1LI, -2E, -2LE, -2I, -2LI	-1E, -1I, -1LI, -2E, -2LE, -2I, -2LI	-1E, -1I, -1LI, -2E, -2LE, -2I, -2LI	-2I, -2LI	-1E, -1I, -1LI, -2E, -2I, -2LI	-1E, -1I, -1LI, -2E, -2I, -2LI	-1E, -1I, -1LI, -2E, -2I, -2LI	-1E, -1I, -1LI, -2E, -2I, -2LI	-1E, -1I, -1LI, -2E, -2I, -2LI	-1E, -1I, -1LI, -2E, -2I, -2LI
	Package Footprint	Package Dimensions	PSIO, HDIO, HPIO GTR, GTY RF-ADC, RF-DAC	PSIO, HDIO, HPIO GTR, GTY RF-ADC, RF-DAC	PSIO, HDIO, HPIO GTR, GTY RF-ADC, RF-DAC	PSIO, HDIO, HPIO GTR, GTY RF-ADC, RF-DAC	PSIO, HDIO, HPIO GTR, GTY RF-ADC, RF-DAC	PSIO, HDIO, HPIO GTR, GTY RF-ADC, RF-DAC	PSIO, HDIO, HPIO GTR, GTY RF-ADC, RF-DAC	PSIO, HDIO, HPIO GTR, GTY RF-ADC, RF-DAC	PSIO, HDIO, HPIO GTR, GTY RF-ADC, RF-DAC	PSIO, HDIO, HPIO GTR, GTY RF-ADC, RF-DAC	PSIO, HDIO, HPIO GTR, GTY RF-ADC, RF-DAC	PSIO, HDIO, HPIO GTR, GTY RF-ADC, RF-DAC
	D1156	35x35	214, 72, 208 4, 16 0, 0											
	E1156	35x35		214, 48, 104 4, 8 8, 8	214, 48, 104 4, 8 8, 8	214, 48, 104 4, 8 8, 8			214, 24, 128 4, 8 10, 8	214, 48, 104 4, 8 4, 4		214, 48, 104 4, 8 8, 8	214, 48, 104 4, 8 8, 8	
	G1517	40x40		214, 48, 299 4, 8 8, 8	214, 48, 299 4, 16 8, 8	214, 48, 299 4, 16 8, 8				214, 48, 299 4, 16 4, 4		214, 48, 299 4, 16 8, 8	214, 48, 299 4, 16 8, 8	
	F1760	42.5x42.5					214, 96, 312 4, 16 16, 16	214, 96, 312 4, 16 16, 16						214, 96, 312 4, 16 16, 16
	H1760	42.5x42.5									214, 48, 312 4, 16 12, 12			

Zynq™ UltraScale+™ RFSoCs

1. This value applies when all RF I/O of an RF-ADC tile are used. 2. Operates in compatibility mode for 16.0GT/s (Gen4) operation. See PG213. 3. For operation up to 10GSPS, contact your local Xilinx Sales Representative.

RFSoC: Versions

	Device Name	ZU63DR	ZU64DR	ZU65DR	ZU67DR
					DFE
PS		**Quad-core** Arm® Cortex®-A53 MPCore™ up to 1.3GHz, **Dual-core** Arm Cortex-R5F MPCore up to 533MHz			
RF Data Converter	14-bit RF-ADC w/DDC # of ADCs	4 / 2	8 / 2	6 / 8	8 / 2
	14-bit RF-ADC w/DDC Max Rate (GSPS)	2.95 / 5.9	2.95 / 5.9	5.9 / 2.95	5.9
	14-bit RF-DAC w/DUC # of DACs	4	8	6	8
	14-bit RF-DAC w/DUC Max Rate (GSPS)	10.0[3]	10.0[3]	10.0[3]	10.0[3]
	SD-FEC	0	0	0	0
	Digital Front-End Hard IP (DFE IP)	Channel Filter, DUC/DDC, Mixer, CFR, Complex Equalizer, PQ Resampler, DPD			
	Low PHY Hard IP	FFT/iFFT, PRACH	None	FFT/iFFT, PRACH	FFT/iFFT, PRACH
	Number of DDCs per RF-ADC[1]	1	1	1	1
	RF input Freq max. GHz	7.125			
	Decimation / Interpolation	1x, 2x, 3x, 4x, 5x, 6x, 8x, 10x, 12x, 16x, 20x, 24x, 40x			
Programmable Logic (PL)	System Logic Cells (K)	393	328	489	489
	CLB LUTs (K)	180	150	224	224
	Max. Dist. RAM (Mb)	5.47	4.56	6.8	6.8
	Total Block RAM (Mb)	17.6	15.8	22.8	22.8
	UltraRAM (Mb)	36.6	22.5	45.0	45.0
	DSP Slices	1,200	1,872	1,872	1,872
	GTY Transceivers	4	8	8	8
	PCIe® Gen3 x16/Gen4 x8 / CCIX[2]	0	0	0	0
	150G Interlaken	0	0	0	0
	100G Ethernet MAC/PCS w/RS-FEC	1	1	1	1
	System Monitor	2	2	2	2
	Speed Grades	-1I, -1LI, -2I, -2LI	-1I, -1LI, -2I, -2LI	-1I, -1LI, -2I, -2LI	-1I, -1LI, -2I, -2LI

Package Footprint	Package Dimensions	PSIO, HDIO, HPIO GTR, GTY RF-ADC, RF-DAC	PSIO, HDIO, HPIO GTR, GTY RF-ADC, RF-DAC	PSIO, HDIO, HPIO GTR, GTY RF-ADC, RF-DAC	PSIO, HDIO, HPIO GTR, GTY RF-ADC, RF-DAC
E1156	35x35	214, 24, 130 4, 8 6, 4	214, 24, 130 4, 8 10, 8	214, 24, 130 4, 8 6, 6	214, 24, 130 4, 8 10, 8

Notes:
1. This value applies when all RF I/O of an RF-ADC tile are used.
2. Operates in compatibility mode for 16.0GT/s (Gen4) operation. See PG213.
3. 10GSPS RF-DAC operation is available in -2I speed grade.

Zynq™ UltraScale+™ RFSoCs

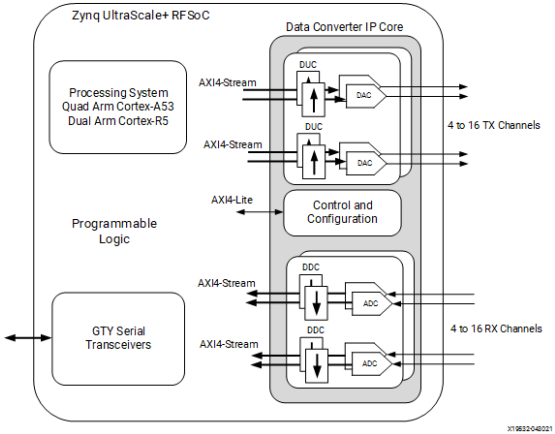
XMP105 (v1.12)

AMD
together we advance_

3

RFDC

RF Data Converter is a key Xilinx IP for RFSoCs

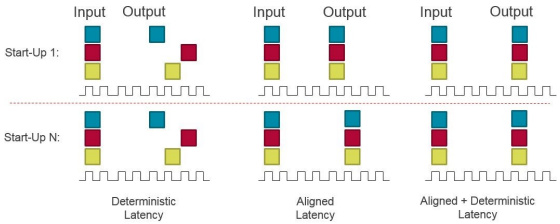


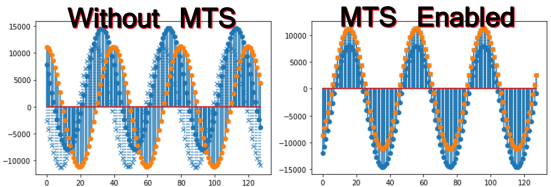
ADCs and DACs are organized in tiles:

- Gen 1/Gen 2: 4 12-bit Dual RF-ADC tiles, or 4 12-bit Quad RF-ADC tiles;
- Gen 3: 1, 2, or 4 14-bit Dual RF-ADC tiles, and/or 2 or 4 14-bit Quad RF-ADC tiles;

Each tile is clocked independently.

Multi-Tile Synchronization, Beam Forming





images from Getting in Synch with RF Data Converters and MTS Overlay

- In order to do beam forming (phase array) the tiles must be synchronized;
- SYSREF – master timing reference;
- RFDC has an MTS out-of-the-box (almost...) feature;
- MTS Overlay – a great example of the MTS performance and RFSoC overall.

Software Tools

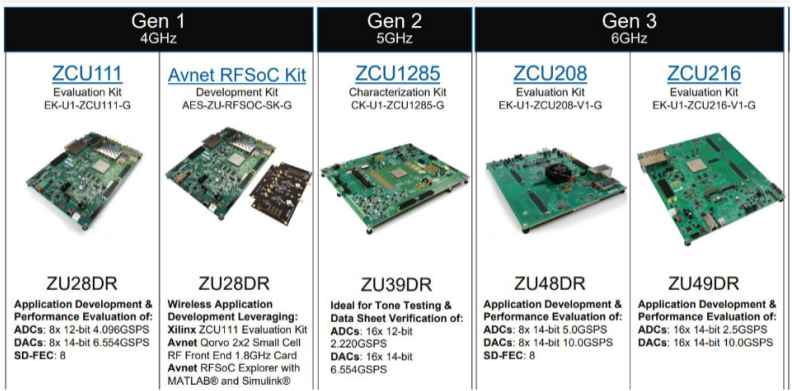
- **Vivado – PL (FPGA)**;
- Vitis – PS;
- IP Integrator;
- MATLAB and Simulink;
- **PYNQ + Jupyter**:
  - Very simple way to start working with the devices;
  - Overlays – board-specific implemented FPGA designs which can be uploaded to the chip from Jupyter;
  - No special software required – works from browser.

Legend / Key

1. Spectrum Analyser Tab Selection
2. Frequency Domain Plot
3. Control Panel
4. Spectrogram / Waterfall Plot
5. Information Panel

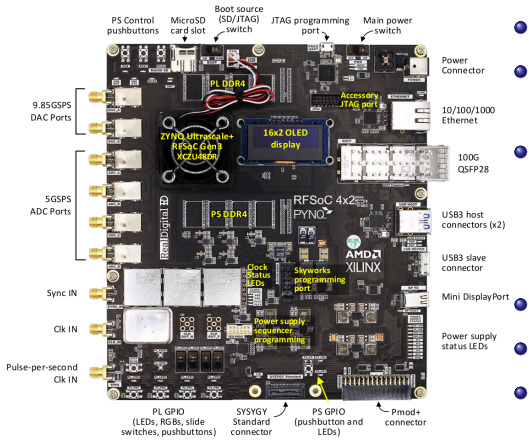
Figure from RFSoC Book

Evaluation Boards: "Standard" Options



$$$: ($10k+)

Evaluation Boards: Academic 4x2 Version



- RFSoC 4x2, Real Digital, Academic Version;
- $2149 – requires approval from Xilinx University Program (XUP);
- Gen3 ZU48DR (4 ADCs and 2 DACs are active); QSFP28 port for 4x25, 2x50 or 1x100 Gbps Ethernet; 8 GBytes DDR4 (4Gbytes - PS; 4GBytes - PL); ZCU208 compatible clocking subsystem
- Comes with PYNQ image;
- Vivado license through XUP;
- Power draw (entire board running a spectrum analyzer): $\sim$ 25W.

At UD we have ZCU208 and 4x2 boards

Useful Resources

- RFSoC Book by University of Strathclyde;
- RF Data Converter LogiCORE IP Product Guide (PG269)
- Getting in Synch with RF Data Converters: MTS;
- MTS Overlay;
- RFSoC PYNQ;
- RFSoC PYNQ Git;
- PYNQ Forum;
- Power Advantage Tool.

Conclusion

- RFSoCs are good candidates for various astroparticle experiments: both DAQ (Rx) and Tx:
  - 'Everything' in one chip $\rightarrow$ simpler hardware design;
  - Flexibility: almost the same hardware can be used for different purposes;
  - Design can be split between different people: e.g. PL and PS;
  - PYNQ gives an opportunity to start working with the devices right away;
- However there are still some cons:
  - Price/procurement;
  - Power consumption may be too high for some applications;
  - New technology $\rightarrow$ less expertise/resources and more bugs in designs and documentation.

Thank you!