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FPGA firmware design and verification for the ATLAS Liquid Argon Calorimeter trigger processor

Wednesday 12 June 2024 10:30 (15 minutes)

Firmware design is a major challenge in LHC experiment upgrades, often leading to significant project delays. While non configurable systems were immediately operational, recent experiences show firmware and hardware readiness can take years. This underscores the need for innovative methods to speed up firmware design and deployment. This study utilizes advanced firmware design techniques, like High-Level Synthesis (HLS), for the ATLAS Liquid Argon Calorimeter trigger processor. HLS simplifies the design process by focusing on essential functions rather than intricate hardware details such as clock networks or signal interfaces. This method allows for easy trade-offs between latency and area, essential for optimizing firmware performance. It enhances firmware maintenance, latency, logic area usage, and timing accuracy. The HLS application has the potential to streamline firmware design, reducing project delays, and increasing efficiency in large-scale experiments like the LHC upgrades.

Talk's Q&A

End of talk

Talk duration

10'+5' (very short, not recommended)

Will you be able to present in person?

Yes

Primary author: AGUIAR, Melissa (Federal University of Juiz de Fora (BR))

Co-authors: OLIVEIRA FACIO VICCINI, Lucca (CERN); SILVA OLIVEIRA, Marcos Vinicius (Brookhaven National Laboratory (US))

Presenters: OLIVEIRA FACIO VICCINI, Lucca (CERN); SILVA OLIVEIRA, Marcos Vinicius (Brookhaven National Laboratory (US)); AGUIAR, Melissa (Federal University of Juiz de Fora (BR))

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