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Artificial Intelligence workflows for FPGA & SoC using a Deep Learning Processor

Wednesday 12 June 2024 11:45 (30 minutes)

Artificial intelligence (AI) is everywhere. Automated image analysis, autonomous driving, industrial inspection, there are many applications today that could benefit from AI. Deep Learning is the most successful solution for image-based object classification, and for most practical applications it requires performant platforms like FPGAs and SoCs.

Designing AI for embedded devices such as FPGAs and SoCs is challenging because of resource constraints, the complexity of programming in Verilog or VHDL, and the hardware expertise needed for prototyping on an FPGA or SoC.

In this presentation I will explain, how to:
- Prototype and deploy Deep Learning-based vision applications using a Deep Learning Processor (DLP).
- Analyze profiling metrics and use compression methods like quantization and pruning to improve performance.
- Optimize the Deep Learning Processor configuration for the chosen AI models.

Talk's Q&A

During the talk

Talk duration

25'+12'

Will you be able to present in person?

Yes

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Session Classification: Algorithm implementation

Track Classification: Algorithm implementation in HDL and HLS