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Plan de Recuperación,  
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AGENCIA  
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# Porting MADGRAPH to FPGA

**Héctor Gutiérrez**, Luca Fiorini, Alberto Valero,

Arantza Oyanguren, Francisco Hervas

Instituto de Física Corpuscular (CSIC-UV)

1st FPGA Developers' Forum (FDF) meeting

June 12th, 2024



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DE VALÈNCIA

**Contact:**

**[Hector.Gutierrez@ific.uv.es](mailto:Hector.Gutierrez@ific.uv.es)**

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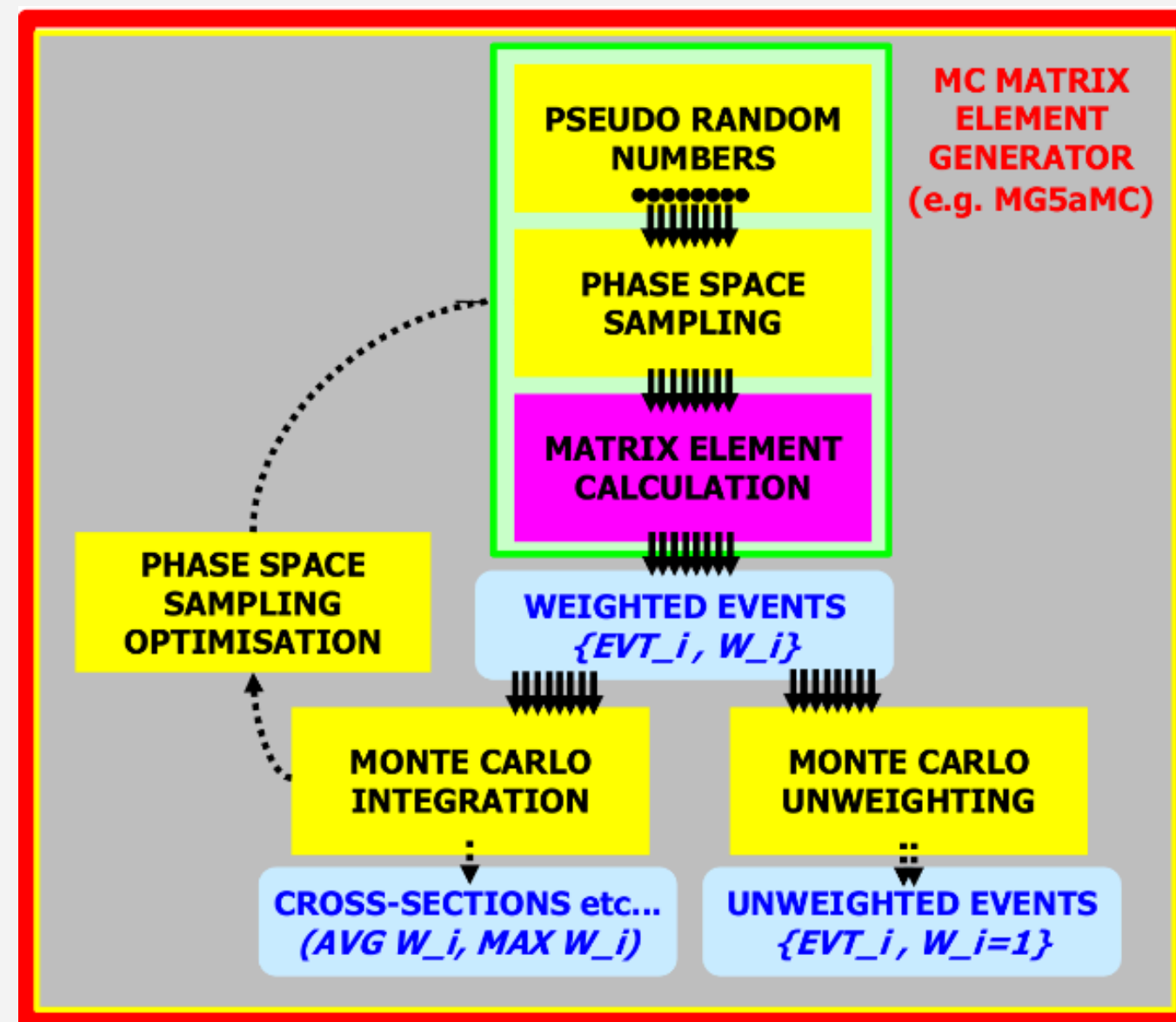
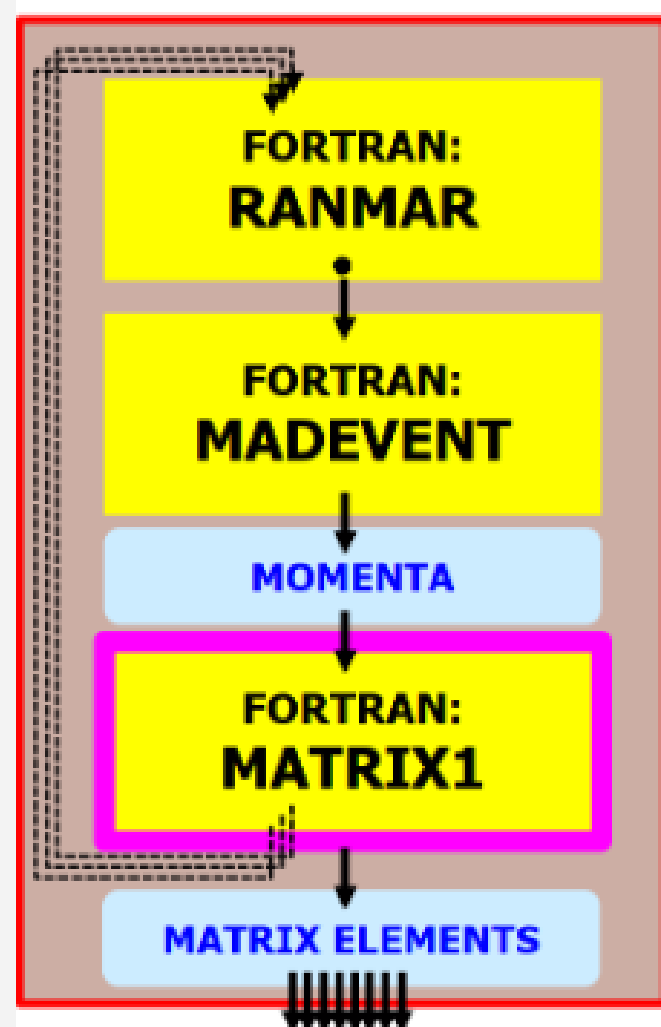
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# MADGRAPH\_aMC@NLO CPU

## What is MADGRAPH?:

*“MadGraph5\_aMC@NLO is a framework that aims at providing all the elements necessary for SM and BSM phenomenology, such as the computations of cross sections, the generation of hard events and their matching with event generators. Processes can be simulated to LO accuracy for any user-defined Lagrangian, and the NLO accuracy in the case of QCD (Quantum Chromo Dynamics) corrections to SM processes. Matrix elements at the tree- and one-loop-level can also be obtained.”*



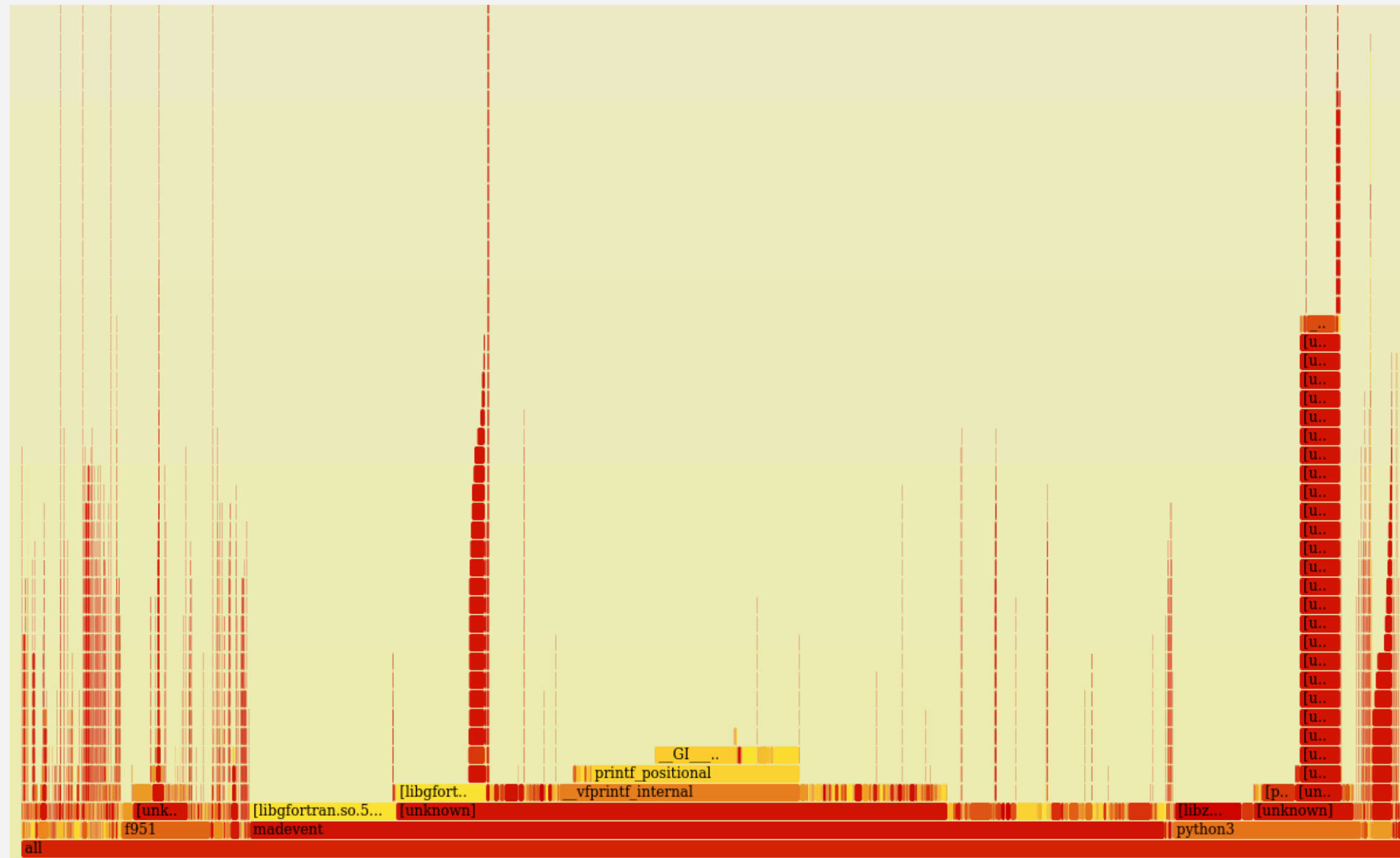
# MADGRAPH\_aMC@NLO CPU

$e^+ e^- \rightarrow \mu^+ \mu^-$

nevents = 204800

Total executing time = 16 s

Function Called



Events

**Total\_program (80%) = madevent (66%) + python3 (14%)**  
**madevent (66%) = ME (40%) + other resources (26%)**

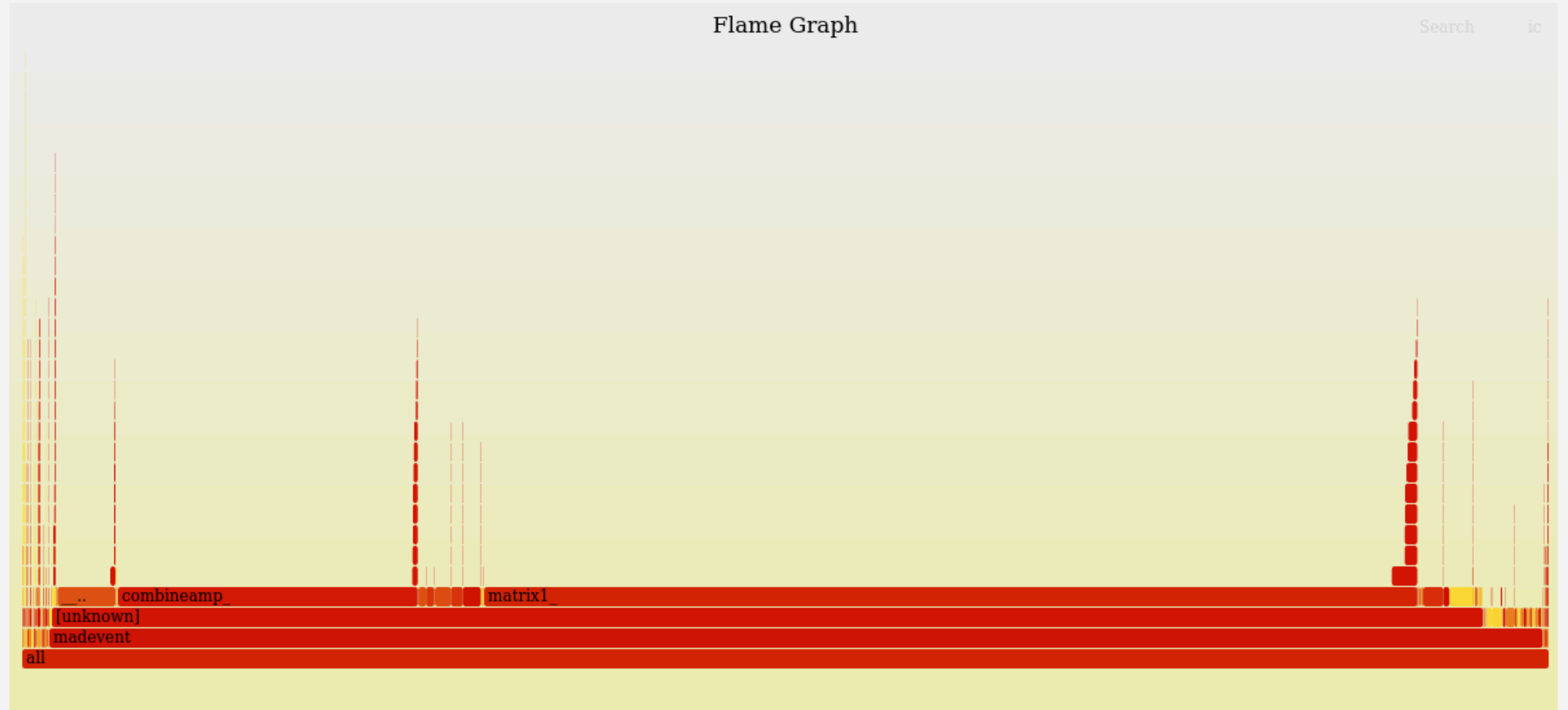
# MADGRAPH\_aMC@NLO CPU

$g g > t t^{\sim} g g g$

nevents = 204800

Total executing time = 32700 s = 9h

Function Called

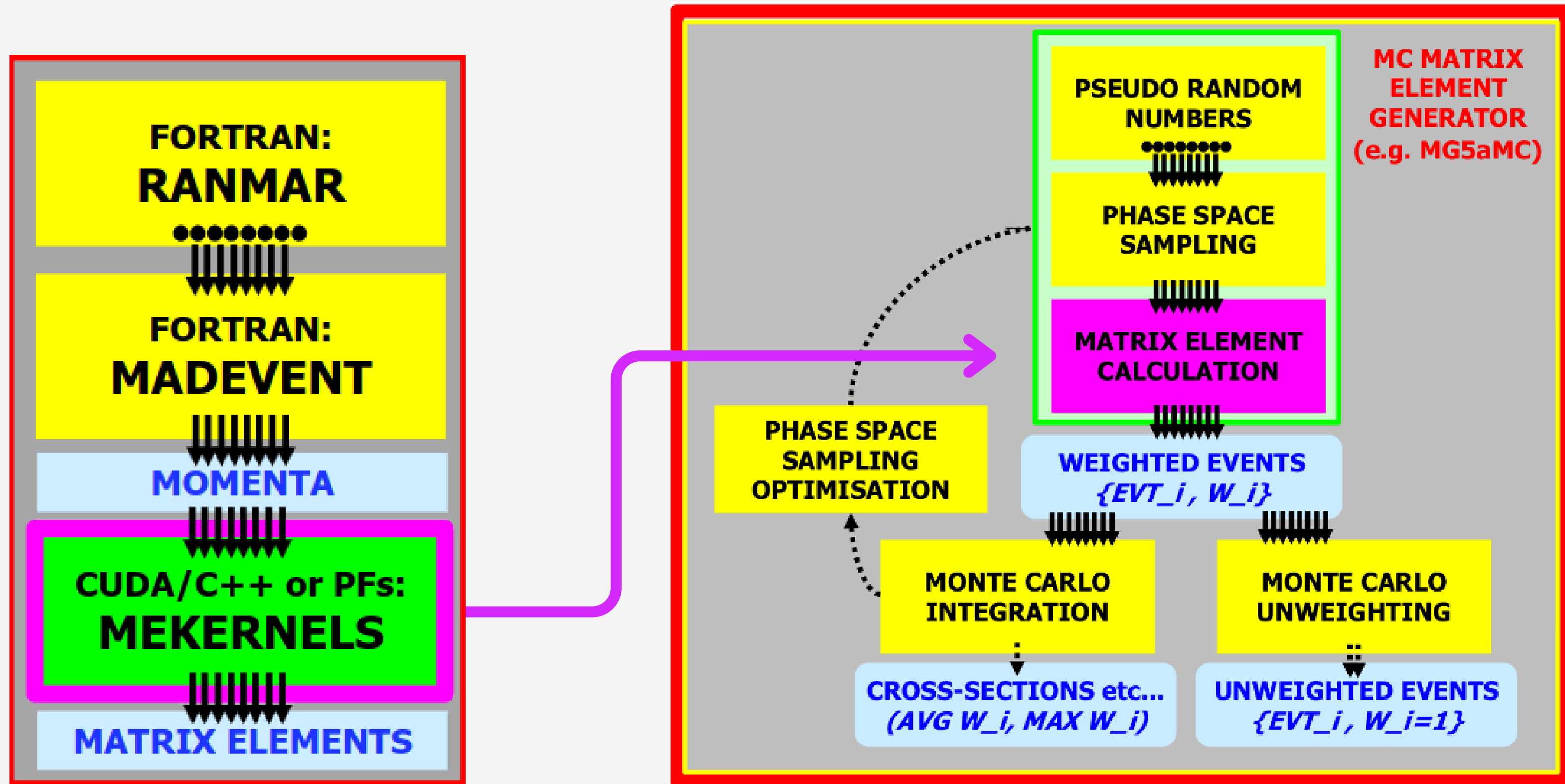


**madevent (97%) = ME (61%) + combineamp\_ (20%) + other resources (16%)**

Events

**5**

# MADGRAPH4GPU



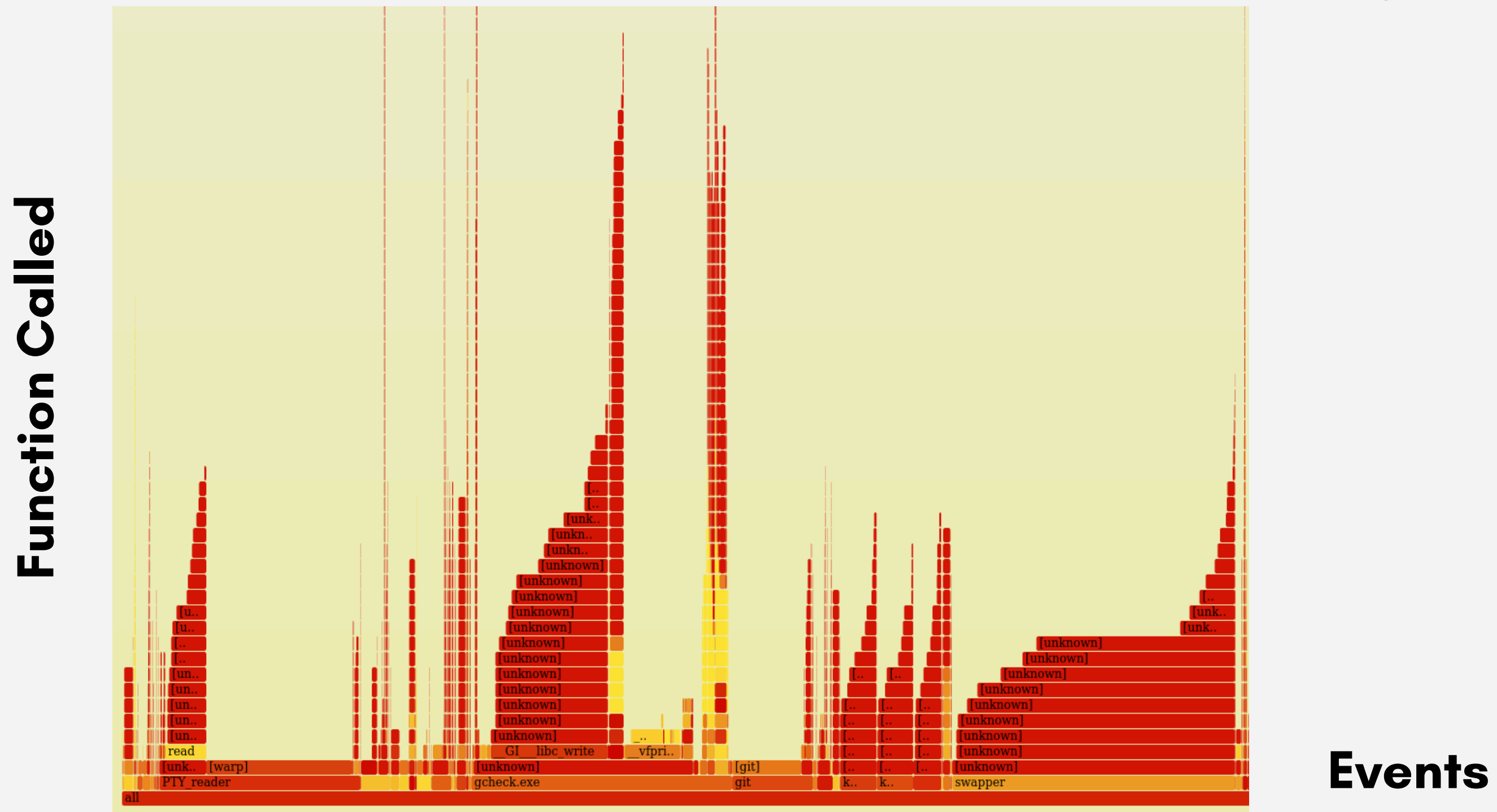
Credits to: Madgraph5\_aMC@NLO for GPUs group

# MADGRAPH4GPU

$e^+ e^- \rightarrow \mu^+ \mu^-$

nevents = 204800

Total executing time = 3.8 s



Total\_program (85%) = gcheck (27%) + Swapper (20%) + P\_reader (18%) + Other\_resources(20%)

gckeck (27%) = ME (24%) + other\_CUDA\_processes (3%)

# Results CPU vs GPU

Process	N_events	t_CPU(s)	t_GPU(s)	SpeedUp
$g g \rightarrow t \bar{t} g g g$	204800	32700 (9 h)	260 (4 min)	125,7
$g g \rightarrow t \bar{t} g g g$	819200	155760 (43 h)	1046 (17 min)	148,9
$g g \rightarrow t \bar{t} g g g$	38000000	7,35E+06 (3 month) (extrapolation)	48895 (13 h)	150,3
$e^+ e^- \rightarrow \mu^+ \mu^-$	204800	16.03+-0.07*	3,86+-0.01*	4,1
$e^+ e^- \rightarrow \mu^+ \mu^-$	819200	70.05+-0.10*	15.29+-0.03*	4,5
$e^+ e^- \rightarrow \mu^+ \mu^-$	6553600	512.1+-0.2* (8 min)	130.56+-0.03*	3,9

\*RMS value



# MADGRAPH FPGA

## Process: $e^- e^+ \rightarrow u^- u^+$

- top -> check\_sa.cpp (IN:NUMBER\_OF\_EVENTS, OUT: MOMENTA, OUT:MATRIX\_ELEMENT)

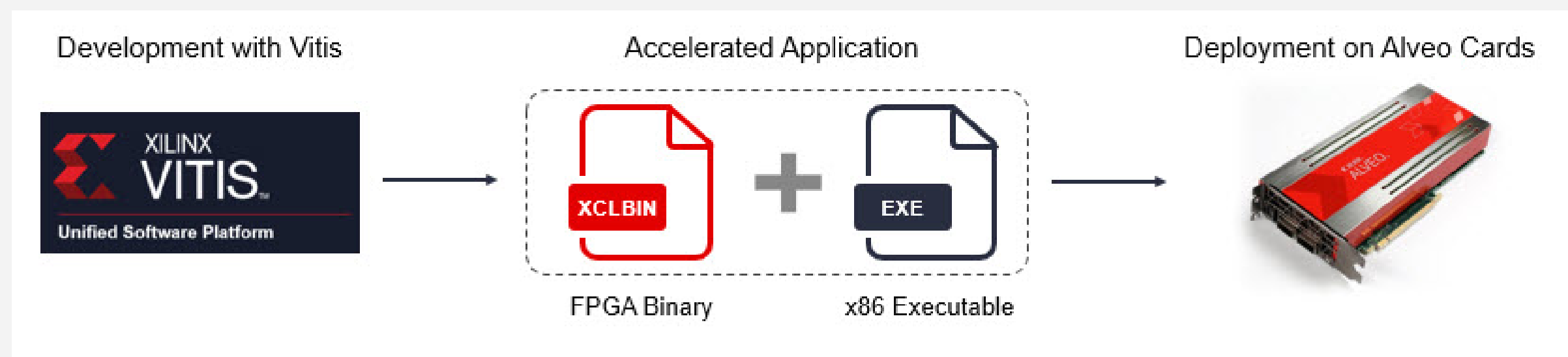
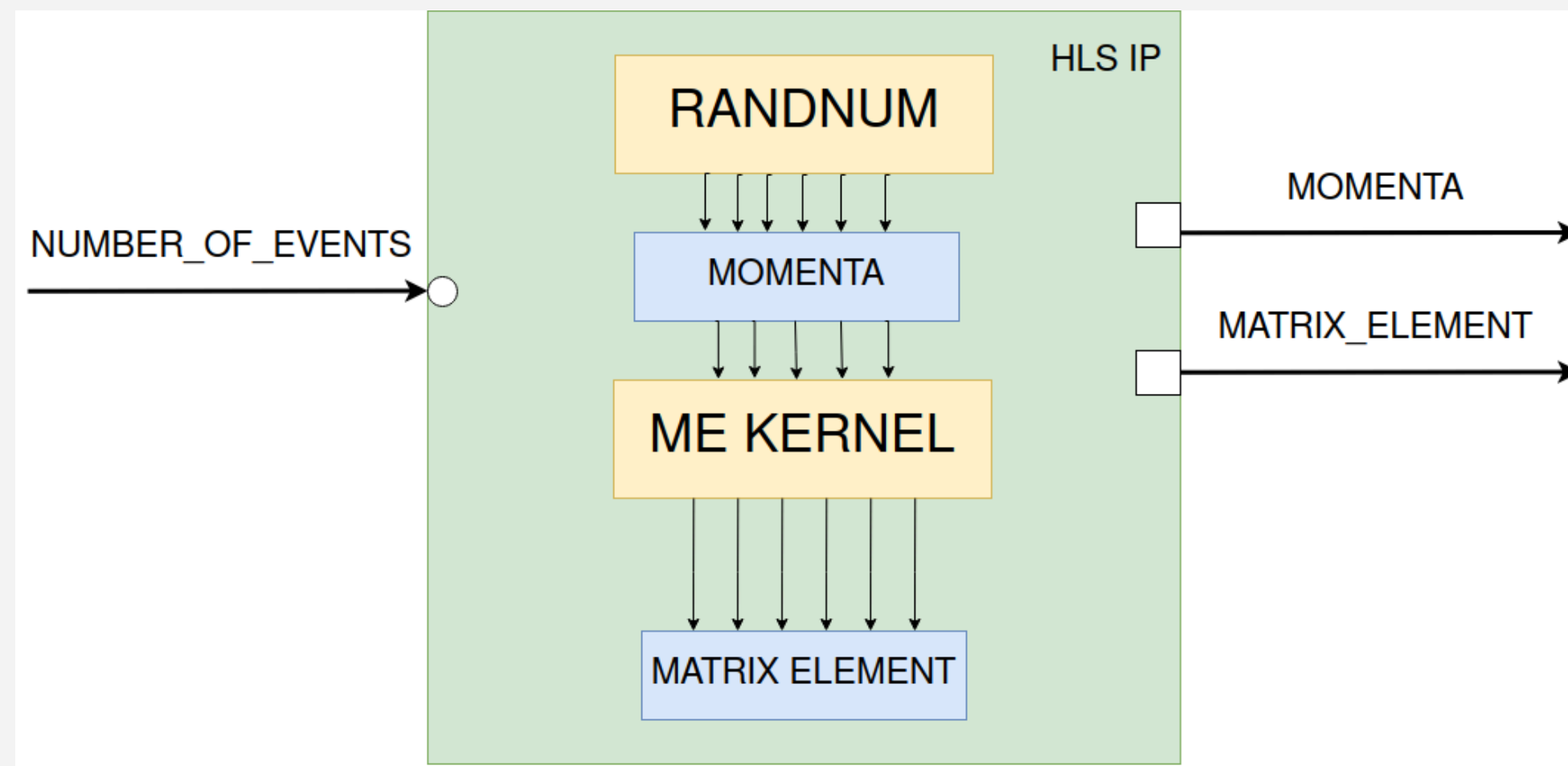
- Rambo -> Momenta
- SigmaKin -> Matrix Element

- Rambo(Energy, masses, weight, masses\_size)

- Generate Random Numbers
  - Obtain Momenta

- SigmaKin

- InitProc() -> SetIndependentCouplings
- SetParameters & SetDependentcouplings
- Calculate waveforms
- Calculate matrix of the process
  - Obtain Matrix Element

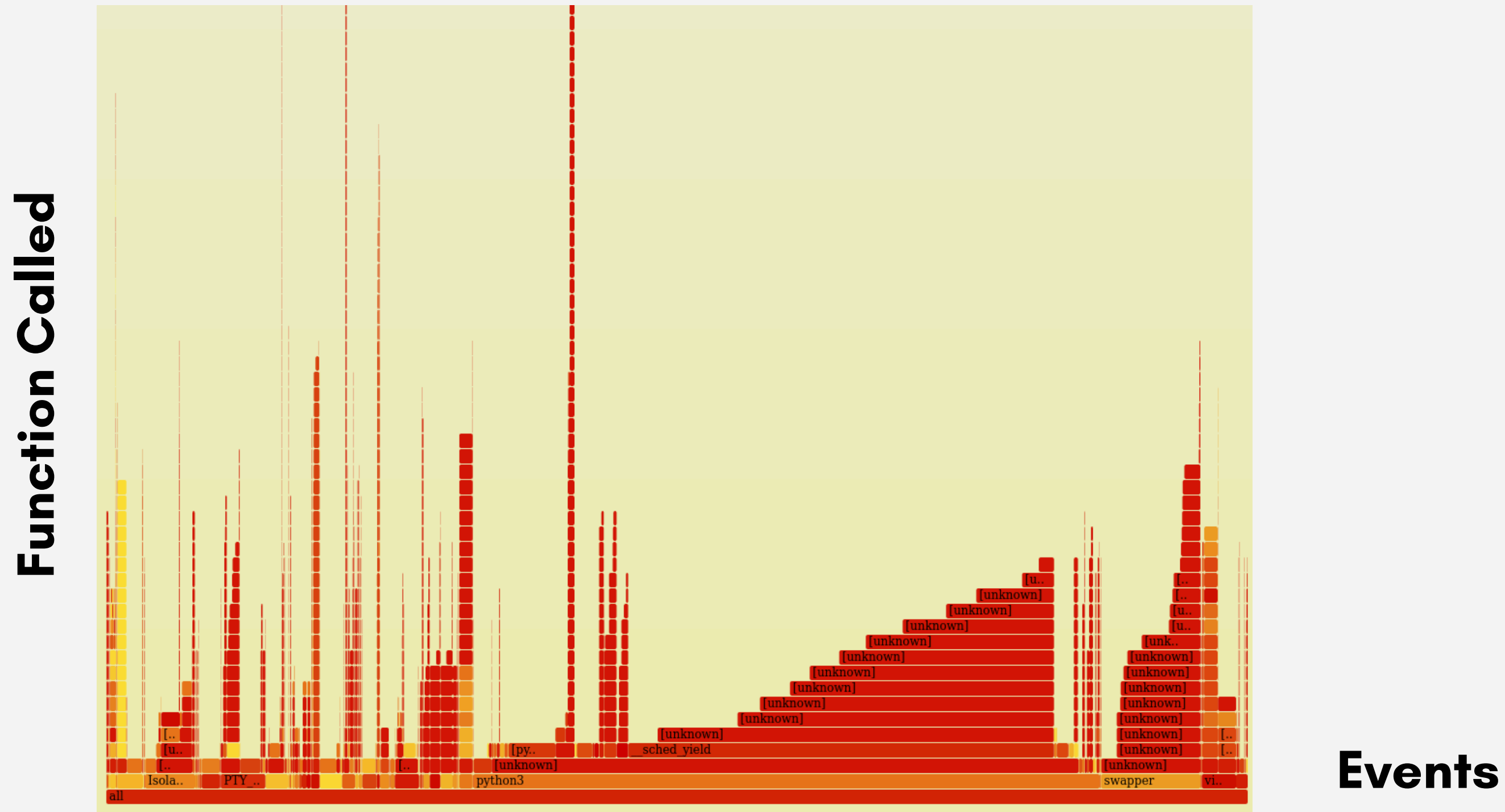


# MADGRAPH FPGA

$e^+ e^- \rightarrow \mu^+ \mu^-$

nevents = 204800

Total executing time = 0.48 s

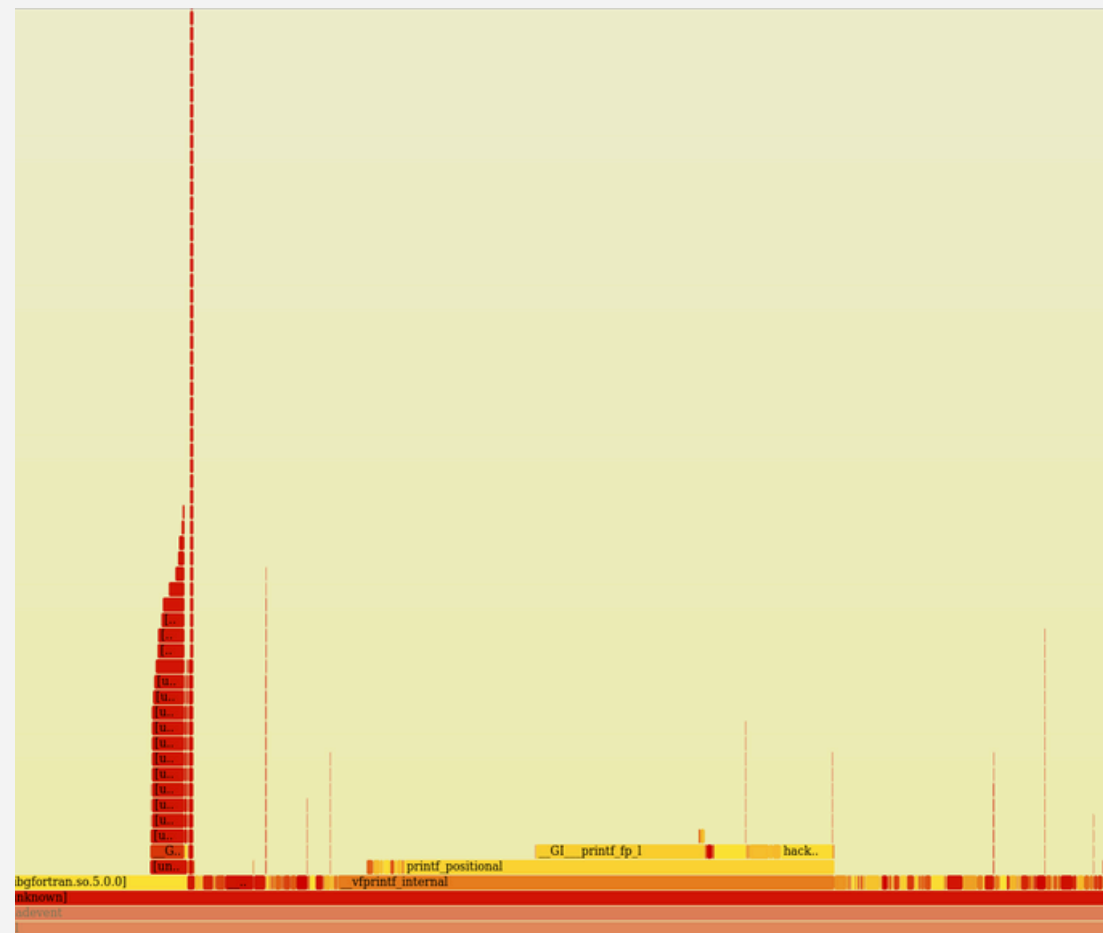


**Total\_program (81%) = Python3 (55%) + other resources (26%)**  
**python3 (55%) = ME (18%) + Communication\_FPGA\_CPU (37%)**

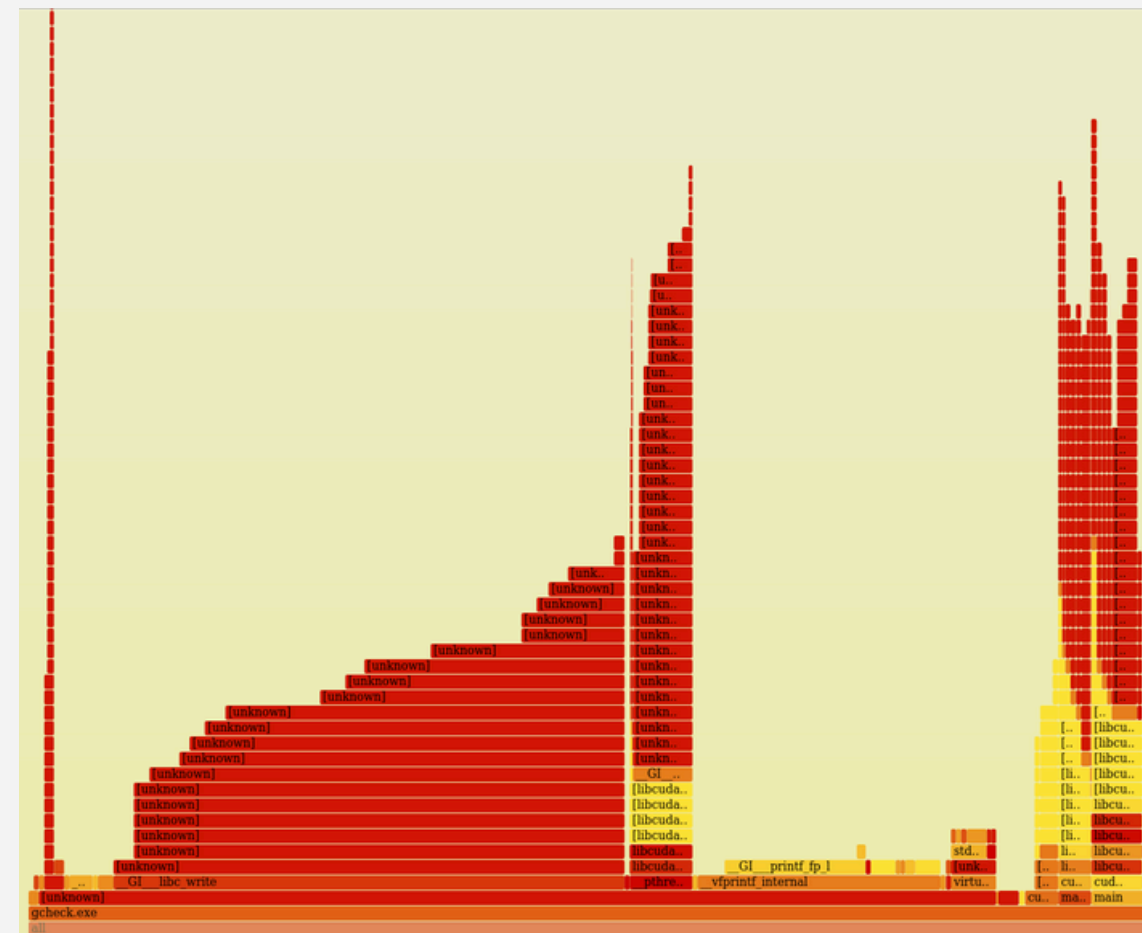
# MADGRAPH FPGA

$e^+ e^- \rightarrow \mu^+ \mu^-$

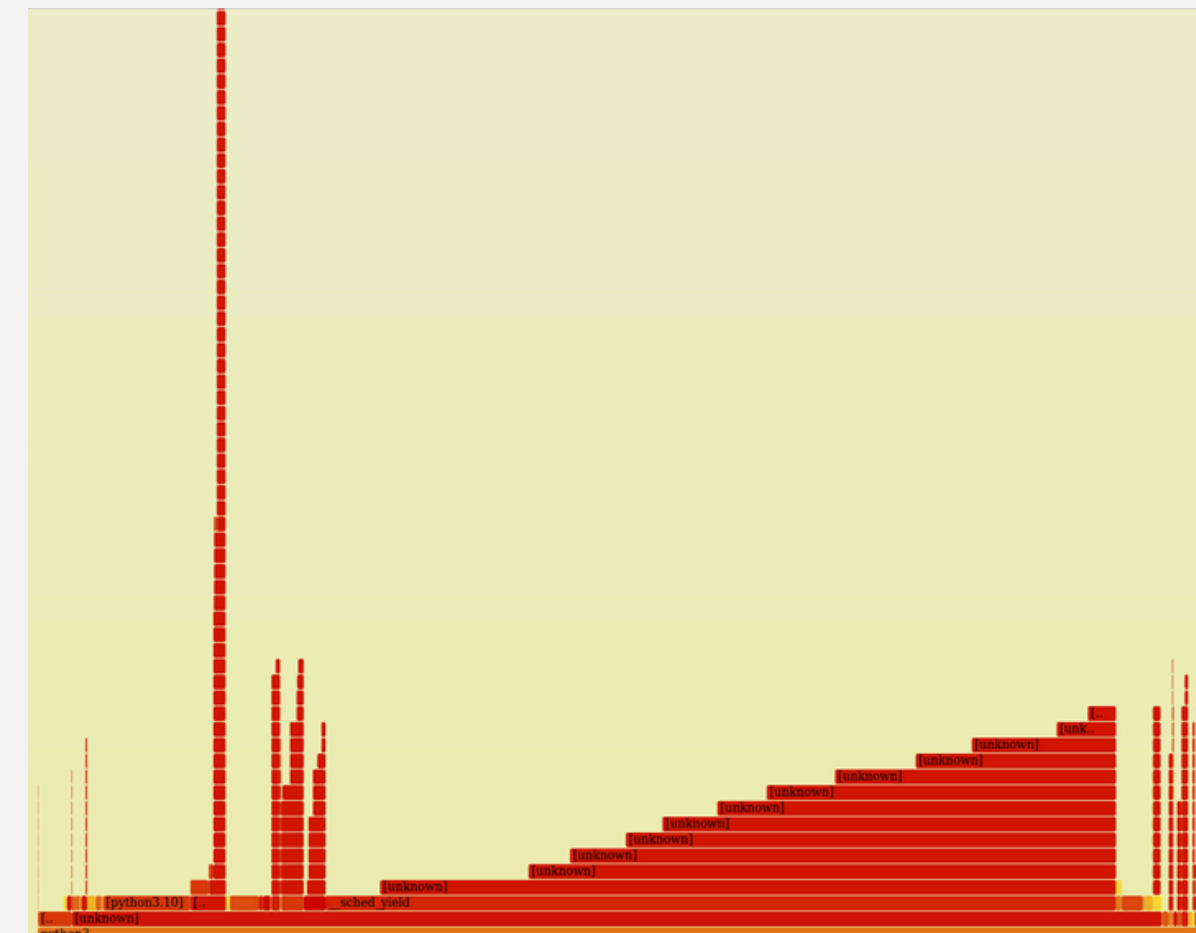
nevents = 204800



**CPU**  
**ME(40%)**



**GPU**  
**ME(24%)**



**FPGA**  
**ME(18%)**

# MADGRAPH FPGA

Process	BRAM	DSP	FF	LUT
me_calc	14	435	136833	81138

Frecuency (MHz)
100
Max = 137

# Results CPU vs GPU vs FPGA

Process	N_events	t_CPU(s)	t_GPU(s)	t_FPGA(s)	Time(CPU/FPGA)	Time(GPU/FPGA)
e+ e- > mu+ mu-	204800	16.03+-0.07*	3,86+-0.01*	0.476+-0.004*	33,6	8,1
e+ e- > mu+ mu-	819200	70.05+-0.10*	15.29+-0.03*	1,324+-0.003*	52,9	11,5
e+ e- > mu+ mu-	6553600	512.1+-0.2* (8 min)	130.56+-0.03*	9,027+-0.001*	56,7	14,4

**\*RMS value**

# Advantages and disadvantages of HLS for this application

- **Advantages:**

- Increased Efficiency and Productivity
- Better for prototyping
- Reduce the development time
- Enables developers to program FPGA in high-level languages

- **Disadvantages:**

- Additional Translation Time
- Slower Than coding RTL
- Less control over memory resources

# FUTURE IMPLEMENTATIONS

- Optimize the code for this case ( $e^+e^- \rightarrow u^+u^-$ )
- Create the code for a complex process
- Create the new version for all LO processes
- Study the implementation of BSM processes and NLO



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