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Transferring HLS-generated BDT model into existing firmware in the ATLAS Level-1 trigger

Wednesday 12 June 2024 14:25 (20 minutes)

An implementation of an ultra-low latency BDT fully evaluated on an FPGA was introduced for 2024 data taking in the ATLAS experiment with inference latency of 60 ns at 200 MHz and full pipelining. The BDT model is synthesized using Conifer and integrated into existing firmware written in VHDL. I will discuss some technical details on how I transferred HLS-generated code into existing firmware. For example, as the BDT is auto-generated, the signal delays must be adjusted at each retraining of the model, which is not practical to do manually. I'll show how I tackled this issue by implementing a python package to automatically compute sums and delays of signals.

Talk's Q&A

End of talk

Talk duration

20'+10'

Will you be able to present in person?

Yes

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Session Classification: Algorithm implementation

Track Classification: Algorithm implementation in HDL and HLS