# 1st FPGA Developers' Forum (FDF) meeting



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# **High-Level Synthesis for Machine Learning**

Wednesday 12 June 2024 16:15 (30 minutes)

hls4ml (High Level Synthesis for Machine Learning) is a tool for translating Neural Networks to synthesizable gateware for FPGAs. The tool is Python software that presents a user-friendly interface to achieve efficient Machine Learning inference in hardware. hls4ml interfaces to the main ML training libraries, as well as their extensions targeting quantized NNs. At the backend of hls4ml are HLS implementations of Neural Network operations targeting high performance for latency, throughput, and power usage. HLS workflows of multiple vendors are supported. In this talk we present the status of the project, recent developments, and future plans.

## Talk's Q&A

End of talk

#### Talk duration

20'+10'

# Will you be able to present in person?

Yes

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Session Classification: HDL development, verification, and simulation tools

Track Classification: HDL development tools