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UVVM –An introduction to the world's fastest growing FPGA verification methodology

Wednesday 12 June 2024 17:15 (40 minutes)

UVVM is the fastest growing FPGA verification methodology –independent of language. This is due to the improvement UVVM yields in both FPGA quality and development time. This open source Library and Methodology has the most extensive VHDL verification support available and lets you verify complex DUTs in a very efficient manner with great testbench overview. And if you have a really simple DUT, then you just use the simple part of UVVM. UVVM has been significantly updated through several ESA (European Space Agency) UVVM extension projects over the last few years.
UVVM provides a testbench kick start with open source BFMs and verification components for UART, SPI, AXI, AXI-lite, AXI stream, Avalon MM + Stream, I2c, GPIO, SBI, GMII, RGMII, Ethernet, Wishbone, Clock generator, and Error injector.
This presentation will give you a brief introduction to UVVM and also show the most important features and explain how they will help you make a better testbench and develop this much faster.

Talk's Q&A

During the talk

Talk duration

30'+12' (very long, not recommended)

Will you be able to present in person?

Yes

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Session Classification: HDL development, verification, and simulation tools

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