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# Becoming vendor agnostic with the help of model-based source code generation

*Thursday 13 June 2024 11:15 (35 minutes)*

The mid-range FPGA market currently sees the introduction of new FPGA(-SoC) devices with attractive specs. This presentation highlights three key areas to avoid vendor lock-in by leveraging OSS model-based source code generation. The use case is a tabletop 3D laser scanner, implemented on FPGA(-SoC) devices of all major vendors.
Firstly, in FPGA designs requiring (CPU) host-based control, design flexibility is increased by abstracting away the underlying UART/SPI/AXILite connection at the CPU-FPGA interface. This is achieved by co-generating C++ and VHDL source code for command and data passing. Secondly, IP blocks for SDRAM/MIPI/PCIe/HDMI are vendor specific. Simple parametrized wrappers help achieve vendor-independence for the most-employed interface features. Finally, live probing of FPGA designs via non-OSS protocols is tightly bound to vendor IDE's. Leveraging aforementioned CPU-FPGA interface, integrated RAM and case-specific RTL code generation helps bypass this dependency.

## Talk's Q&A

End of talk

## Talk duration

25'+12'

## Will you be able to present in person?

Yes

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