Summary

FPGA Developers Forum 2024

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On behalf of FDF Committee


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Not a complete summary.

My personal perspective.

Share yours!

Personal Experience with FPGA

HDL languages: steep learning curve!

Firmware development: time consuming!

Long compilation time (especially when dealing with timing issues)

Personal Experience with FPGA

HDL languages: steep learning curve! WIP

C to HDL

HLS : has been developed by Xilinx for the past 10+ years . Still has a learning curve (but much smaller) and some limitations (slower, less control).

HLS4ML, Conifer, Madgraph in HLS on FPGA

BondMachine

Support to enable bondmachine from high level languages

Personal Experience with FPGA

HDL languages: steep learning curve! WIP

Firmware development: time consuming!

Long compilation time (especially when dealing with timing issues) WIP

From C to Routed Circuits for FPGAs in Seconds:

Impressive 15 sec to full placed and routed circuit. Preliminary. Not for algorithm intensive application. Routing remains a challenging problem.

Better Verification/Monitoring

Formal Verification, UVVM, Spy Buffer

Formal Verification

My first time learning about this. A very powerful tool.

Open source option (SymbiYosis) makes this possible cost wise. Has some limitation, and can take some time getting it to work (but now we have all these tutorials!)

> Special license to the commercial option given to open source project (contact YosysHQ!)

- Assertion-Based Formal Debugging During RTL Development
- Open source formal verification with SymbiYosis
- Colibri: Towards a CERN-wide common cores library

This should become a common practice for firmware implementation!

Common Frameworks and Tools

To reduce duplication and avoid reinventing the wheel, lots of frameworks and tools are independently invented

The fact we have developed so many shows that we all recognize there is a need!

This community building may help consolidate some of the efforts. Let's get the discussion started on the forum!

- Colibri: Towards a CERN-wide common cores library
- CERN control group cores and tools
- Automatic code generation for managing the firmware and software for configuration/status registers and memories in the ATLAS Level-1 Central Trigger
- The YML2HDL Tool
- LoCod: an open-source hardware/software co-design tool for SoC/FPGA
- BondMachine
- ....

Common Frameworks and Tools

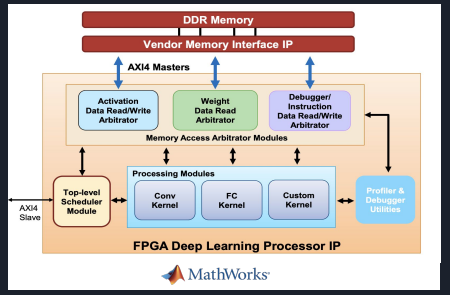
Why should experienced HDL developers adopt a common framework?

- Reduce the learning curve for beginners (i.e. your students)
- Expand your horizon - opportunity to learn different practices/approaches
- Opportunity to improve the existing framework with your expertise -> even better framework!

Machine Learning Algorithm

Pruning & quantization !

Common tools:



More specific applications

- A Neural Network-based trigger for detecting ultra-high-energy neutrinos for RNO-G and IceCube-Gen2
- Tree Tensor Network inference on FPGA
- Transferring HLS-generated BDT model into existing firmware in the ATLAS Level-1 trigger
- Hardware acceleration for fast Magnetic Resonance Fingerprinting map reconstruction: FPGA porting of a deep learning algorithm (<3 min network training on FPGA)

Other Very Interesting Topics

Madgraph on FPGA

Tested with e+e->u+u-. ~14 x faster than GPU, ~56 x faster than CPU. Same output.

Quantum applications (sensor, computing):

Use FPGAs to readout and control the qubits (cost effective)

And many more great talks!

Best Presentation!

We decided to select a best talk with a surprise gift!

Best Presentation!

Nominations:

- Alberto Perro Colibri: Towards a CERN-wide common cores library
- Mattia Ricchi Hardware acceleration for fast Magnetic Resonance Fingerprinting map reconstruction: FPGA porting of a deep learning algorithm
- Anna Malgorzata Kulinska Automatic code generation for managing the firmware and software for configuration/status registers and memories in the ATLAS Level-1 Central Trigger
- N. Engelhardt Assertion-Based Formal Debugging During RTL Development

Best Presentation!

What are your thoughts?