Contribution ID: **40** Type: **not specified**

Automatic code generation for managing the firmware and software for configuration/status registers and memories in the ATLAS Level-1 Central Trigger

Thursday, June 13, 2024 9:20 AM (20 minutes)

Large FPGA firmware designs, such as the ones used in the trigger systems of HEP experiments, typically contain many hundreds of configuration/status registers and memories. Managing the required HDL code and software for these can become challenging. We therefore developed a dedicated tool, called HardwareCompiler, which parses an XML description of the registers and memories and generates the required HDL code as well as C++ access functions used to configure and monitor the modules. The tool has been successfully applied in several generations of FPGA-based modules developed for the ATLAS Central Trigger system, greatly simplifying their development and testing. We present the capabilities of the HardwareCompiler with examples of generated VHDL register packages and address decoders as well as low-level C++ software. The latter is also used to generate wrappers for Python, which simplifies the development of scripts for configuring and testing the hardware.

Talk's Q&A

End of talk

Talk duration

20'+10'

Will you be able to present in person?

No

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