1st FPGA Developers' Forum (FDF) meeting

Tuesday 11 June 2024

Sharable HDL Cores - 30/7-018 - Kjell Johnsen Auditorium (15:40 - 18:20)

-Conveners: Francesco Gonnella; Mathieu Saccani

time	[id] title	presenter
15:40	[15] Convenient and reliable clock domain crossings, using scoped constraints and reusable blocks	VIK, Lukas
16:20	[1] COLIBRI: Towards a CERN-wide common cores library	PERRO, Alberto
16:50	[32] CERN control group cores and tools	GINGOLD, Tristan
17:20	[21] Fast Monitoring of FPGA algorithms using SpyBuffers	LONGARINI, Iacopo
17:50	[12] The BondMachine Project	MARIOTTI, Mirko MARIOTTI, Mirko