1st FPGA Developers' Forum (FDF) meeting

Wednesday 12 June 2024

Algorithm implementation: Late morning - 30/7-018 - Kjell Johnsen Auditorium (11:15 - 12:15)

-Conveners: Davide Cieri; Rui Zou

time	[id] title	presenter
11:15	[65] A Neural Network-based trigger for detecting ultra-high-energy neutrinos for RNO-G and IceCube-Gen2	MARCINIEWSKI, Pawel Mr MARCINIEWSKI, Pawel
11:45	[20] Artificial Intelligence workflows for FPGA & SoC using a Deep Learning Processor	VAN BEEK, Stephan

Algorithm implementation: Afternoon - 30/7-018 - Kjell Johnsen Auditorium (13:45 - 15:45)

-Conveners: Rui Zou; Davide Cieri

time	[id] title	presenter
13:45	[8] Tree Tensor Network inference on FPGA	BORELLA, Lorenzo
14:05	[43] Porting MADGRAPH to FPGA using High-Level Synthesis (HLS)	GUTIERREZ ARANCE, Hector
14:25	[64] Transferring HLS-generated BDT model into existing firmware in the ATLAS Level-1 trigger	REIKHER, David
14:45	[52] Hardware acceleration for fast Magnetic Resonance Fingerprinting map reconstruction: FPGA porting of a deep learning algorithm	RICCHI, Mattia MARELLA, Camilla
15:05	[36] Resource-efficient FPGA implementation of a channelization stage for superconducting quantum detectors DAQ systems	MUSCHEID, Timo
15:25	[46] Qibosoq: an open-source framework for quantum circuit RFSoC programming	CAROBENE, Rodolfo