1st FPGA Developers' Forum (FDF) meeting

Wednesday 12 June 2024

HDL development, verification, and simulation tools: Late afternoon - 30/7-018 - Kjell Johnsen Auditorium (16:15 - 18:45)

-Conveners: Tom Williams; Nicolo Vladi Biesuz

time	[id] title	presenter
16:15	[56] High-Level Synthesis for Machine Learning	GHIELMETTI, Nicolo
16:45	[5] Under the Canopy: Exploring Conifer for Low-Latency Decision Forests on FPGAs	SUMMERS, Sioni Paris
17:15	[26] UVVM – An introduction to the world’s fastest growing FPGA verification methodology	TALLAKSEN, Espen
17:55	[30] LoCod: an open-source hardware/software co-design tool for SoC/FPGA	MANNI, Florent

Thursday 13 June 2024

HDL development, verification, and simulation tools: Morning - 30/7-018 - Kjell Johnsen Auditorium (09:00 - 10:45)

-Conveners: Evangelia Gousiou; Francesco Gonnella

time	[id] title	presenter
09:00	[17] YML2HDL tool	COSTA DE PAIVA, Thiago
09:20	[40] Automatic code generation for managing the firmware and software for configuration/status registers and memories in the ATLAS Level-1 Central Trigger	KULINSKA, Anna Malgorzata
09:40	[49] Assertion-Based Formal Debugging During RTL Development	ENGELHARDT, N.
10:15	[7] Open source formal verification with SymbiYosis	THOMA, Yann

HDL development, verification, and simulation tools: Late morning - 30/7-018 - Kjell Johnsen Auditorium (11:15 - 12:20)

-Conveners: Francesco Gonnella; Evangelia Gousiou

time	[id] title	presenter
11:15	[61] Becoming vendor agnostic with the help of model-based source code generation	WIRTHMÜLLER, Alexander
11:50	[29] HDL on git (Hog)	ARANZABAL BARRIO, Nordin