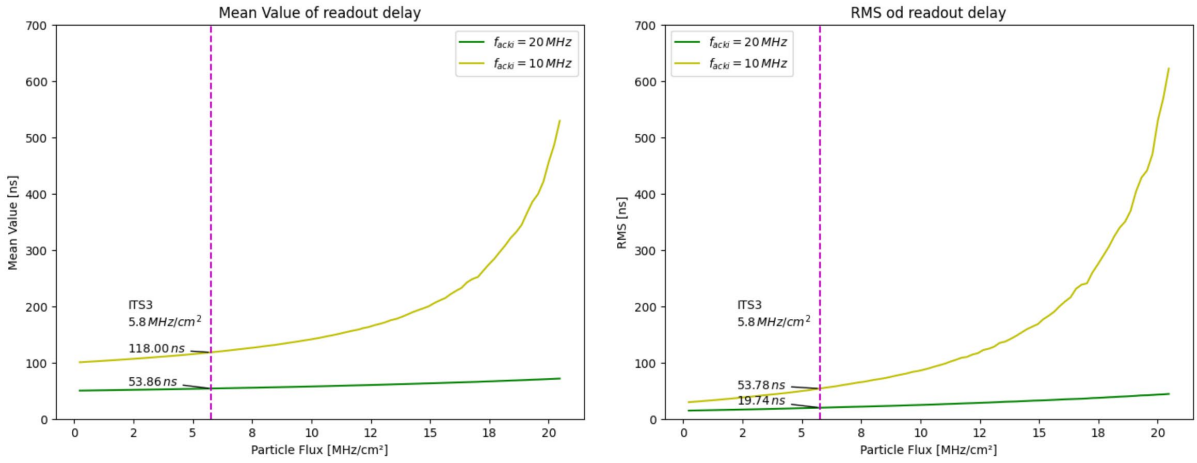

(a) (b)

Fig. 1. The mean and RMS of readout latency as a function of particle flux (~event generation) for different readout clock speeds.

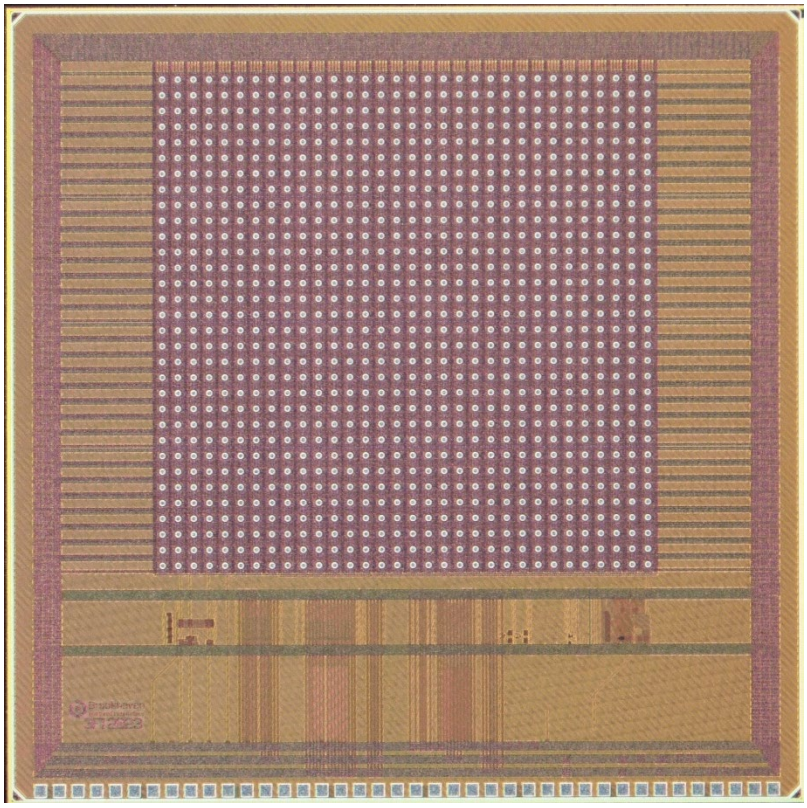

Fig. 2. EDWARD65P1: Test chip built on the skeleton of X-ray detector readout chip

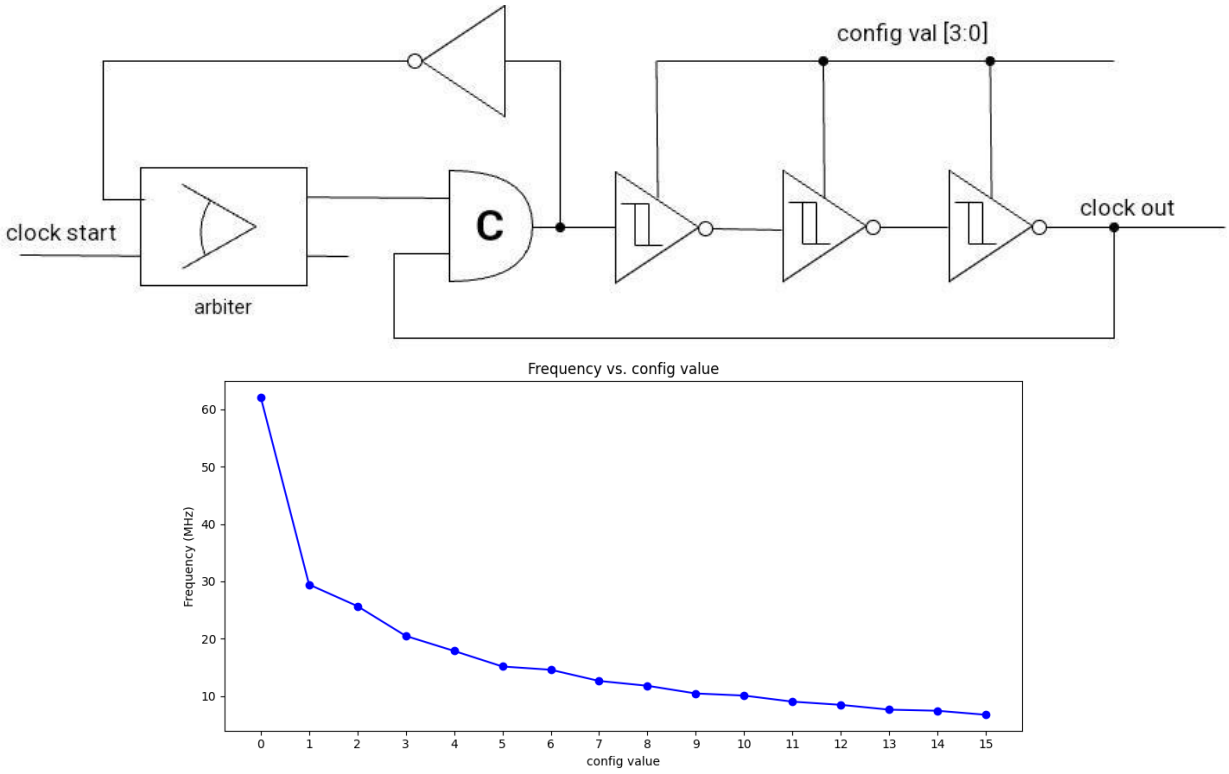

Fig. 3. Block diagram of in-pixel clock generator and the freqency vs. configuration value plot

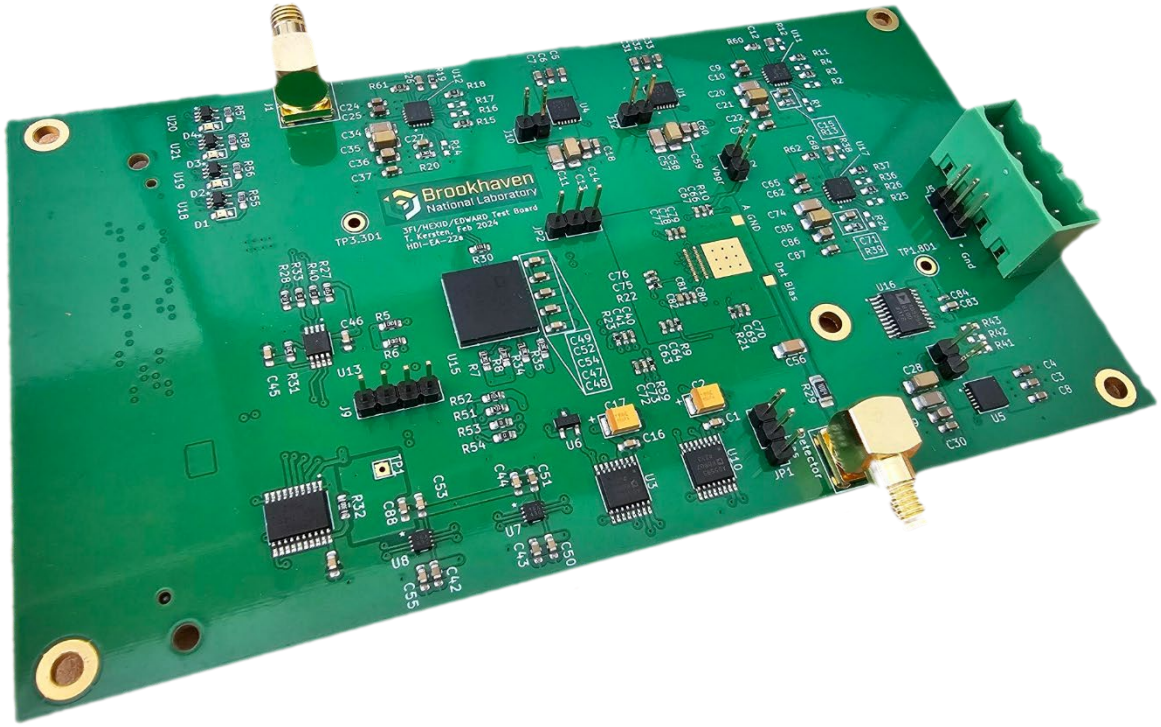

Fig. 4. Testbench

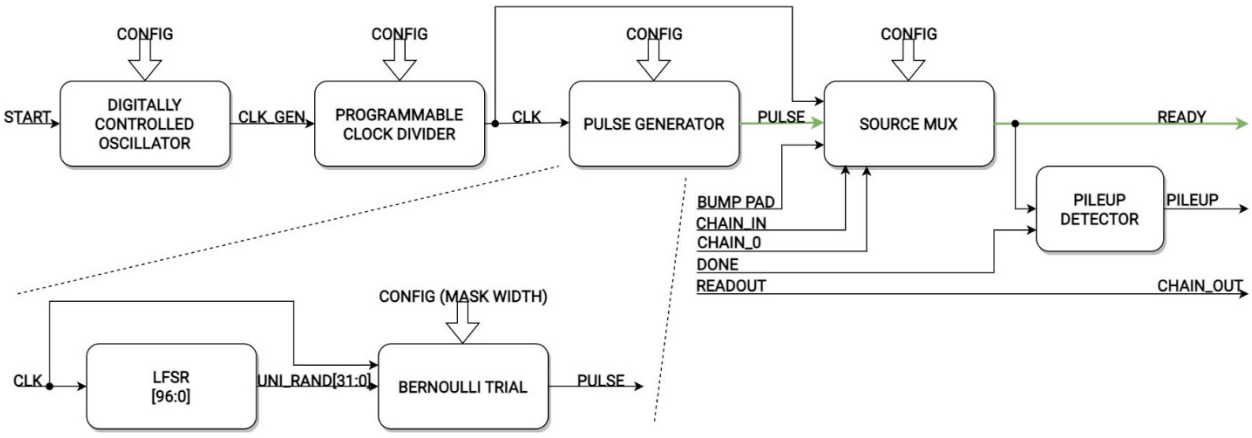

Fig. 5. Block diagram for the signal generator implemented in the EDWARD65P1 chip [4]

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