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Event-Driven Readout Development: Testing of the EDWARD65P1 Chip with Integrated Event Generators

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In response to the need for higher timing resolution innovative readout schemes are being explored for silicon vertex detectors like being under development ALICE ITS3 and EIC ePIC SVT. A promising direction is the event-driven approach, exemplified by the EDWARD (Event-Driven With Access and Reset Decoder) architecture. This presentation will highlight the capabilities of the EDWARD65P1 test ASIC, which includes a digital event generator to generate uncorrelated hits at varying rates. For the first time presented at TWEPP 2021, EDWARD has been shown operational, offering substantial improvements in timing resolution and setting new benchmarks for asynchronous readout systems.

Summary (500 words)

Current methodologies for data readout from pixels in silicon detectors [1][2] predominantly utilize priority encoders. While efficient, these systems lack memory elements, rendering them vulnerable to data corruption during readouts caused by switching activities. Traditional mitigation involves snapshotting the matrix state before readout, which prevents data corruption and metastable states but limits timing resolution to the frame rate, recently proposed to be reduced from 10 µs to 2 µs in ITS3 [3], which is still far more than needed 100 ns scale or lower.

In order not to be bound by time frames and to allow on-the-fly sparsification free of polling, present in for example token rings the EDWARD architecture has been developed [4][5]. EDWARD is an event-driven solution that incorporates a memory cell within the arbitration tree. This design moves away from purely combinatorial arbitration logic to a robust asynchronous operational framework. This frame-free mechanism ensures that each detected hit generates a single readout request, enhancing timing resolution primarily limited by the uncertainty of request arrival at the peripheral circuitry. Such uncertainty stems from variable propagation times within the arbitration tree –measurable and compensable –and queuing delays during high hit rates (Fig. 1). It is important to emphasize that there is no digital activity directed to the pixel matrix unless there is a request.

We have integrated the test architecture into the EDWARD65P1 chip (Fig. 2). This ASIC is equipped with digital circuitry designed to simulate various event rates simultaneously in each of its 1024 independent digital channels. Each channel includes a pausable, frequency-controllable ring oscillator based on inverters with hysteresis, capable of generating clocks ranging from 7 MHz to 62 MHz (Fig. 3). The oscillator connects to a versatile clock divider, which consists of a 4-bit pre-divider reducing the frequency by powers of two, and a secondary divider adjustable from 1 to 15. The resulting clock signal drives a 97-bit maximum-length Linear Feedback Shift Register (LFSR) utilizing Fibonacci architecture for parallel feedback signal calculation, allowing a pseudo-random number to be generated in every clock cycle. The result then enters a Bernoulli trial block, converting the sequence of random numbers into a Poisson process sequence in the time domain with an exponential distribution [6]. This hardware forms a robust digital Poisson process generator, demonstrating the EDWARD architecture's capability to simulate realistic sensor signal behaviors in virtually any rate and channel occupancy scenarios. The generator fits into a footprint of a single pixel.

Our presentation will focus on experimental results from the EDWARD65P1 chip, particularly assessing how

closely simulation predictions align with the observed timing characteristics. We measure readout latency, both mean and RMS values, under various event rate hits and clock speeds. A complete testbench has been set up for these experiments (Fig.4), and we anticipate collection of whole data sets before the conference. These ongoing efforts are refining the capabilities of silicon detector technologies, defining a new standard for asynchronous readout systems, and highlighting the transformative potential of the EDWARD architecture for highly segmented detectors.

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