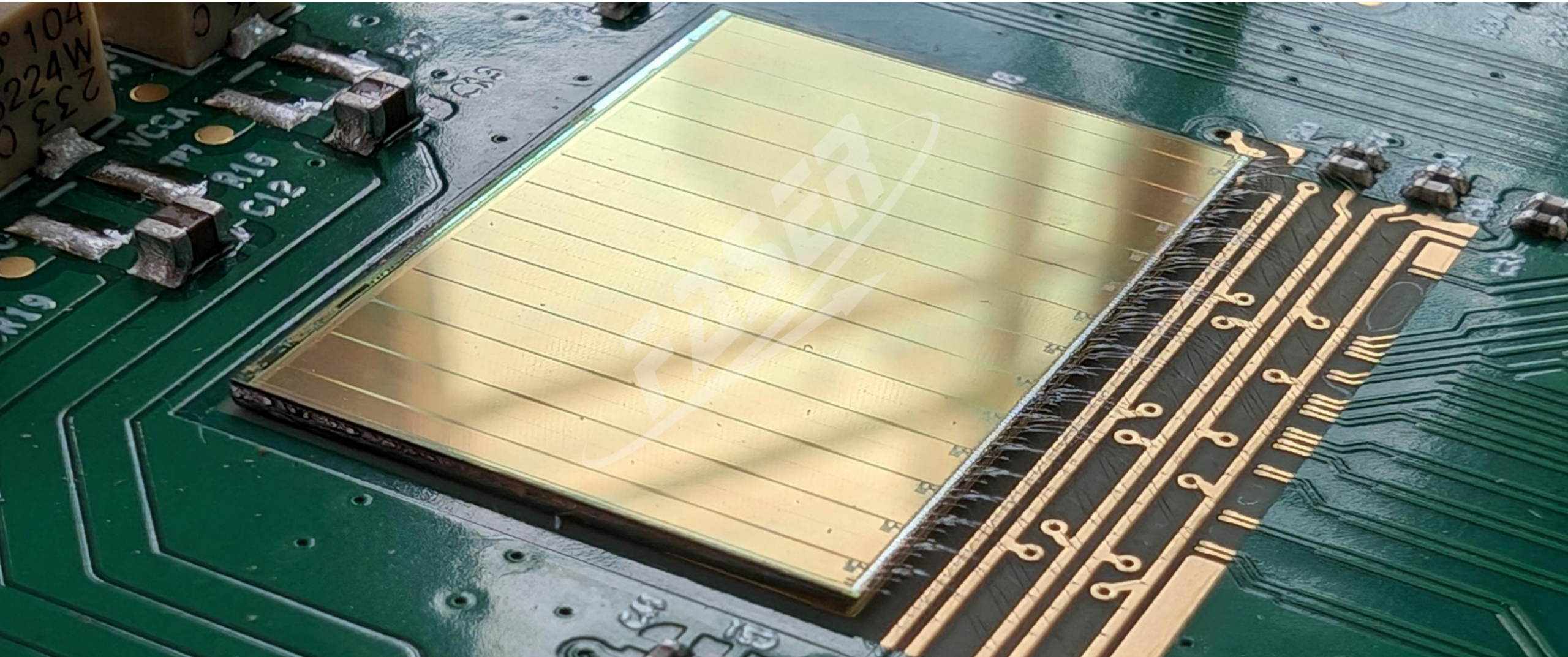
Design and Characterization of the Monolithic ASIC for the Preshower Upgrade of the FASER Experiment

Carlo Alberto Fenoglio, on behalf of the Pre-Shower Upgrade team

UNIVERSITÉ DE GENÈVE
FACULTY OF SCIENCE
Department of Nuclear and Particle Physics

Glasgow, 2nd October 2024



Outline

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FASER Experiment at CERN

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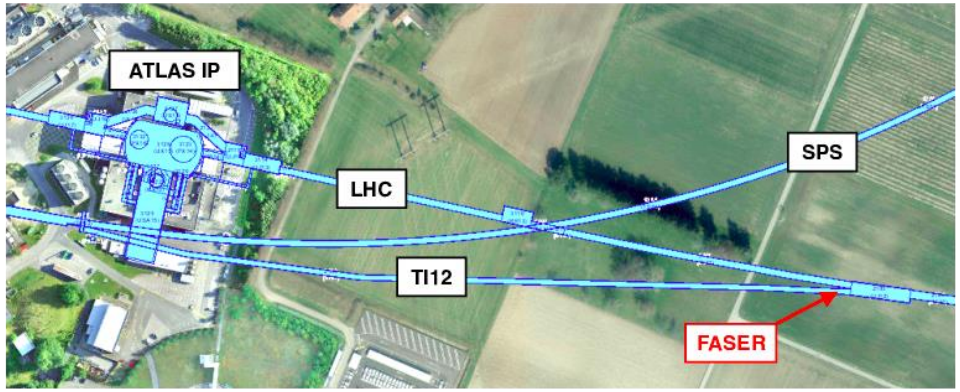
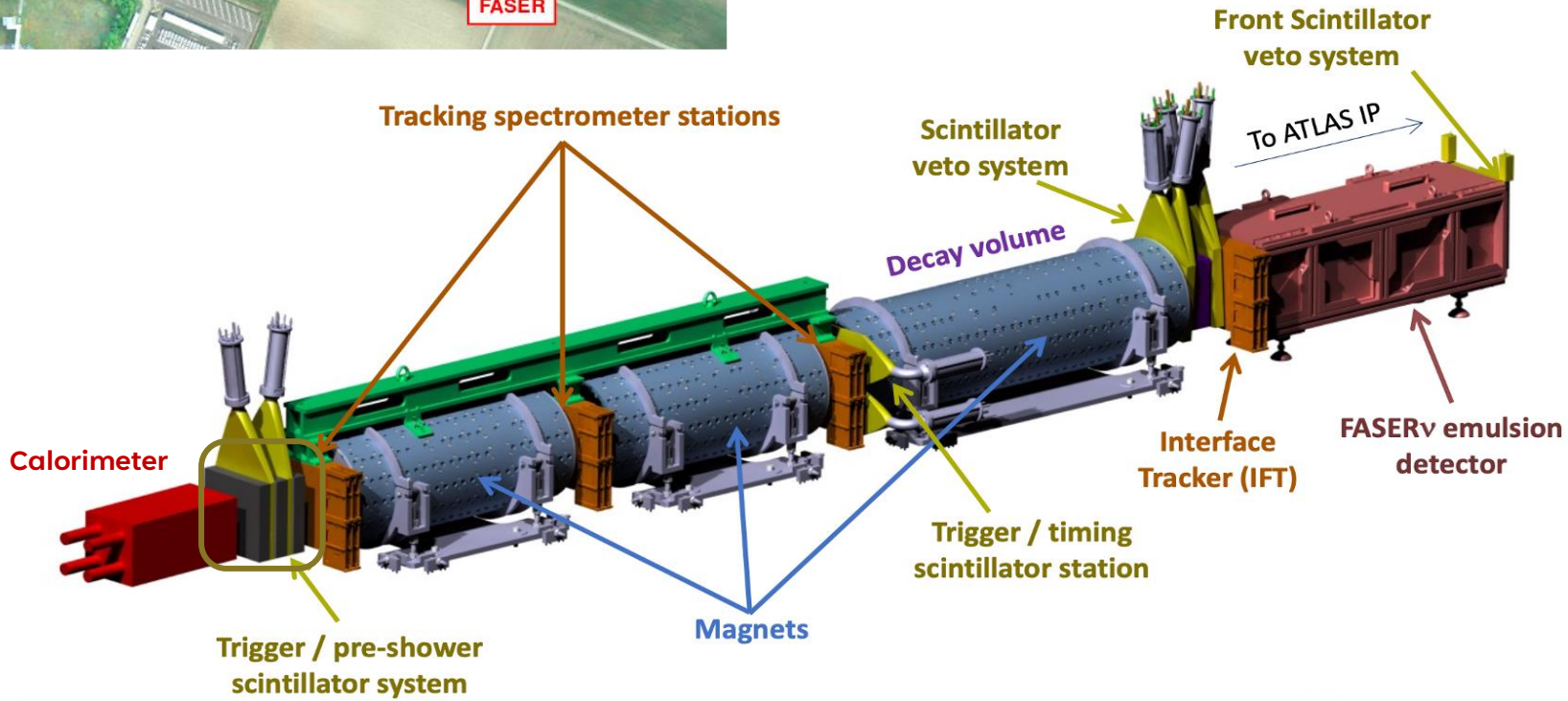


ForwArd Search ExpeRiment at the LHC

Search for light, weakly interacting particles as potential dark matter candidates



Preshower Detector Upgrade

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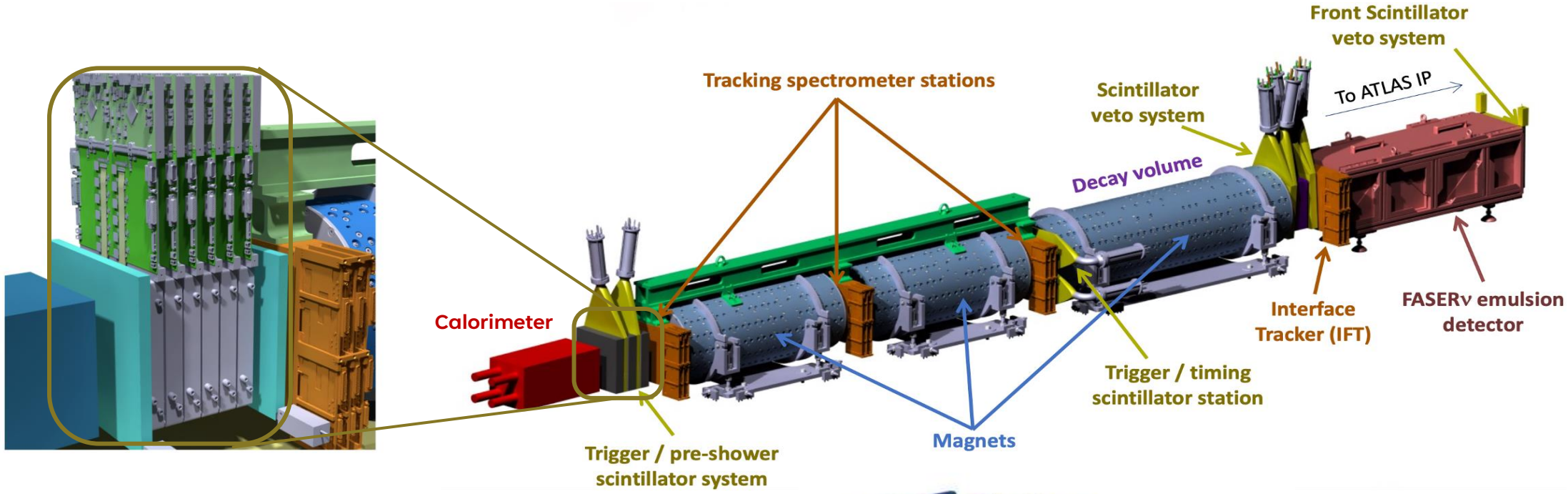
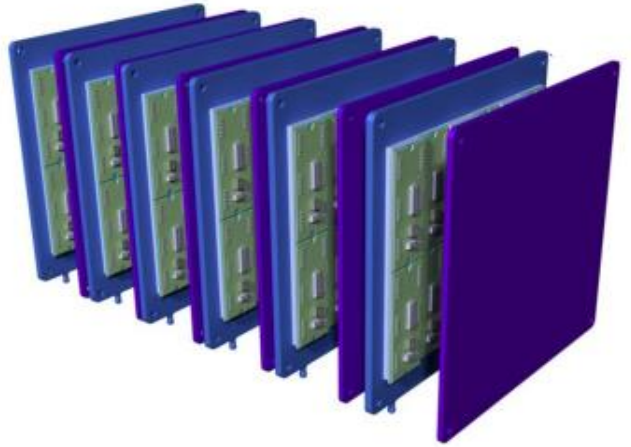


- Installation in **December 2024**
- Operation during **LHC Run 3** and **Run 4**

New preshower detector with 200 μm X-Y granularity for di-photon events resolution



- 6 detector planes:
  - 1 W layer
  - 1 Si plane

CERN-LHCC-2022-006 (Technical proposal)

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1 FASER Experiment

Experiment overview and preshower upgrade

2 **Preshower ASIC**

Chip Architecture, front-end electronics and readout

3 ASIC Characterization

Lab measurements and prototype comparison

4 Conclusion

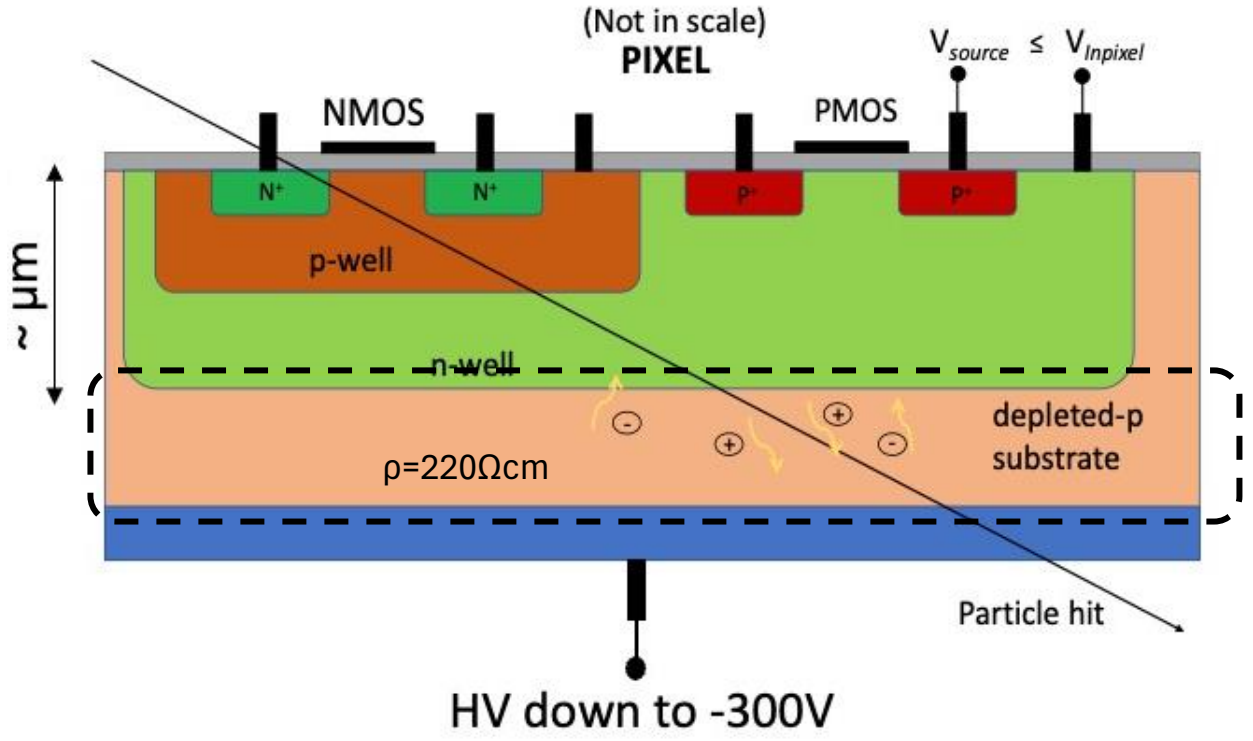
Summary and outlook

Monolithic ASIC Technology

Monolithic active pixel sensor

130 nm SiGe BiCMOS technology (IHP SG13G2)

- High R substrate (220 Ωcm), 150 µm thick



Monolithic ASIC Technology

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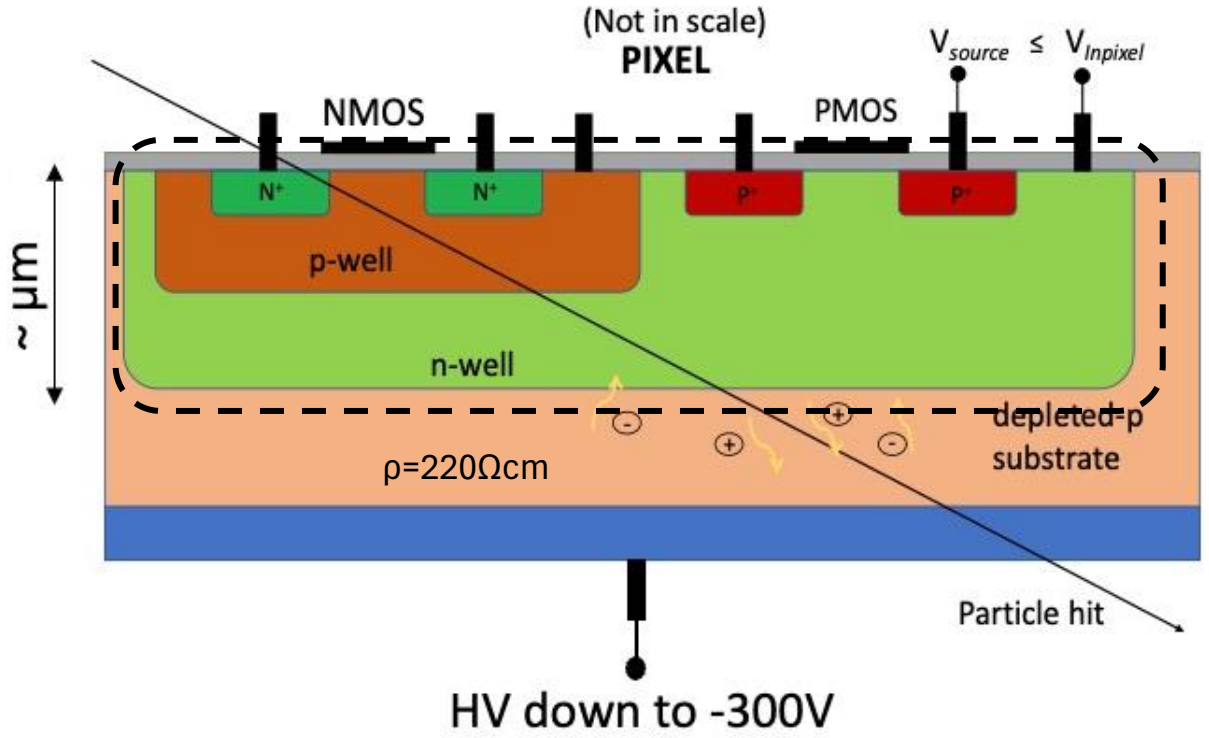
- Deep n-well hexagonal pixels



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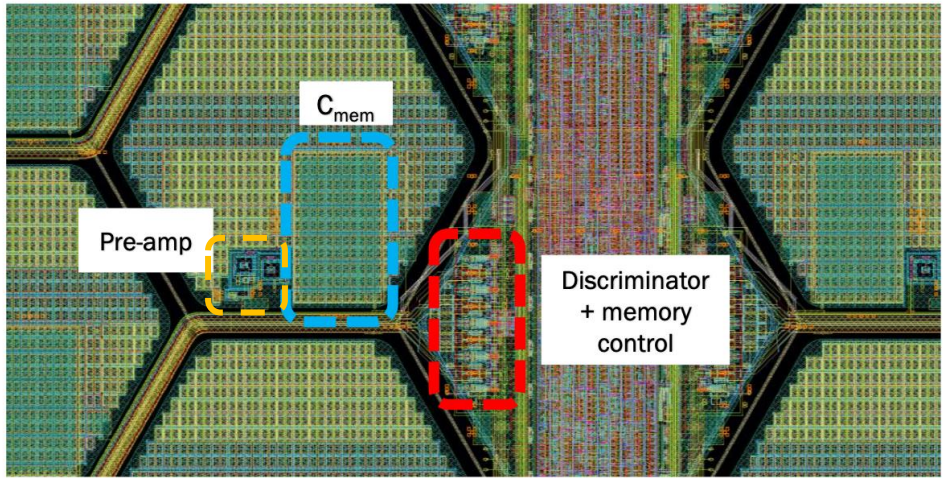
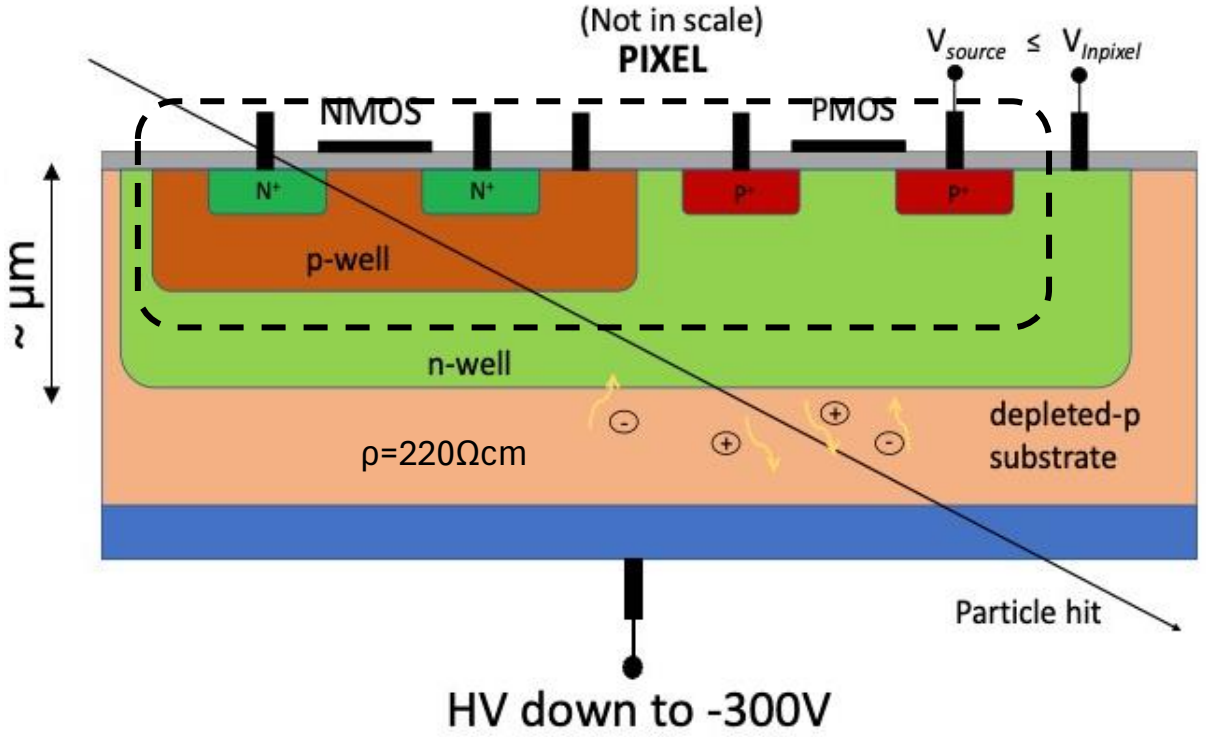
- Deep n-well hexagonal pixels
- In-pixel front-end ($C_{iso\text{-}pwell}$ = 183 fF)





ASIC Specifications

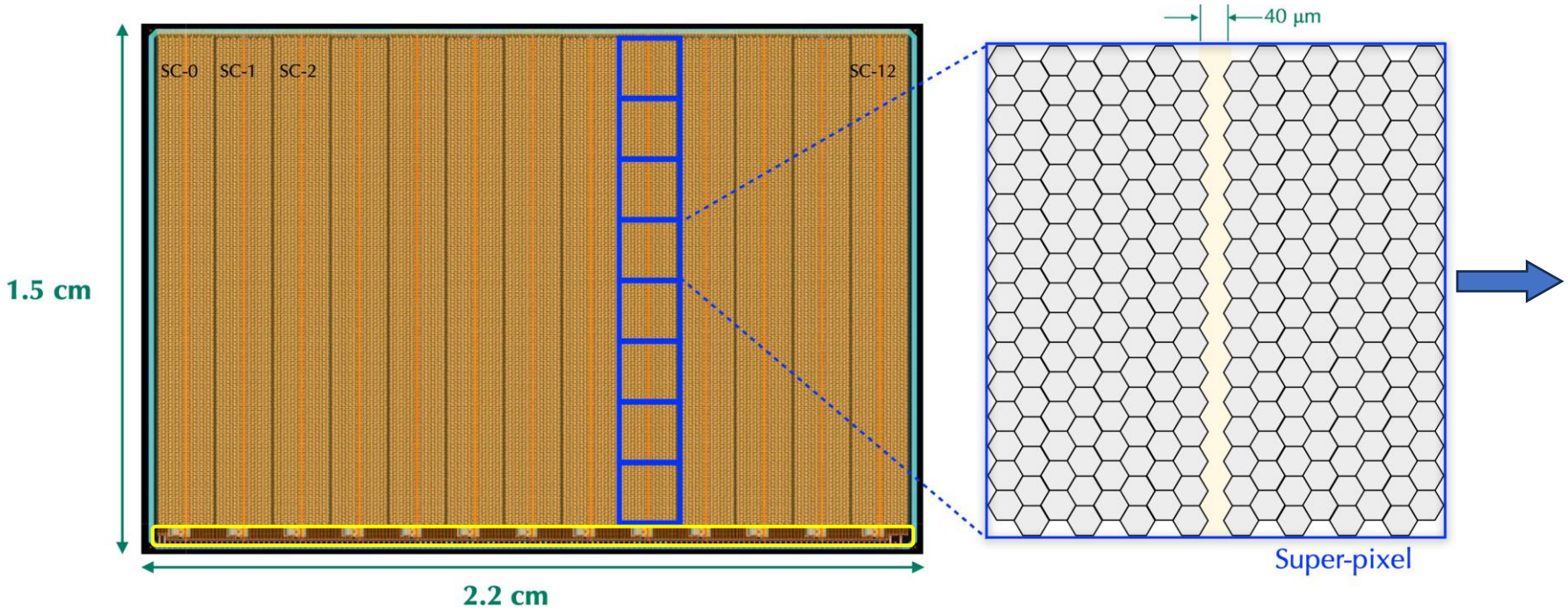
ASIC specs	
Pixel Size	65 µm side (hexagonal)
Time resolution	< 1 ns
Event size	from 1 pixel to 2000 pixels
Event readout time	$\lesssim$ 200 µs
Background readout time	$\lesssim$ 10 µs
Pixel charge information	0.5 fC to 65 fC
Pixel ENC	< 200 e- (0.032 fC)
Power consumption	< 150 mW/cm^2

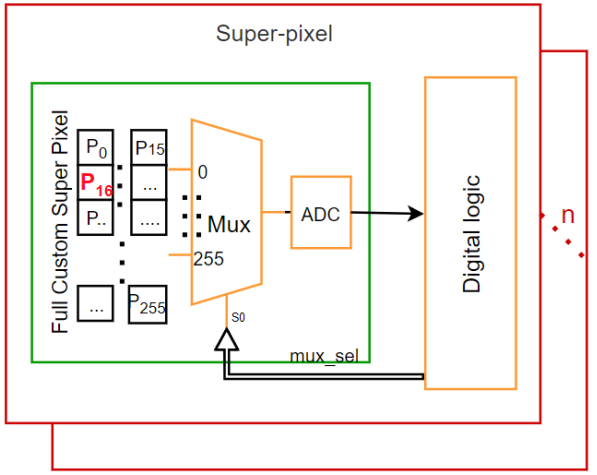
Chip Architecture

Full-reticle chip divided in 13 “super-column” with:

- Active region, subdivided into 8 “super-pixels” of 16x16 pixels
- Digital column (40 µm thick) in the middle with distributed logic for masking and readout

Digital periphery at the bottom for configuration and readout

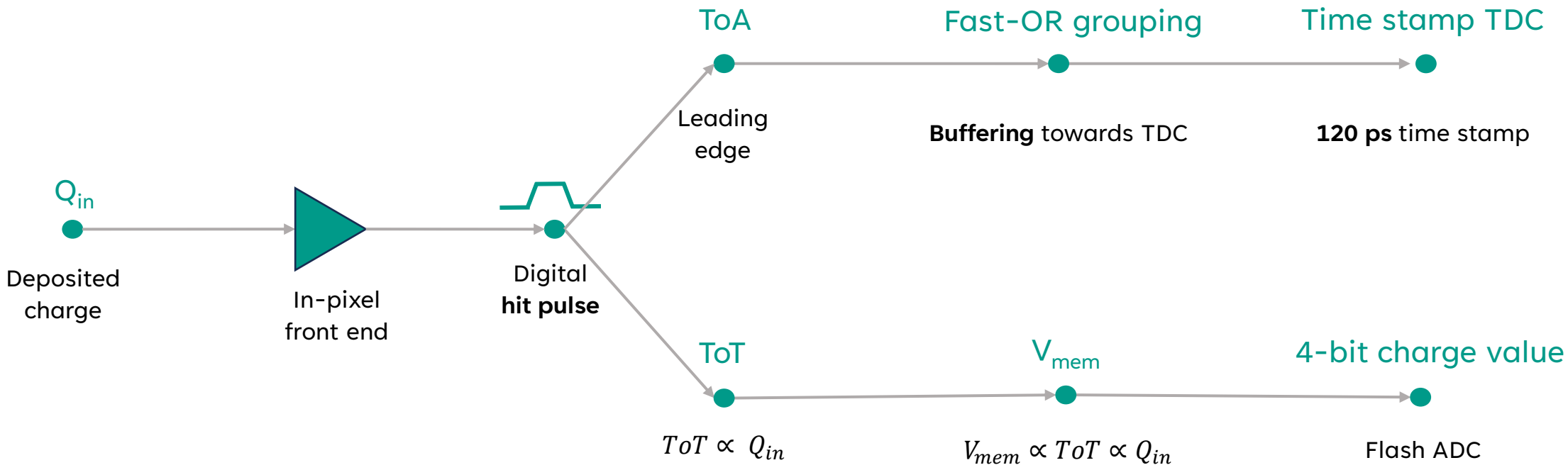




Super-pixel:

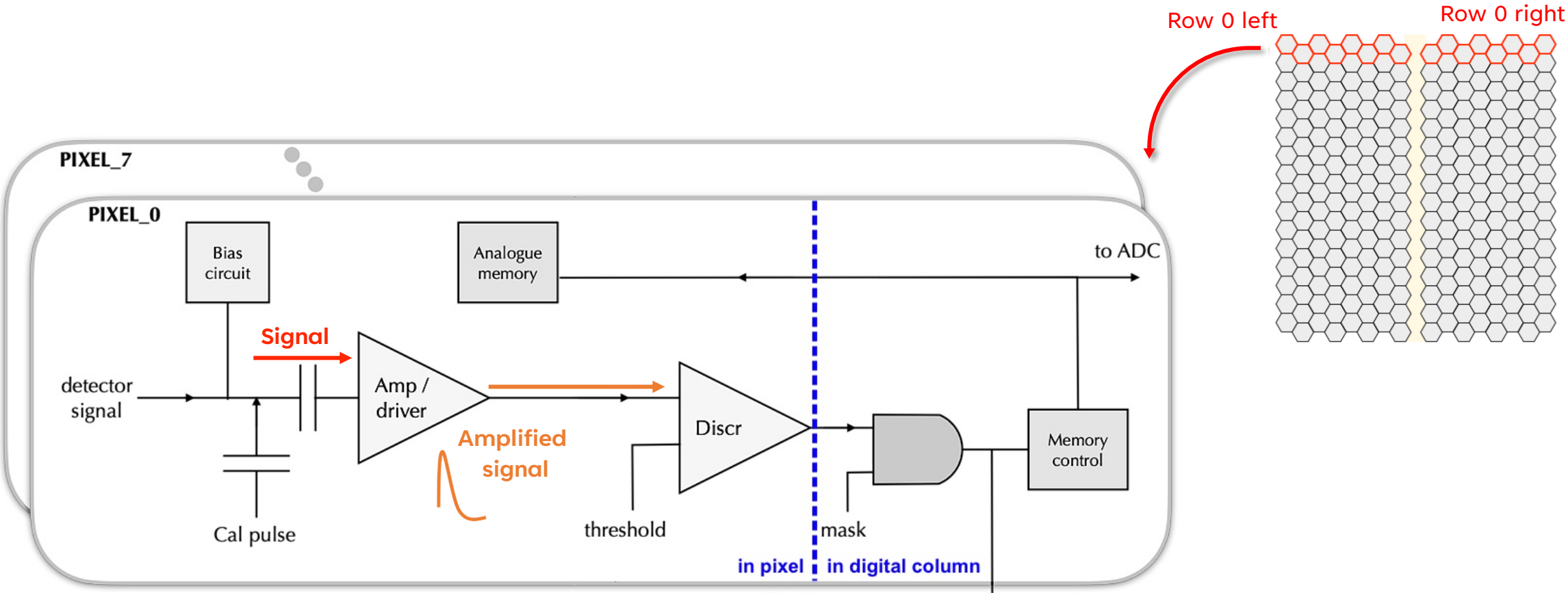
- 16 rows with 8+8 pixels
- Analogue 256-to-1 MUX
- 4-bit flash ADC
- 3 fast-OR lines
- Local biasing
- Masking logic

Charge and Time Measurements



Pixel circuitry

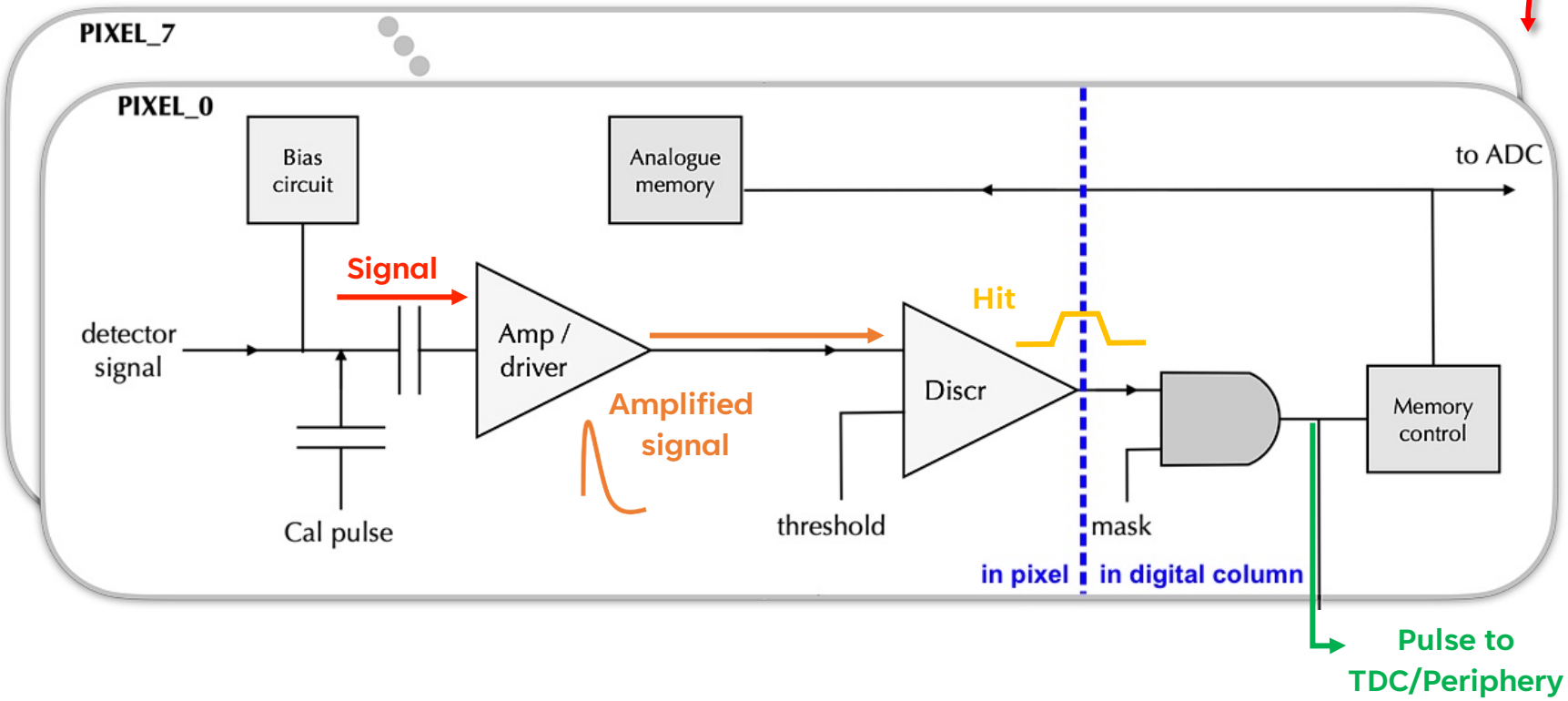
Charge measured per-pixel

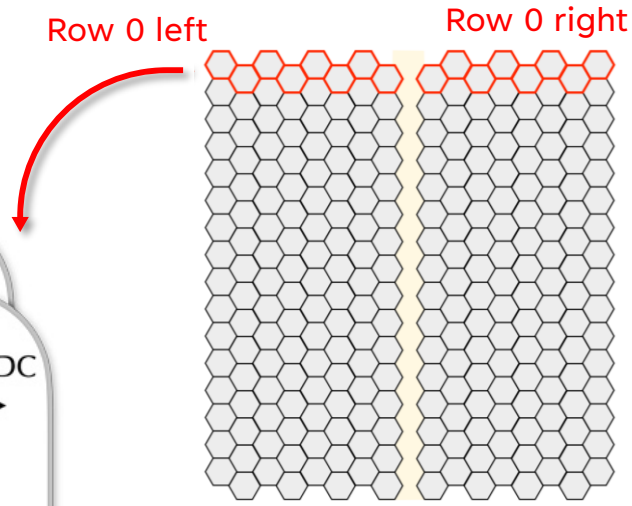


Pixel circuitry

Charge measured per-pixel

- **Hit** above threshold generates **signal** buffered to the periphery through fast-OR tree

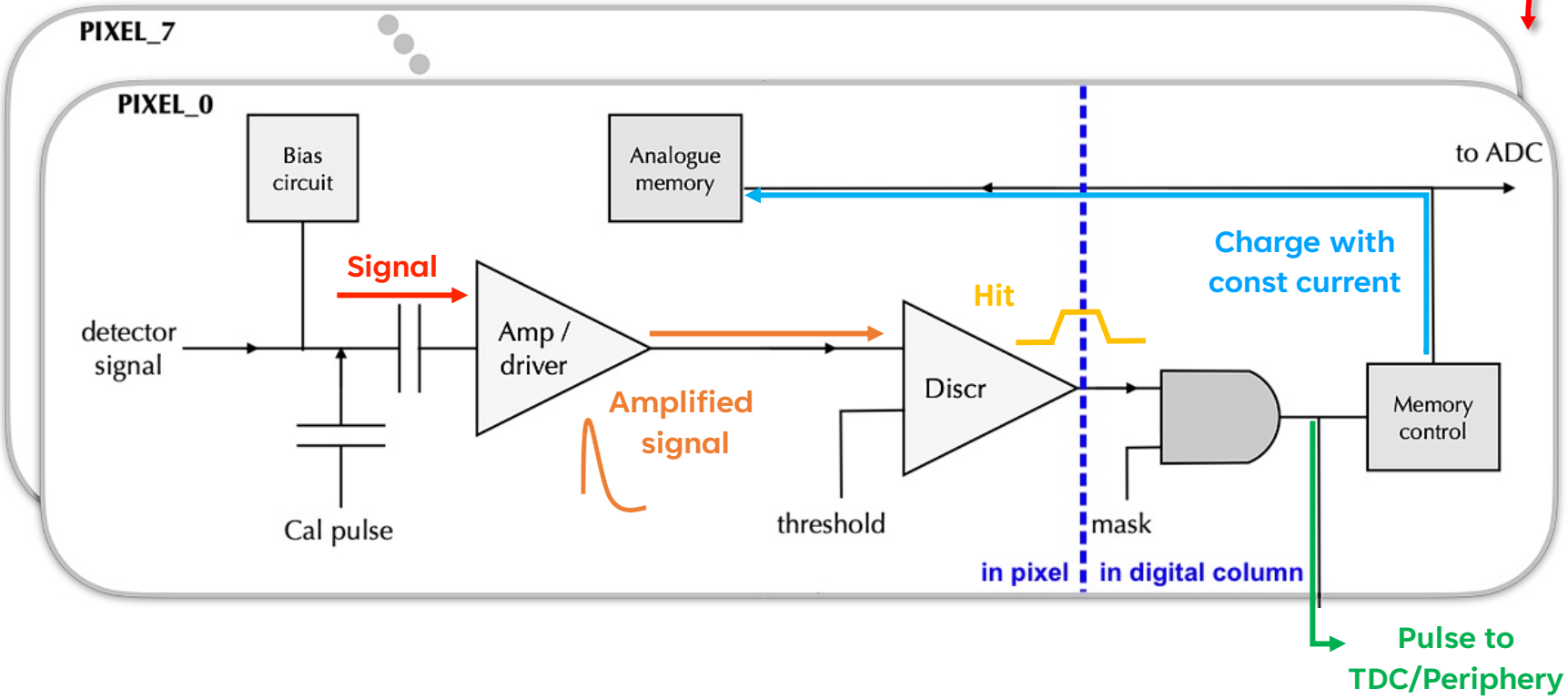


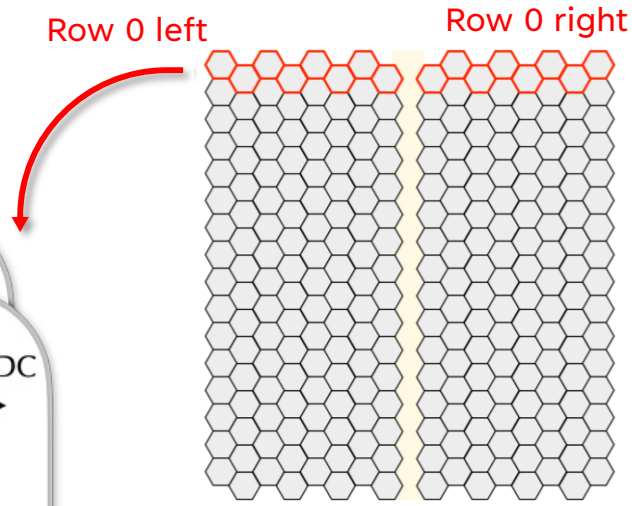


Pixel circuitry

Charge measured per-pixel

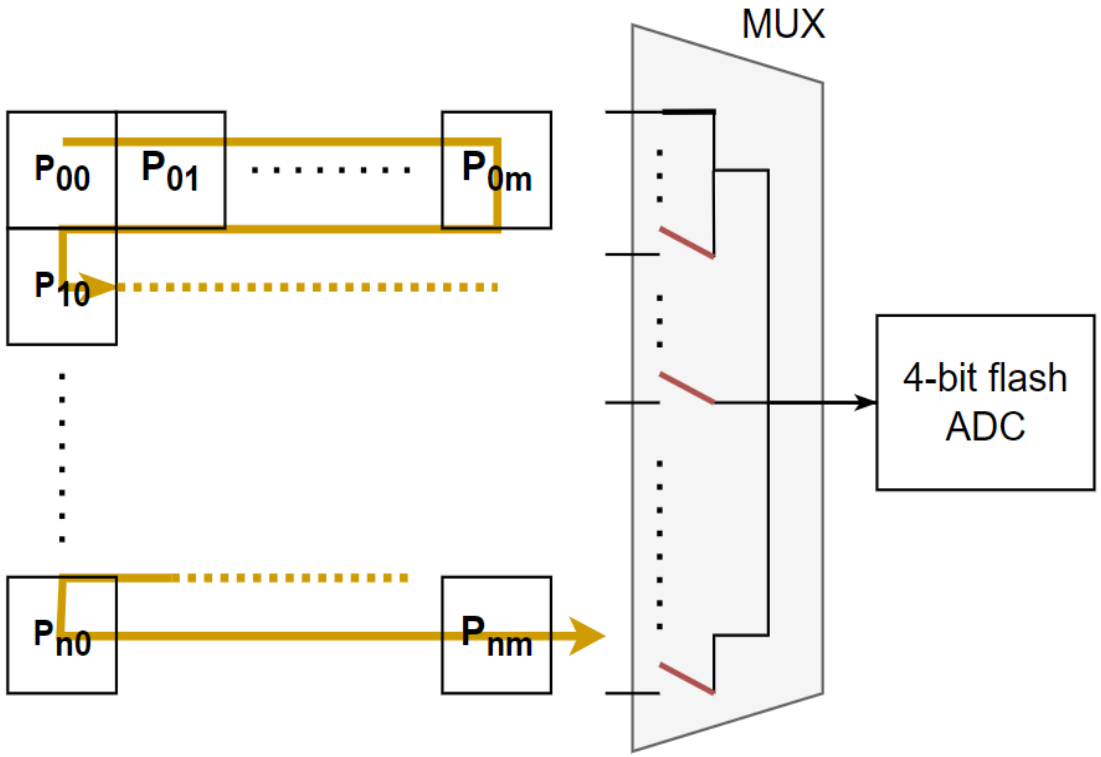
- **Hit** above threshold generates **signal** buffered to the periphery through fast-OR tree
- A **charge** proportional to the ToT is stored into pixel's analogue memory





Pixel polling scheme

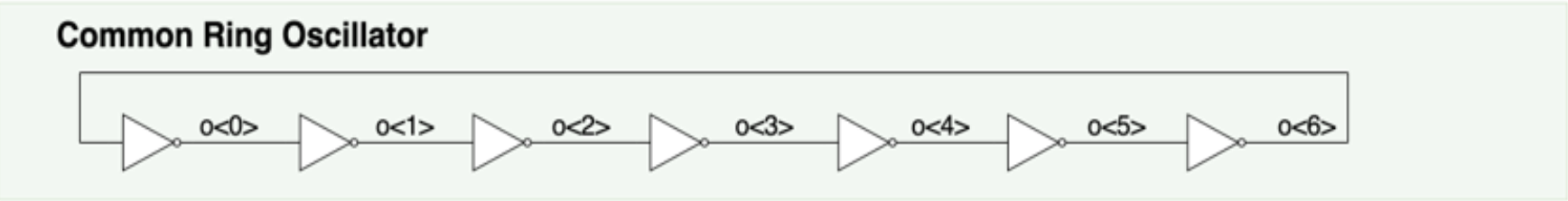
- **Local 4-bit flash ADC** housed in the inactive region in the middle of each super-pixel
- **1 ADC** per super-pixel, **shared** for all its pixels
- An **analogue MUX** scans the super-pixel, connecting one pixel at a time to the ADC during readout.

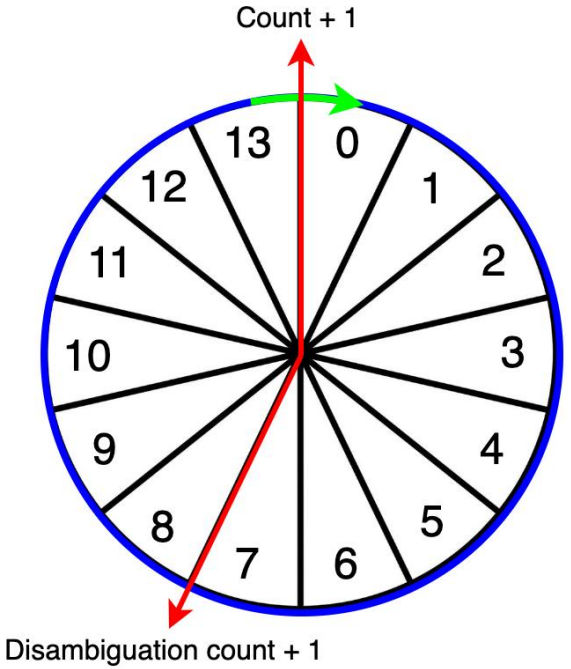


Pixels scanning in a single frame

Time-to-Digital Converter

- 1 TDC per super-column
- Each with a shared, 7-stages**, free-running ring oscillator** with **calibration**
- **24 channels** + 1 calibration channel
- Power consumption ~ 7.68 mW (0.36 mW in power saving mode)





- **Coarse time** counter on ↑ o<0>
- **Fine time** encoding oscillator states gives the LSB
- **Disambiguation** on ↑ o<1> (in anti-phase, checked for fine time 13 and 0 to avoid an error of full period T)

$$LSB\ \Delta T = \frac{T}{2N}$$

Design parameters:
N = 7
T = 2.1 ns
ΔT = 117 ps (measured)

Packet- vs Frame-Based Readout

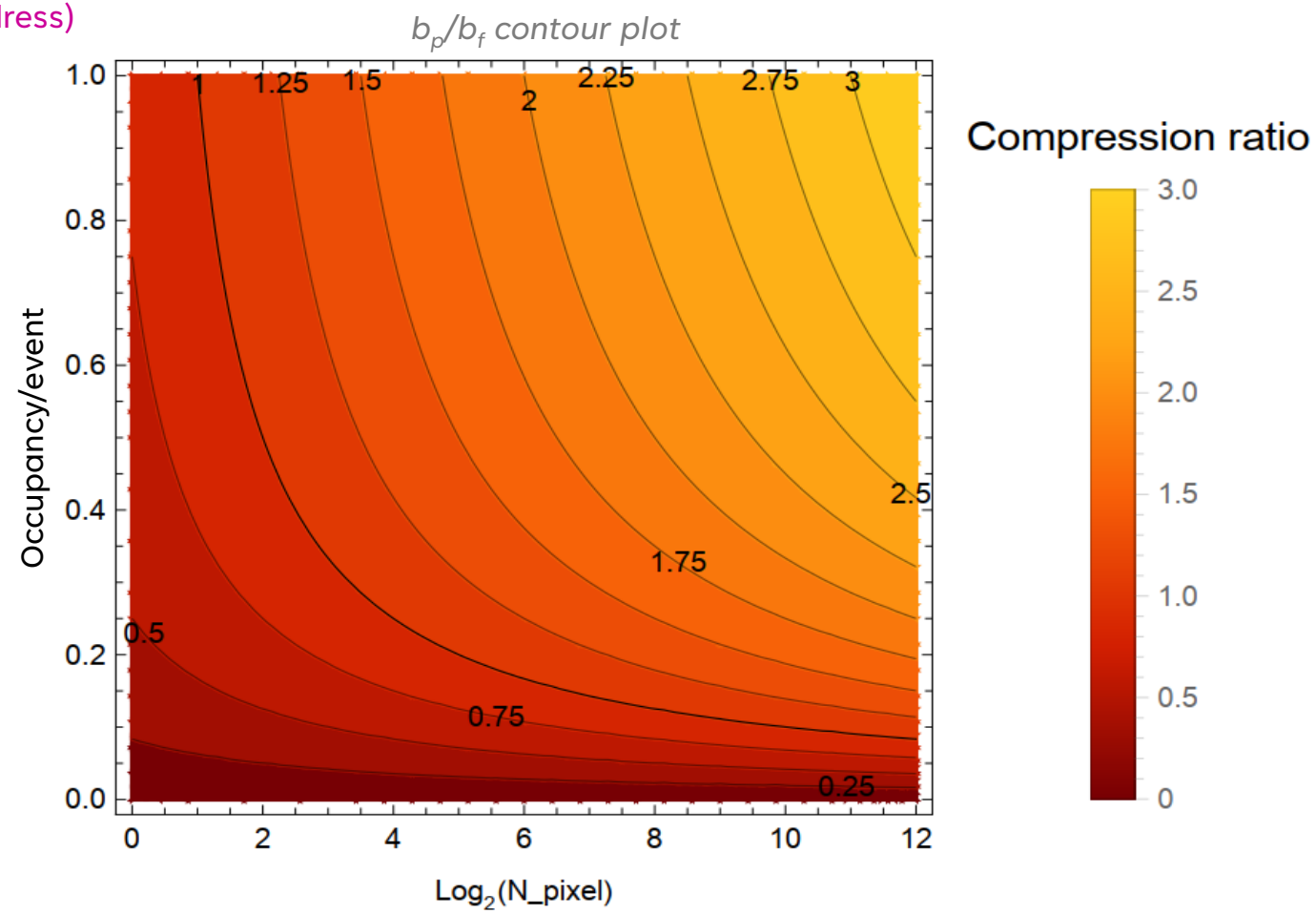
Hit pixels — Data bits (i from ADC + address)

$$b_p = N_{pixel} \cdot occupancy \cdot (i + \log_2(N_{pixel}))$$

$$b_f = N_{pixel} \cdot (1 + occupancy \cdot i)$$

Hit flag — ADC data for hit pixels

$$Compression\ ratio = b_p/b_f$$



C. A. Fenoglio et al. "A Scalable Frame-Based Readout Architecture for Monolithic Pixel Detectors with Local ADC and Time Digitization," 2023 18th Conference on Ph.D Research in Microelectronics and Electronics (PRIME), Valencia, Spain, 2023, pp. 89-92, doi: 10.1109/PRIME58259.2023.10161814.

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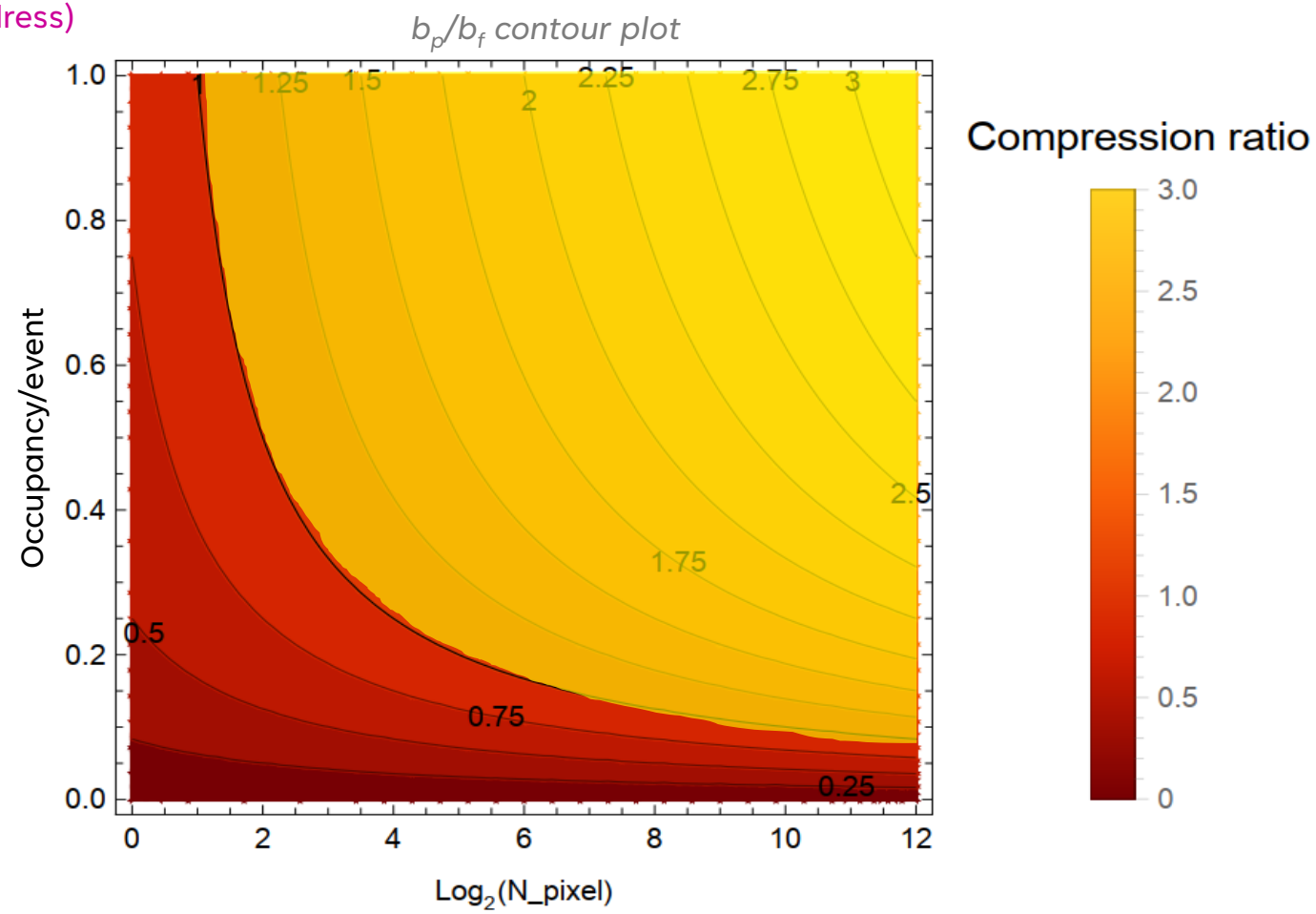

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Pixels

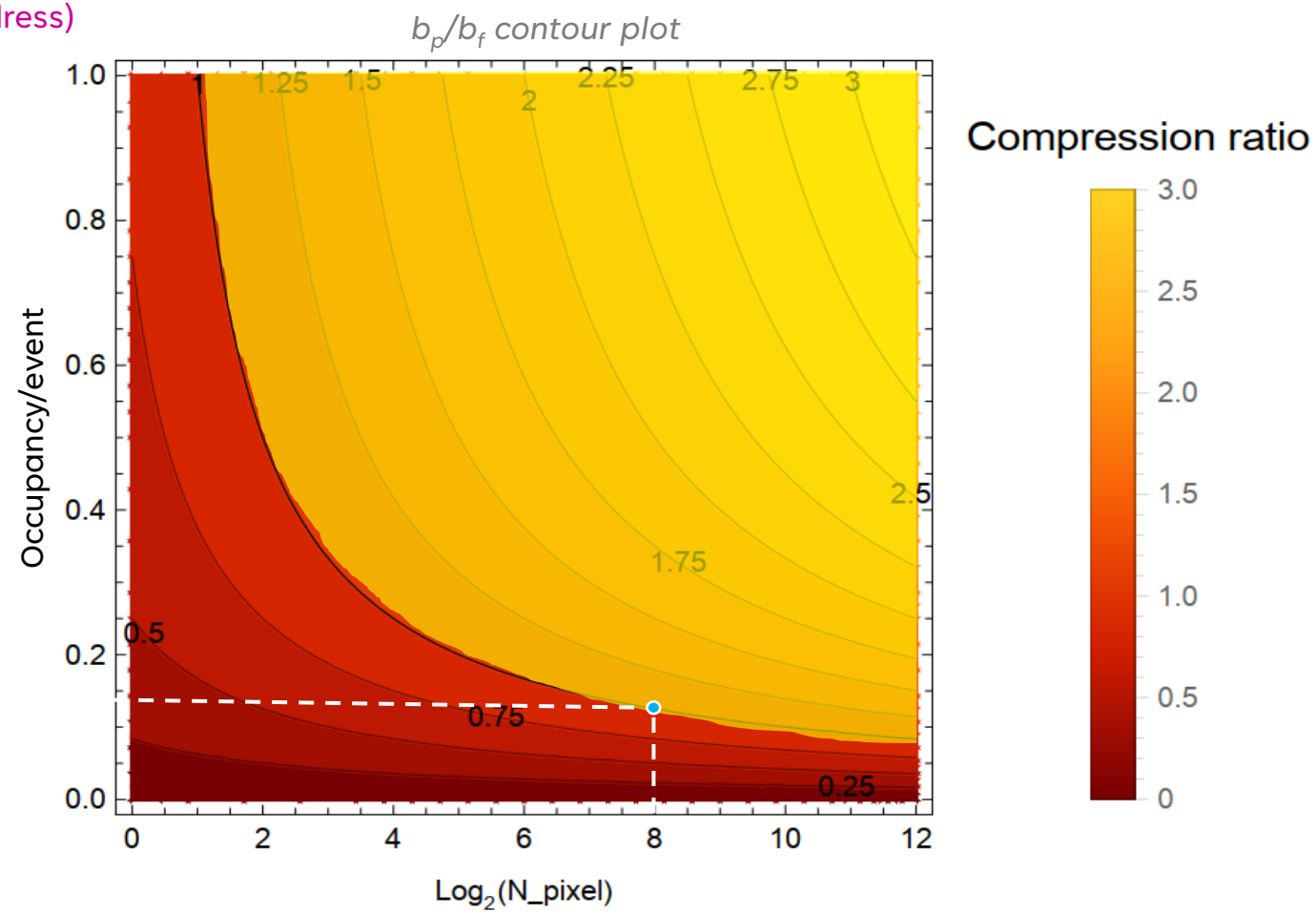
256

Super-pixel size in FASER design

Occupancy

12%

Lower occupancy limit convenient for frame readout



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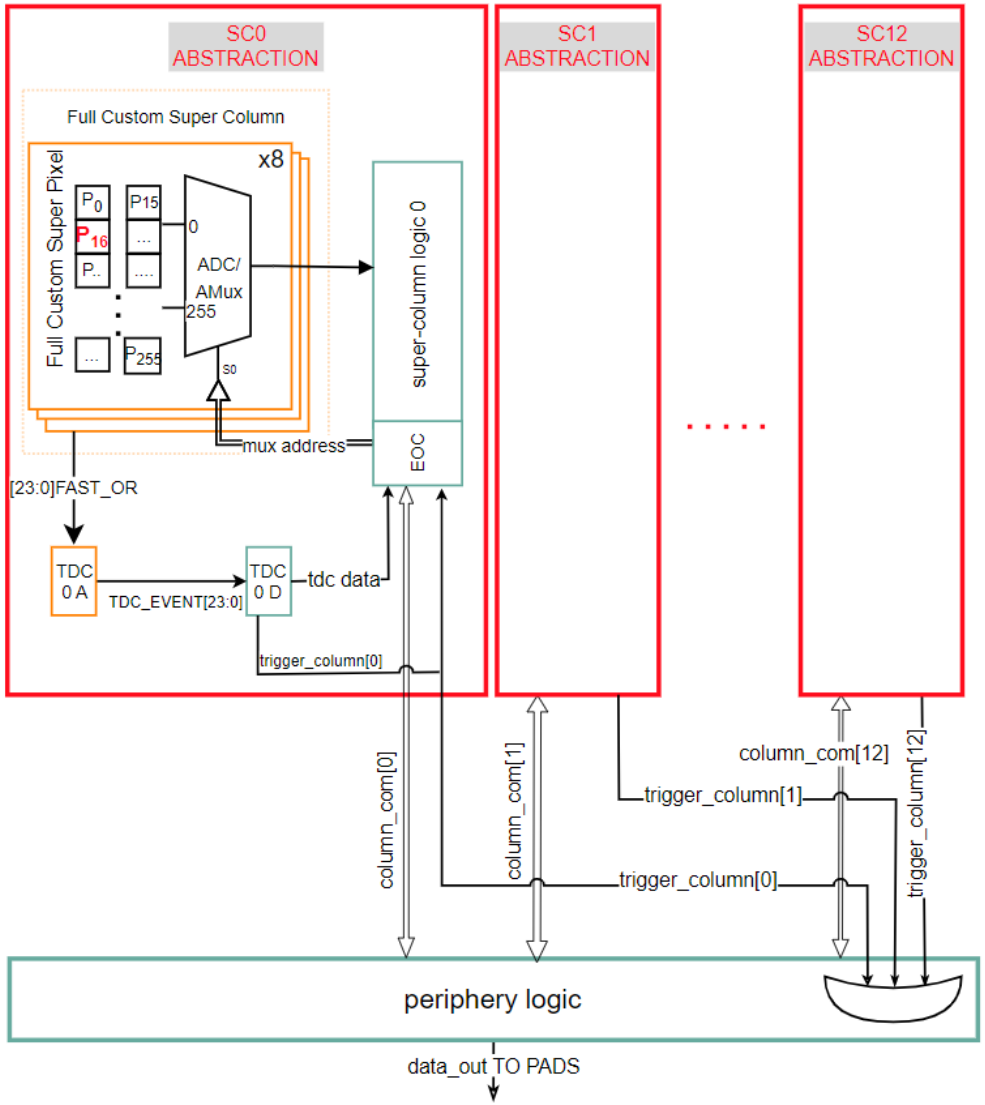
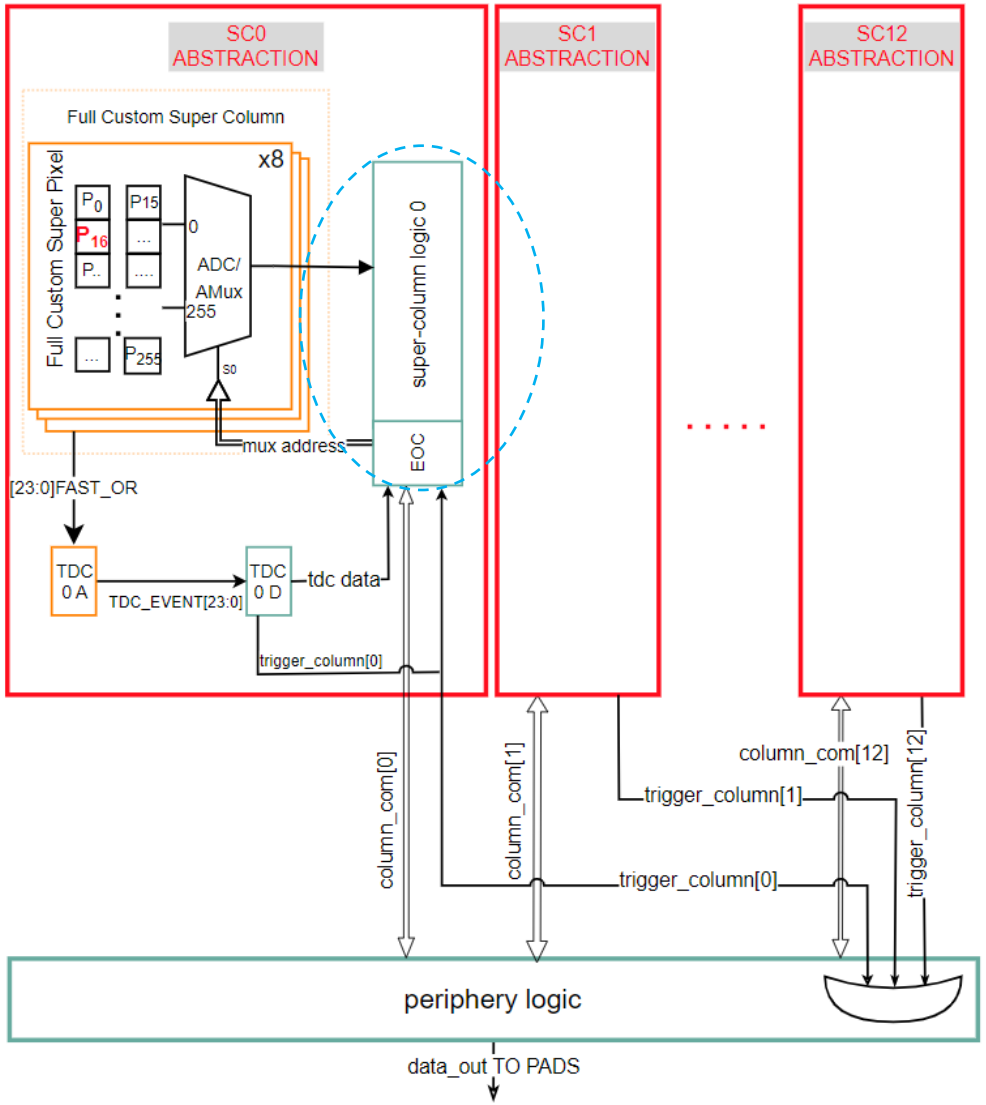
Readout Architecture



Frame-based, event-driven readout:

- After a hit, a snapshot of the matrix is taken
- *Non-continuous readout* of all the pixels at 200 Mbps
- Dead time (~ us to 200 us depending on event occupancy)
- More like an **image sensor** than a HEP tracker

Readout Architecture



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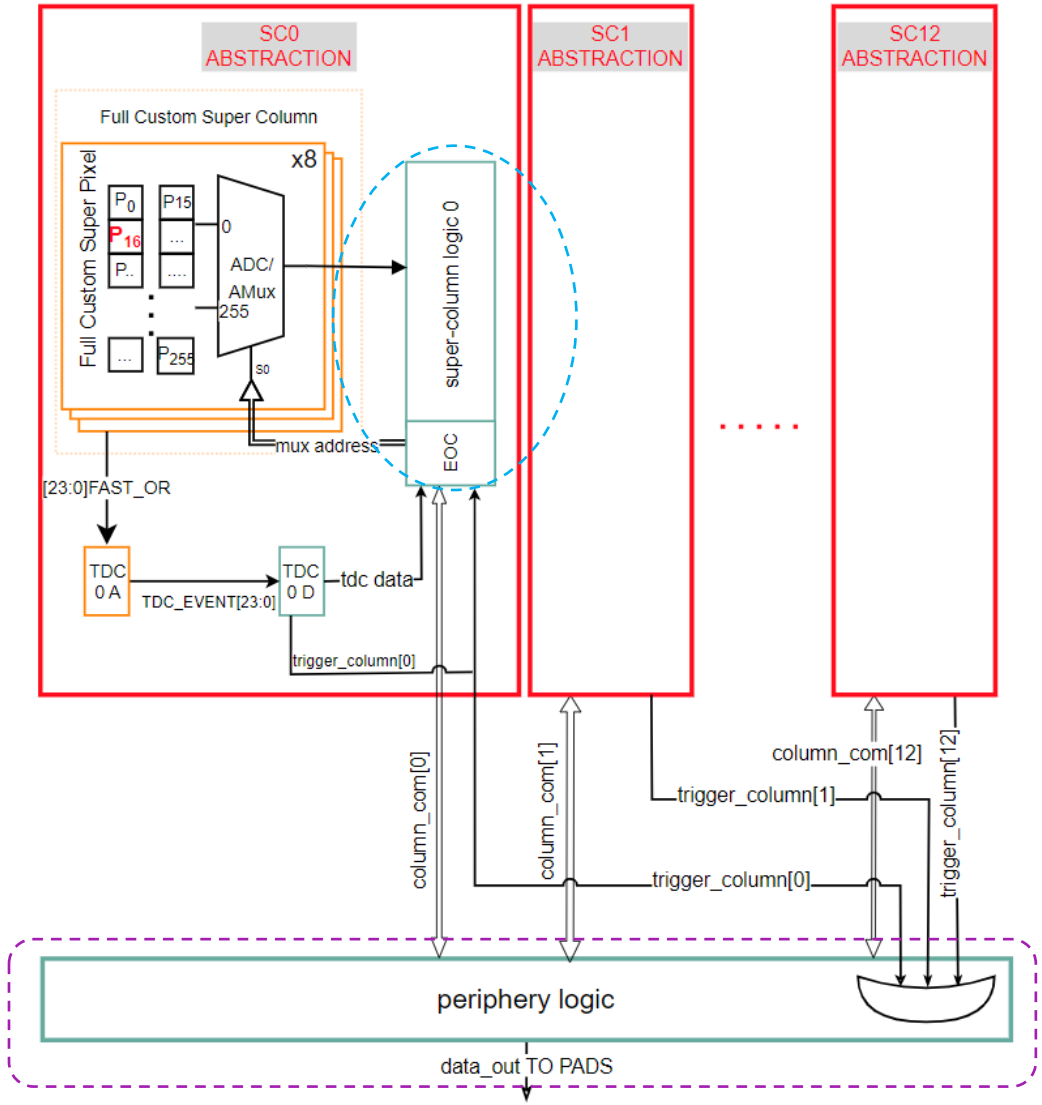
Distributed control logic inside the matrix:

- Each super-pixel is readout in **parallel** by a standalone processing unit
- **Groups** the bits and sends them to the periphery logic
- Performs **zero suppression** at pixel level

Readout Architecture



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Periphery control logic at the bottom:

- Controls the **frame-based** readout
- Reads one super-column after the other acting as **arbiter**
- Performs empty columns **data suppression**

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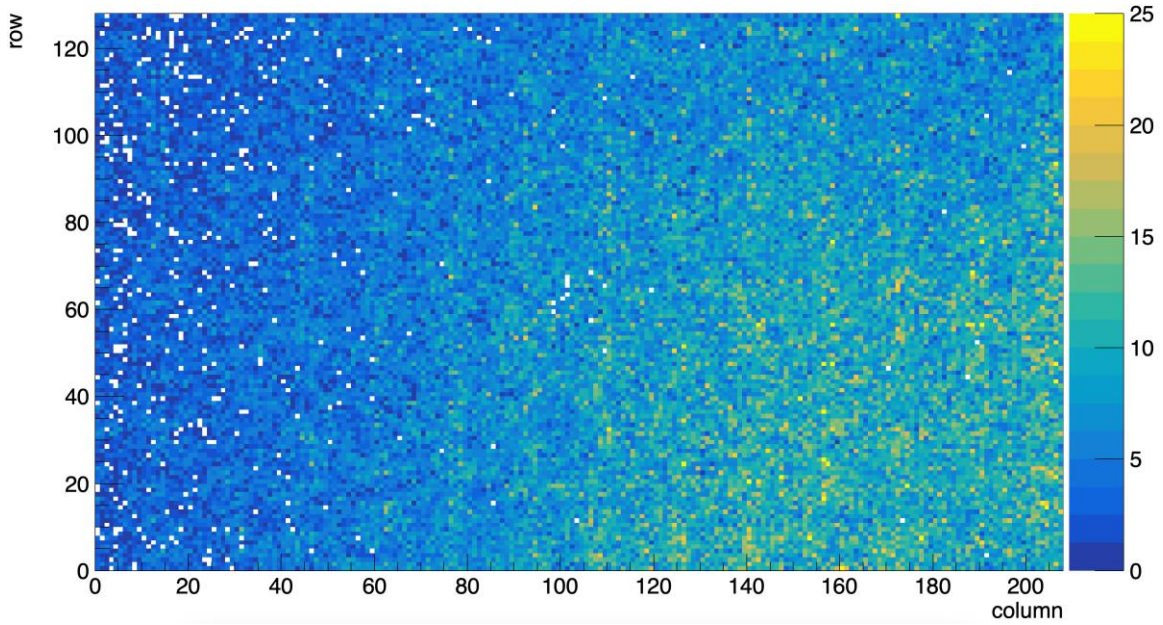
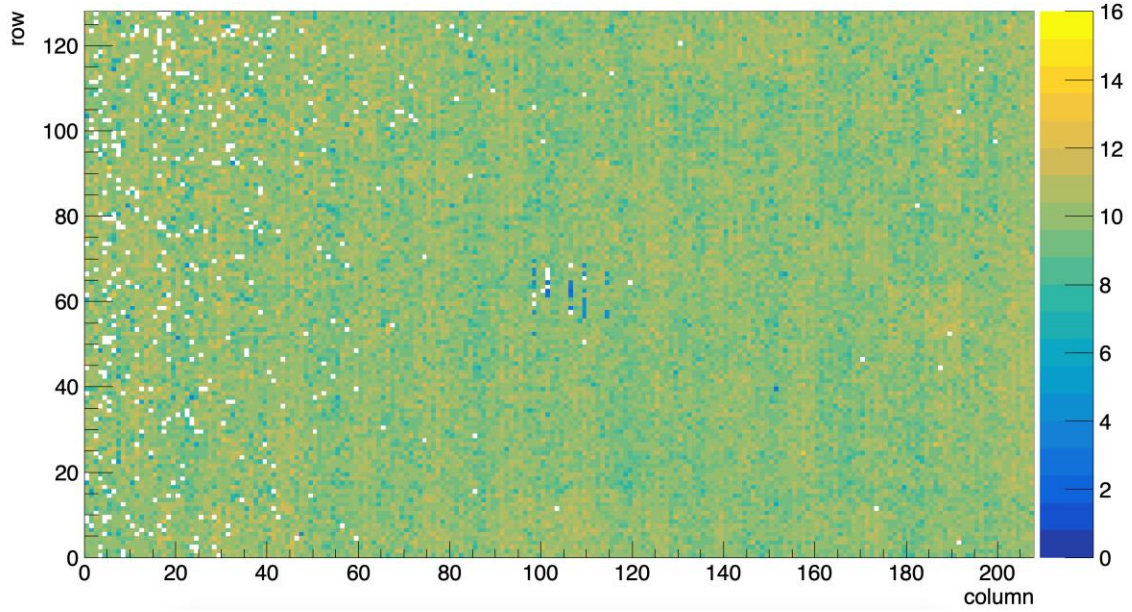
Sr90 Measurement

Sr^{90} Hit-map



Sr^{90} Charge



Not calibrated!

Pre-Production Prototype

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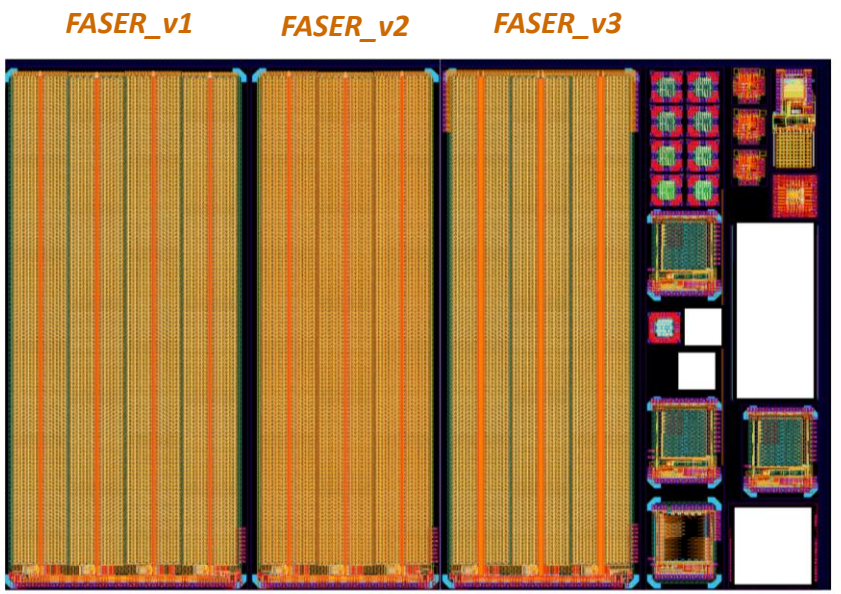
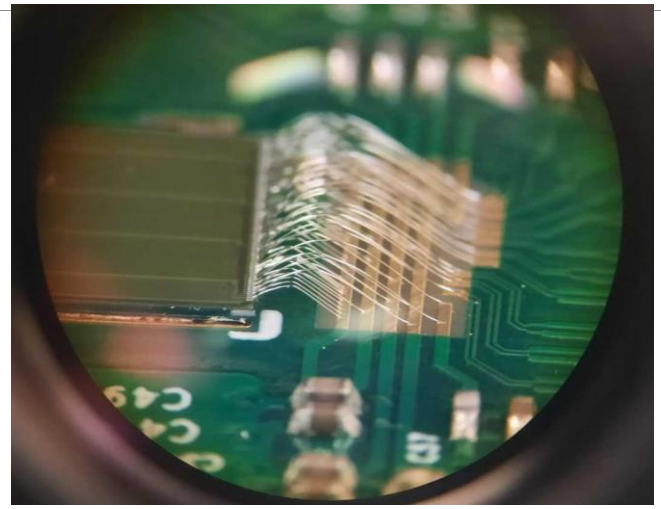
Main Fixes from Pre-Production

- Fix on memory leakage
- Improved FE : resizing to improve mismatch.
- Improved FE : removed Post-amp -> operation at higher gain
- Power-on reset
- Default configuration at power-on (not for masking)
- Allow readout when pixel always firing
- Readback configuration
- Readout at 200 MHz (not achieved in pre-production)
- Fix on output data stream + multiple header for easier reconstruction.
- Fix on TDC reset (absent in pre-production)





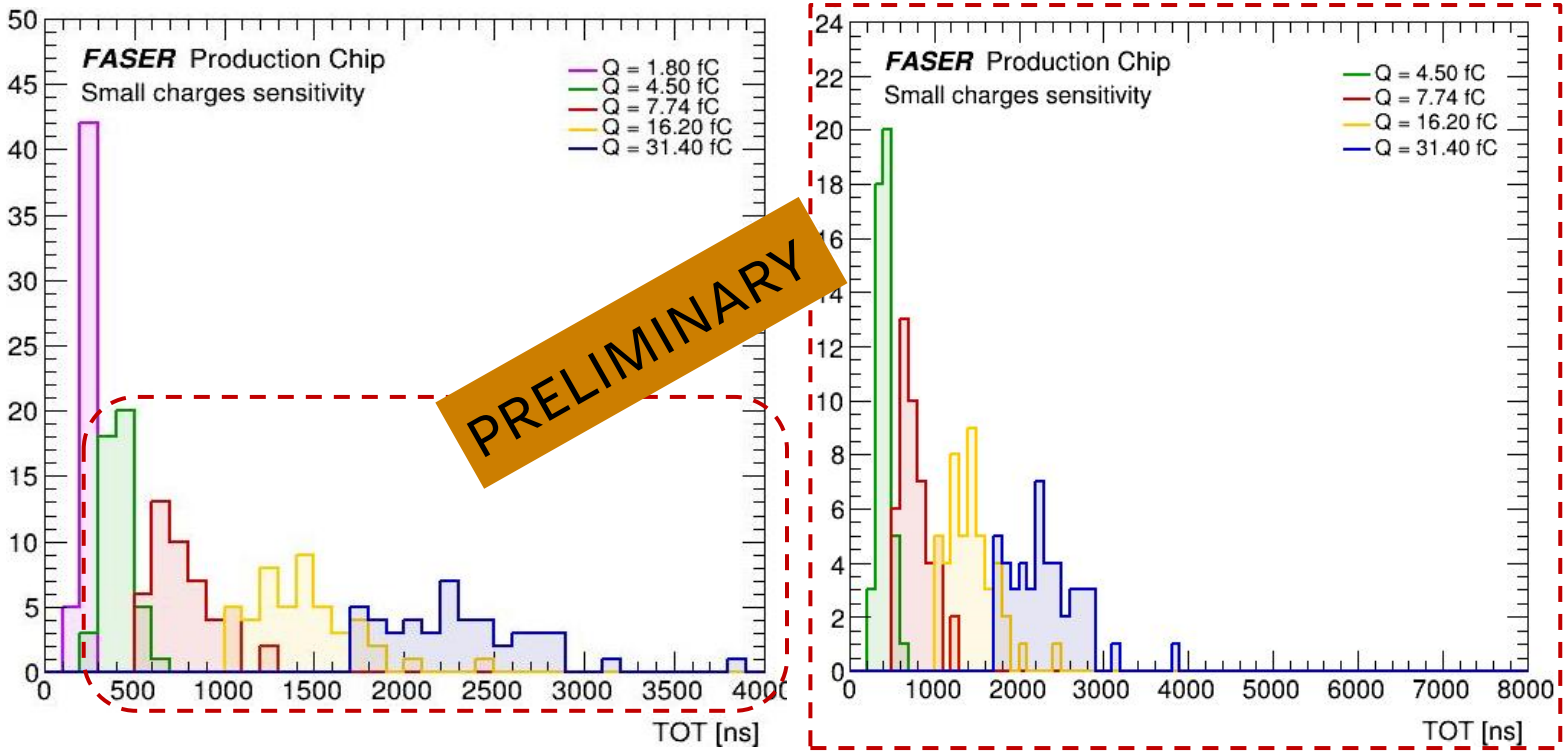
Mismatch studies

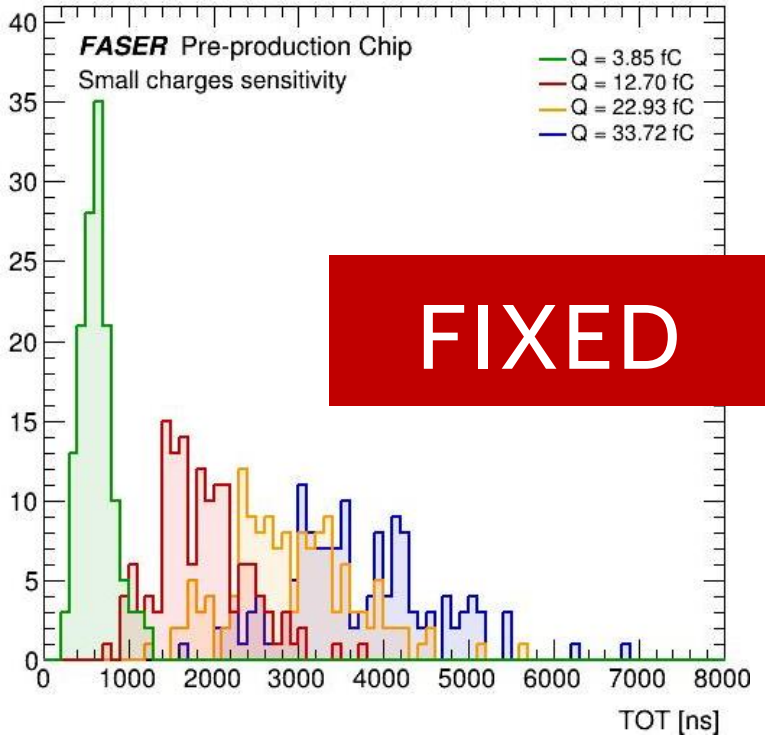
Production Chip:

Small charges are properly discriminated

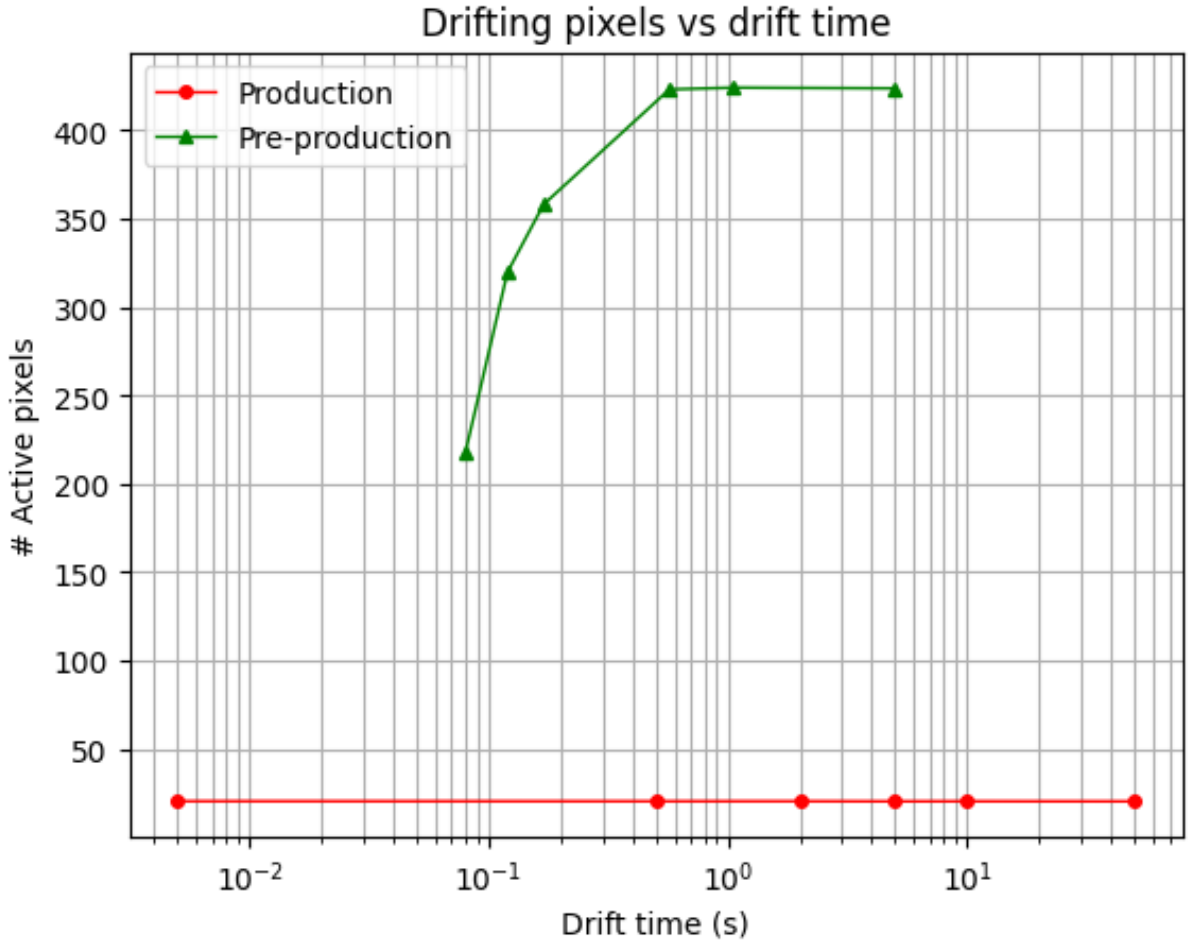
Pre-Production Chip:

Peaks are not well separated





Memory drift



Analogue memories **leakage** could modify the memory value:

➔ Fake hits in the ADC data

➔ The higher the drift time, the more visible the effect, the more fake active pixels

➔ Need to operate at high rates

Fix is working and the problem is solved in Production ASIC

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Summary and Outlook

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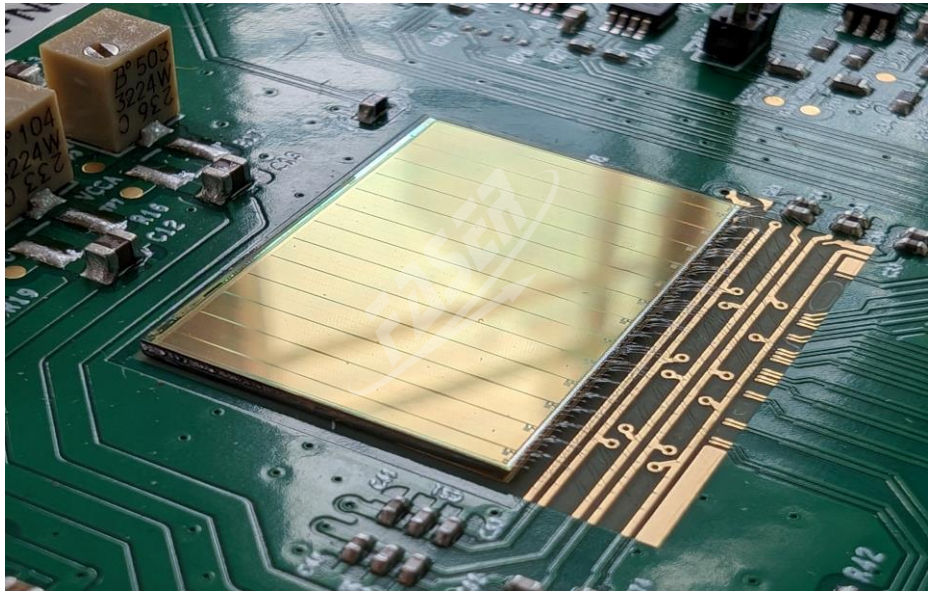
New FASER preshower ASIC

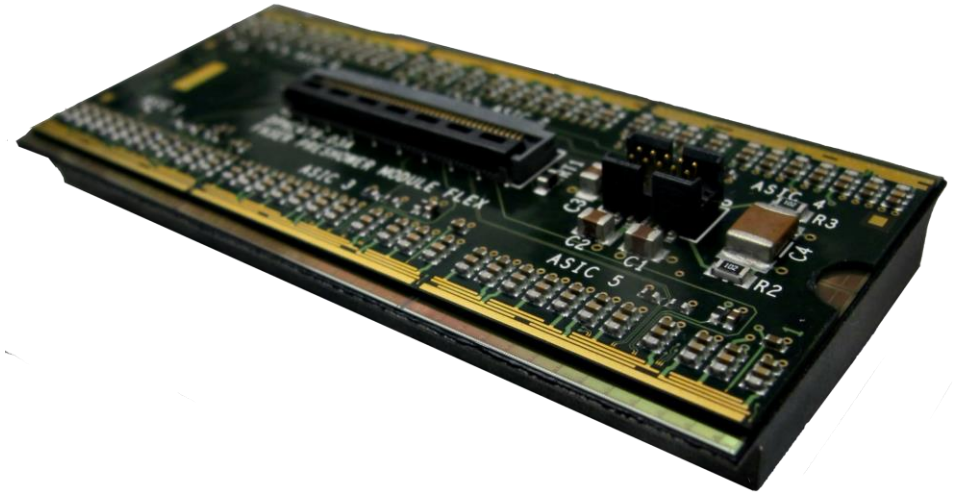
- Full-reticle imaging chip
- Fast charge and time measurement
- Optimized readout

ASIC preliminary validation

- Implemented fixes from prototype work
- Final test beam next week to validate the whole detector system

→ **Ready and hopeful for the detector installation in December 2024**





Acknowledgments and collaboration

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ASIC design team

Lorenzo Paolozzi
- Sensor design
- Analog electronics

Roberto Cardella
- Analog/Dig electronics

Thanushan Kugathasan
- Analog electronics

Jordi Sabater Iglesias
- Sensor design

Carlo Alberto Fenoglio
- Digital electronics
- ASIC test

Antonio Picardi
- Analog electronics

Luca Iodice
- Analog electronics

Pierpaolo Valerio
- Former member

Fulvio Martinelli
- Former member

FASER collaboration:
99 collaborators, 27 institutions, 11 countries

Backup

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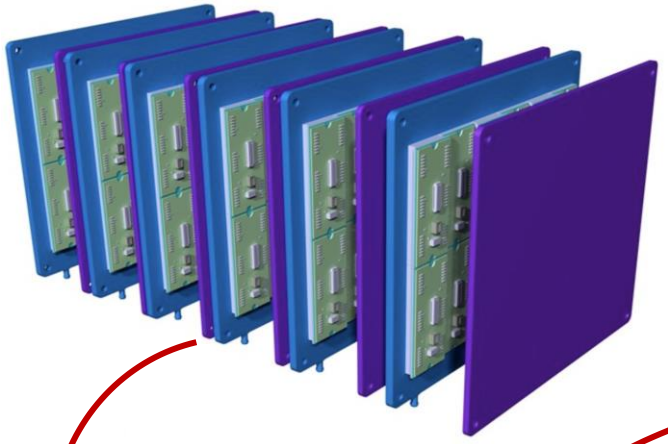
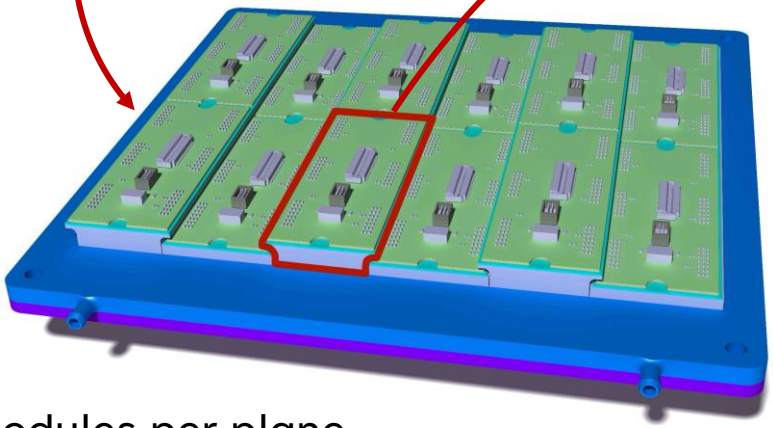
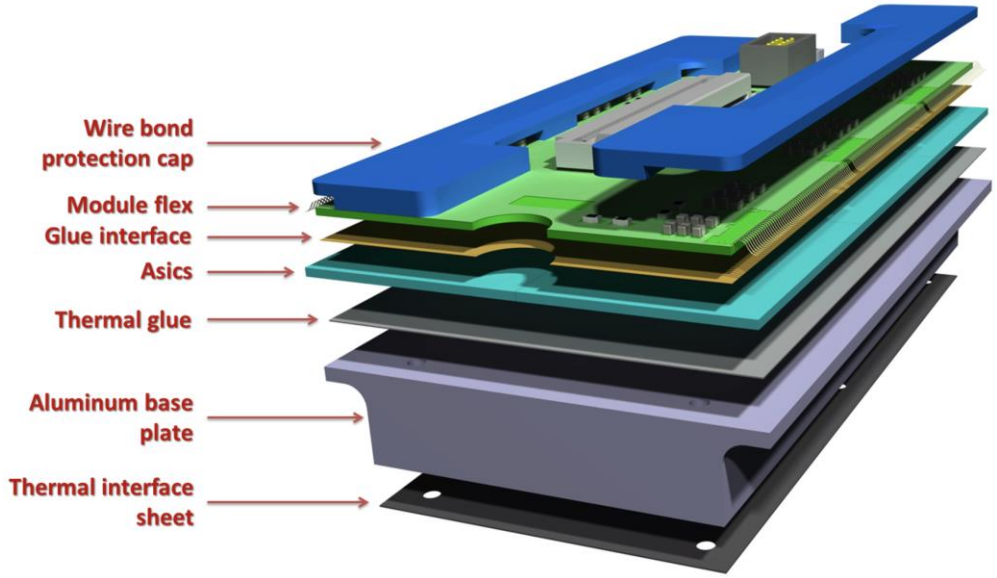
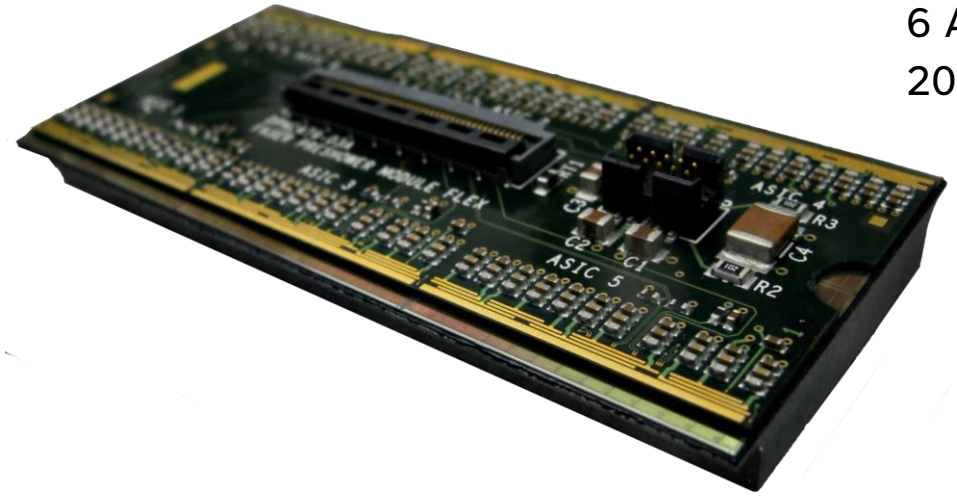
Preshower Detector Upgrade – 2/2





12 modules per plane





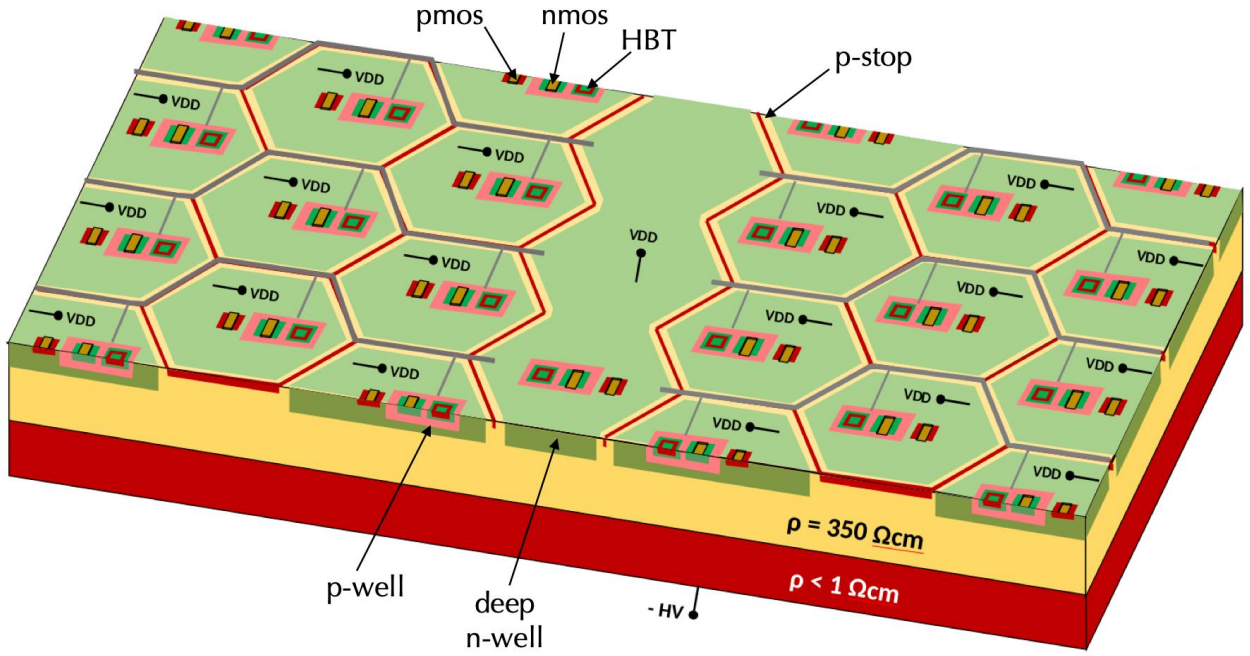
6 ASICs per module,
208x128 pixels each

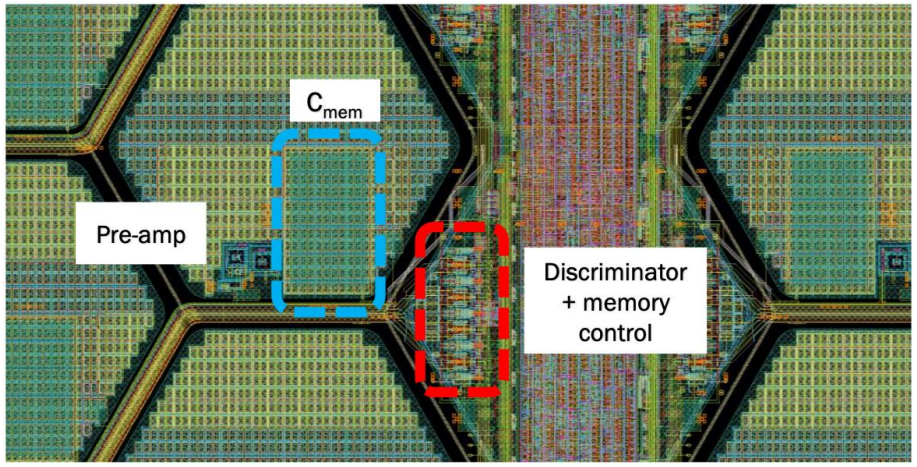
Monolithic ASIC

Monolithic active pixel sensor

130 nm SiGe BiCMOS technology (IHP SG13G2)

- High R substrate (220 Ωcm), 130 µm thick
- Deep n-well hexagonal pixels (C_{pix} = 183 fF)
- In-pixel front-end



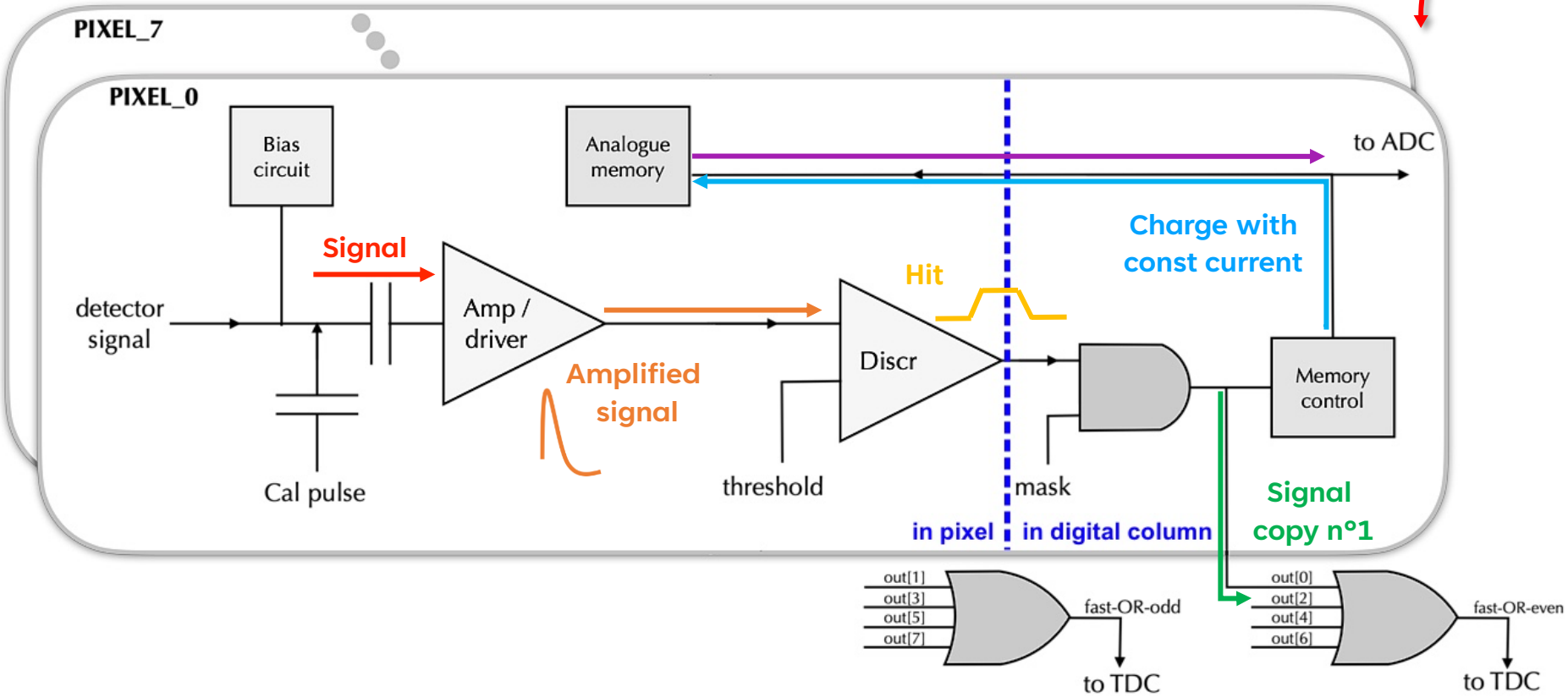


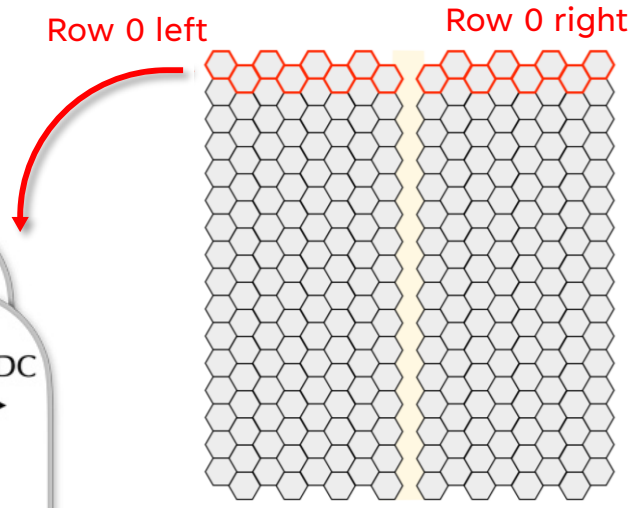
ASIC specs	
Pixel Size	65 µm side (hexagonal)
Time resolution	< 300 ps
Event size	from 1 pixel to 2000 pixels
Event readout time	≲ 200 µs
Pixel charge information	0.5 fC to 65 fC
Pixel ENC	< 200 e- (0.032 fC)
Power consumption	< 150 mW/cm^2

Pixel circuitry

Charge measured per-pixel

- **Hit** above threshold generates **signal** buffered to the periphery through fast-OR
- A **charge** proportional to the ToT is stored into pixel's analogue memory
- After a configurable delay, readout starts, the **ADC reads** each analogue memory

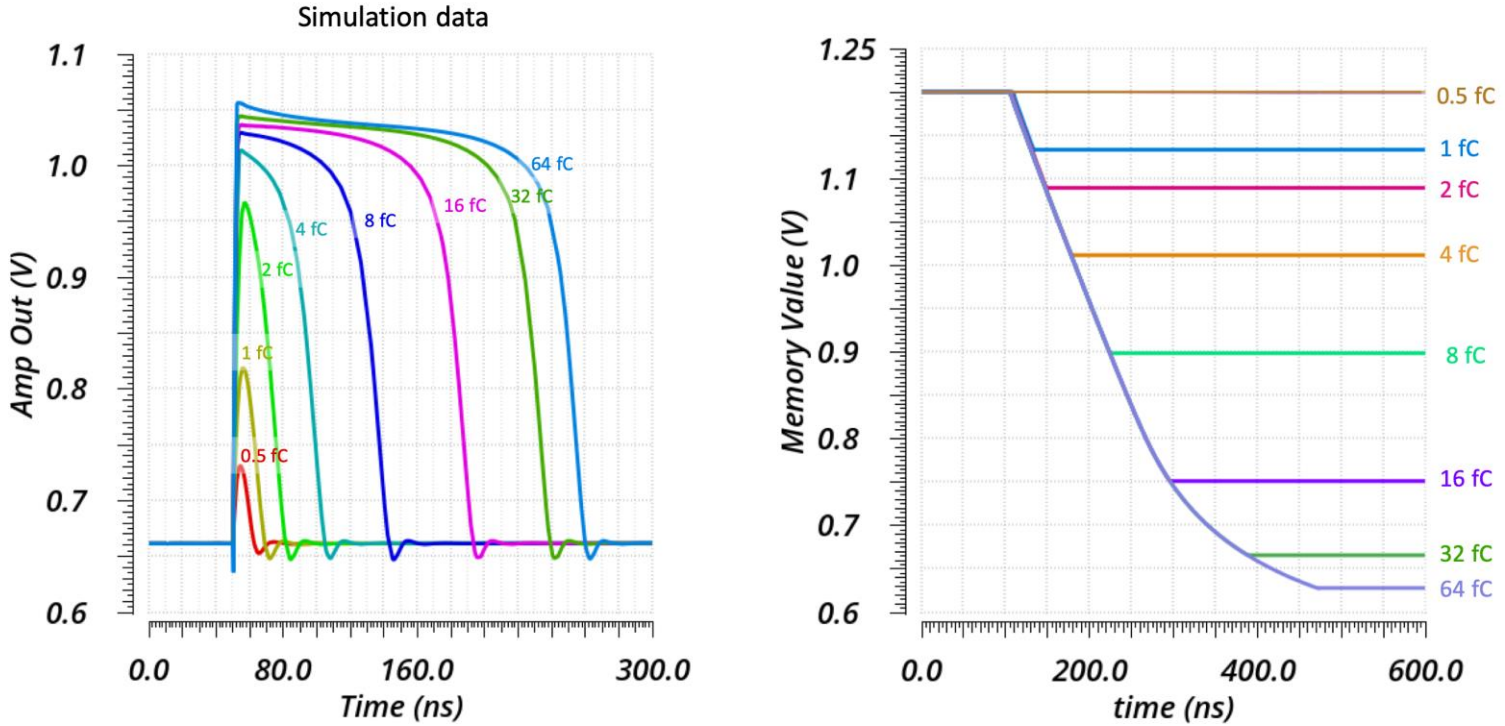




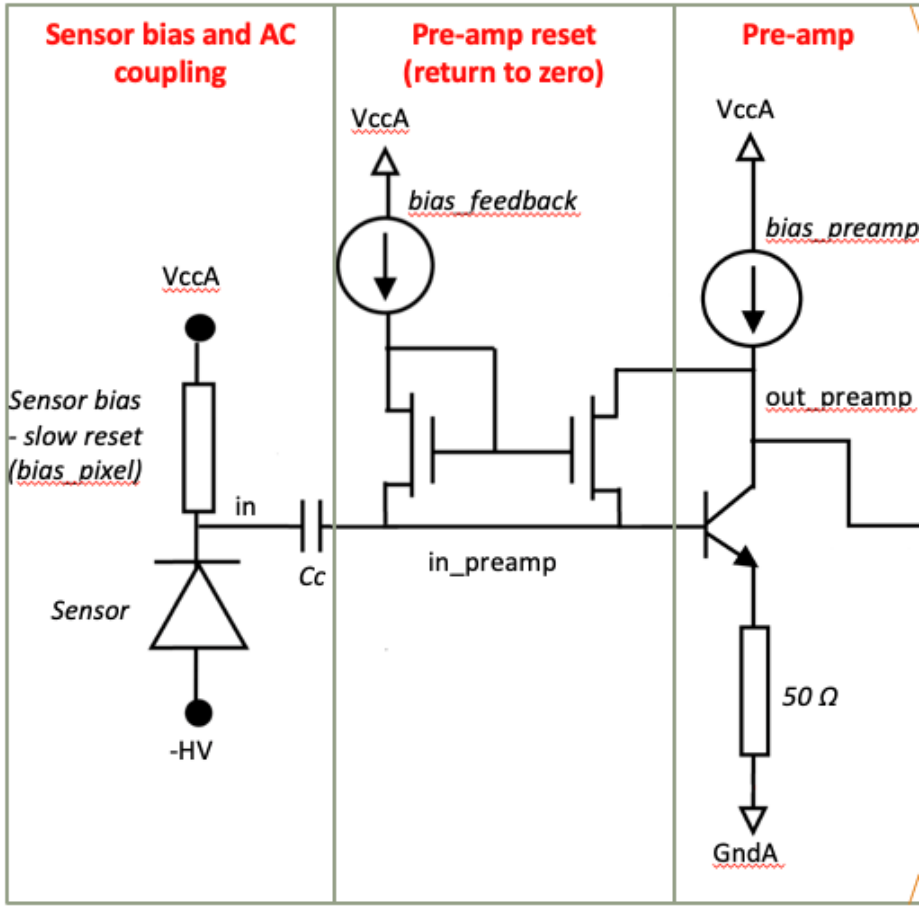
Charge Measurement

Analogue memories: capacitors inside each pixel charged with constant current during ToT

- When signal returns below threshold, memory is disconnected and left floating until the readout by the ADC
- Preamplifier designed to produce a signal proportional to the **log** of the input charge



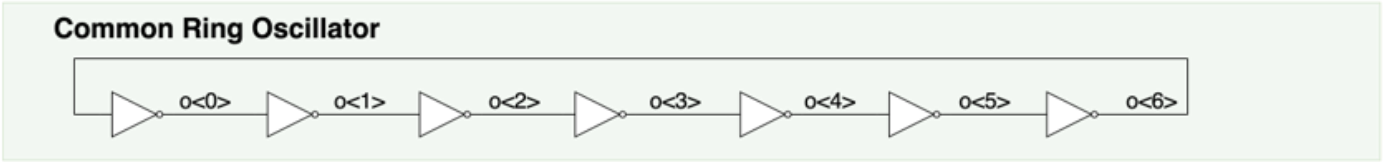
In-Pixel Front-End



Time-to-Digital Converter

Q_{in} → ToA → Fast-OR grouping → Time stamp TDC

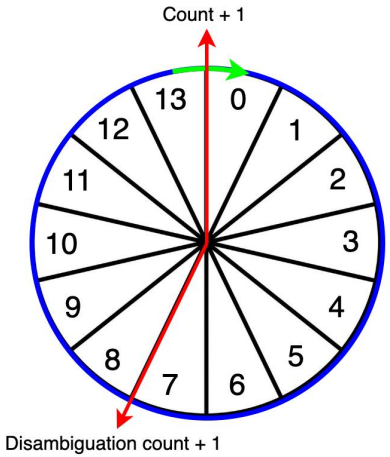
Deposited **charge** → Digital **hit pulse** → **Buffering** towards TDC → **150 ps** time stamp



$$\Delta T = \frac{T}{2N}$$

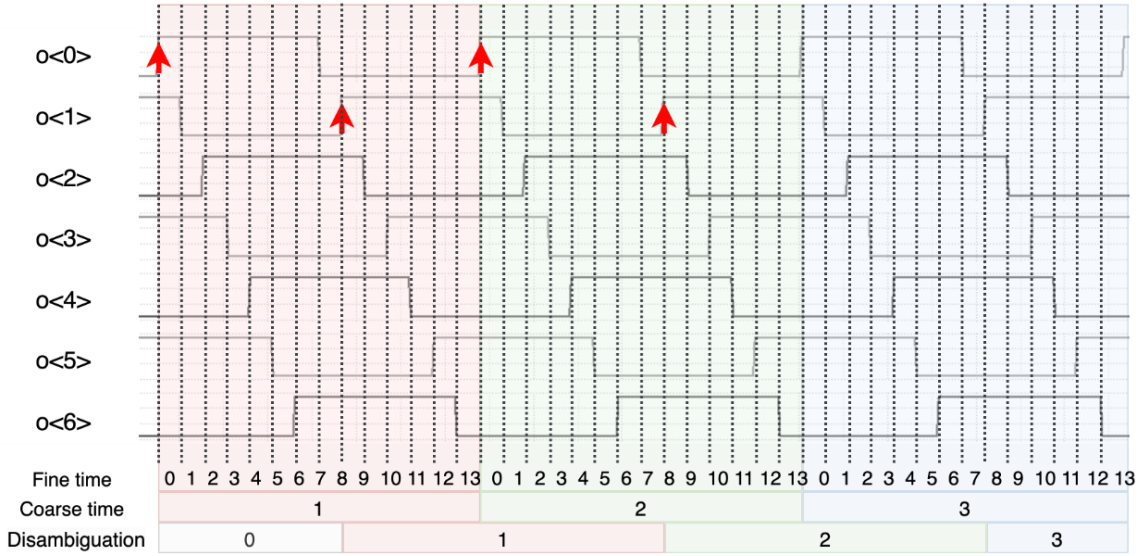
Design parameters:
N = 7
T = 2.1 ns
ΔT = 150 ps

- **Coarse time** counter on ↑ o<0>
- **Fine time** encoding oscillator states gives the LSB
- **Disambiguation** on ↑ o<1> (in anti-phase, checked for fine time 13 and 0 to avoid an error of full period T)

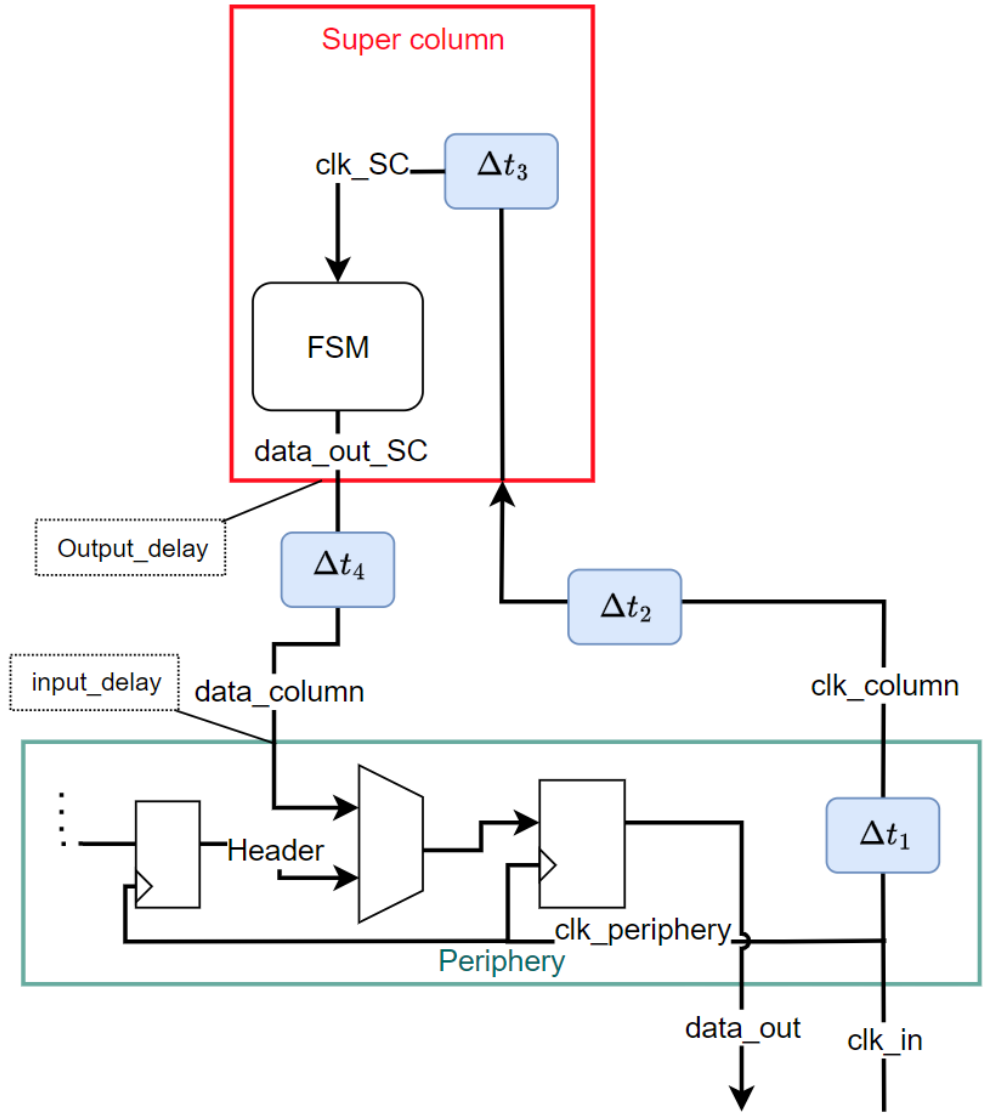


Fine time measurement states encoding

	Encoded states													
Time	0	1	2	3	4	5	6	7	8	9	10	11	12	13
o<0>	1	1	1	1	1	1	1	0	0	0	0	0	0	0
o<1>	1	0	0	0	0	0	0	0	1	1	1	1	1	1
o<2>	0	0	1	1	1	1	1	1	1	0	0	0	0	0
o<3>	1	1	1	0	0	0	0	0	0	0	1	1	1	1
o<4>	0	0	0	0	1	1	1	1	1	1	1	0	0	0
o<5>	1	1	1	1	1	0	0	0	0	0	0	0	1	1
o<6>	0	0	0	0	0	0	1	1	1	1	1	1	1	0



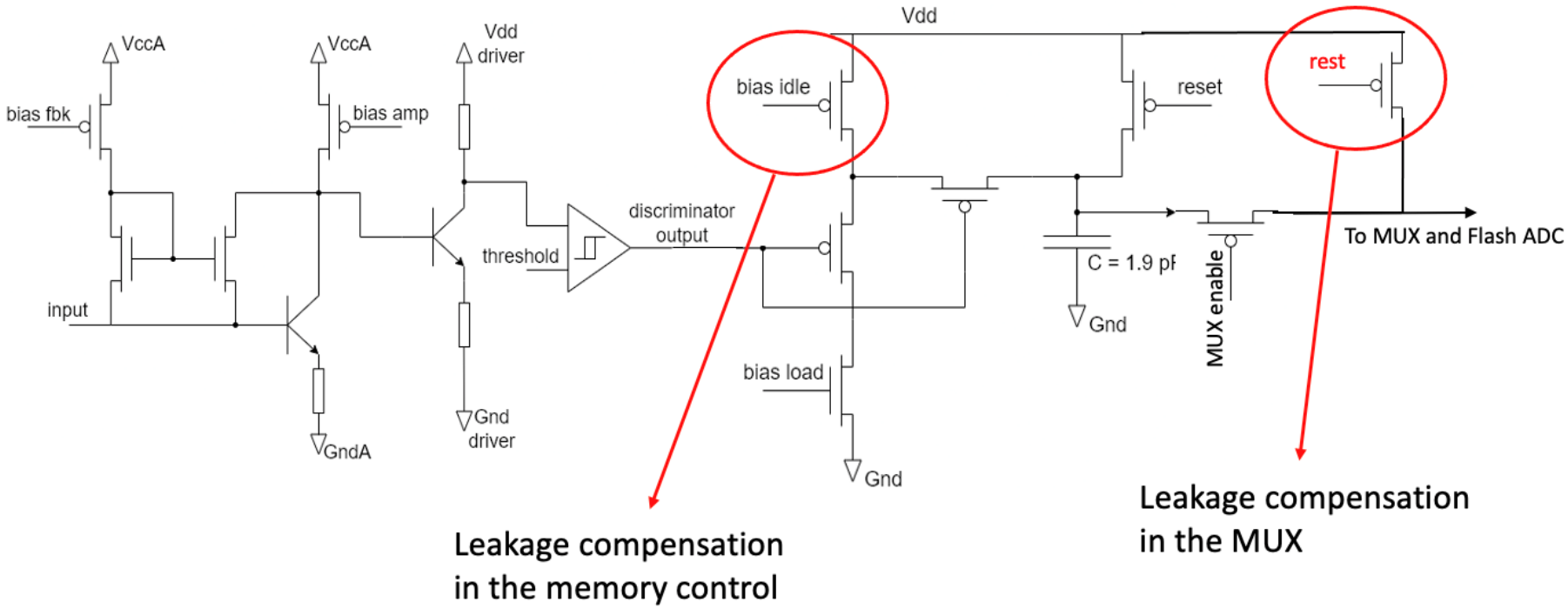
Chip Assembly



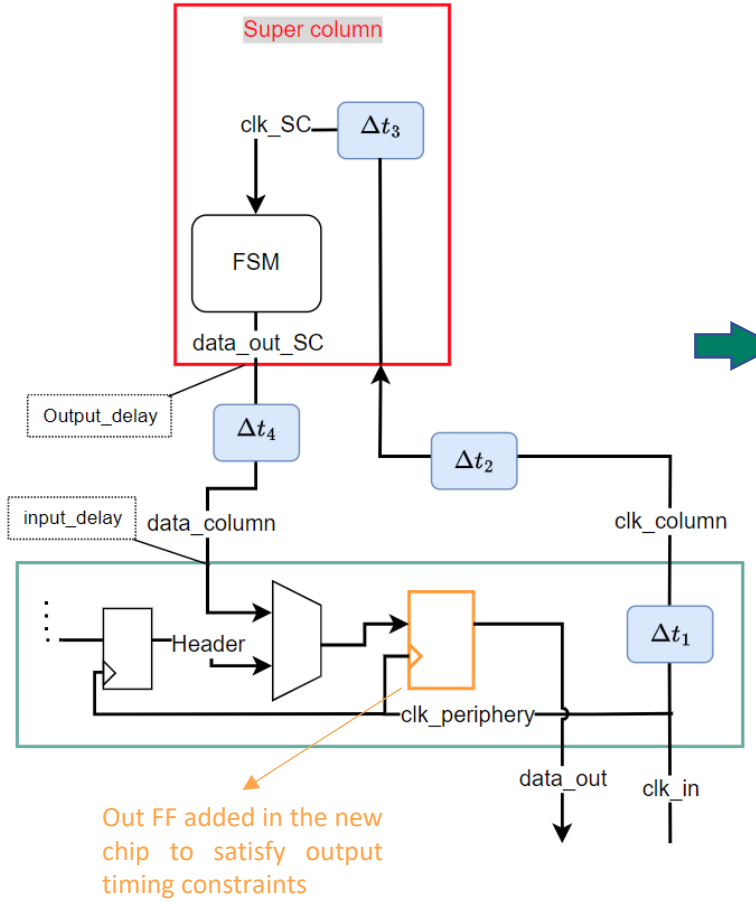
Analogue-on-top design

- Asynchronous interfaces
- Distribution of 200 MHz clock
- Careful, manual timing closure analysis:
  - Δt_1: clock tree delay in periphery
  - Δt_3: clock tree delay in SC
  - Δt_2 and Δt_4: connection delays
  - Δt_{tot} between the two clocks:
    $\Delta t_{tot} = \Sigma_i \Delta t_i$

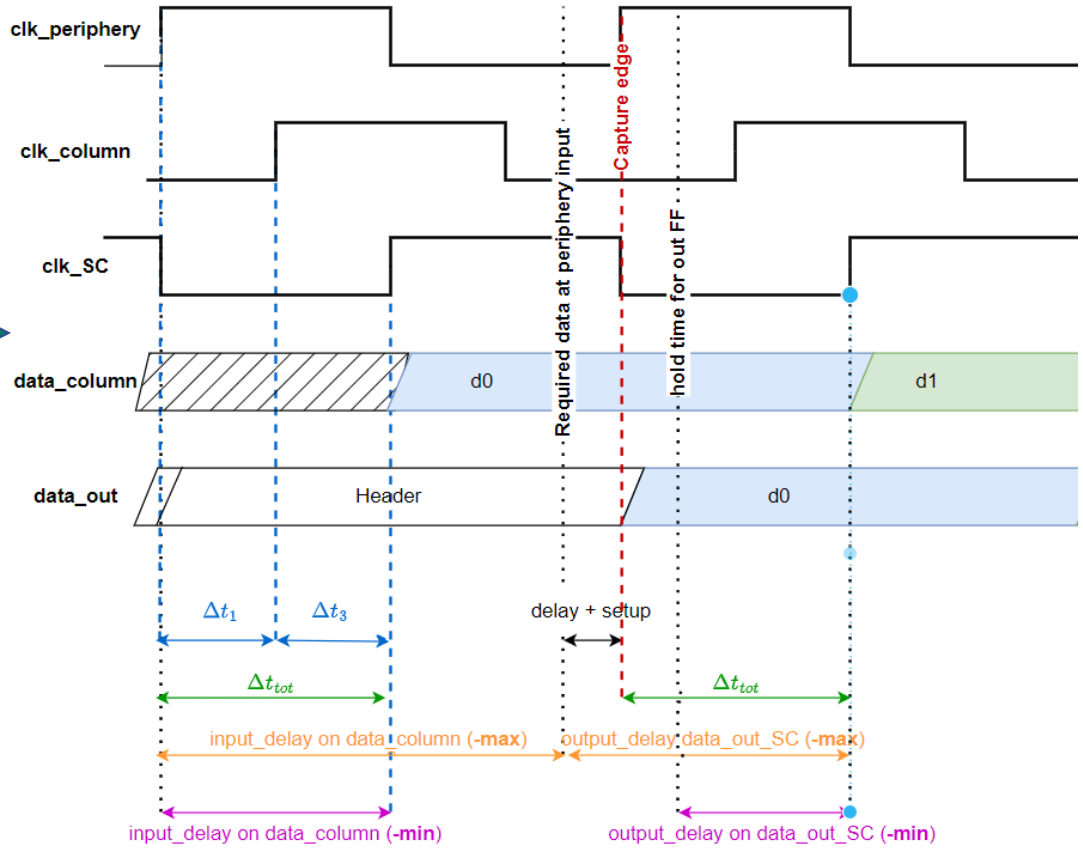
Memory Leakage



Periphery – SC Data Synchronization



- Δt_1: clock tree delay in periphery
- Δt_3: clock tree delay in SC
- Neglect Δt_2 and Δt_4
- Δt_{tot} between the two clocks: $\Delta t_{tot} = \Delta t_1 + \Delta t_3$

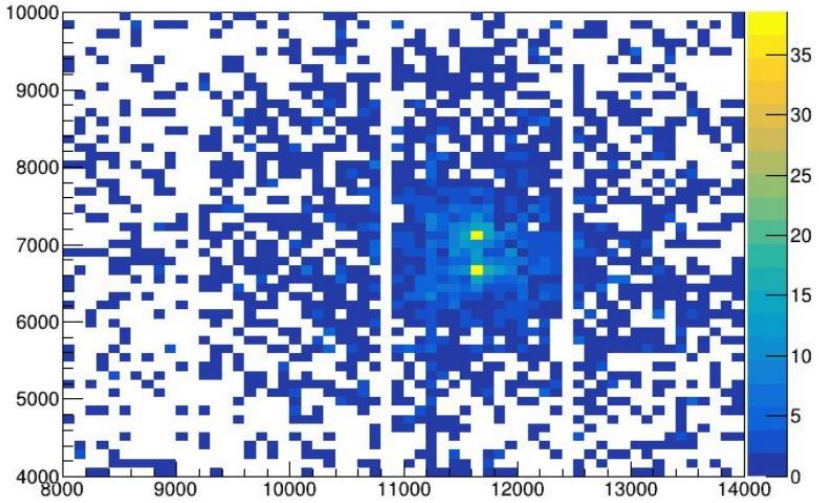


Hit-Map Simulations

UNIVERSITÉ DE GENÈVE
FACULTY OF SCIENCE
Department of Nuclear and Particle Physics

One Event - Hitmap - Chip 405 -2 photons - 1 Tev each - 500 μm Distance - After the Detector Effects

Before the Detector Effects



After the Detector Effects