Contribution ID: **172** Type: **Oral**

Design and characterization of the monolithic ASIC for the pre-shower upgrade of the FASER experiment

Wednesday 2 October 2024 11:40 (20 minutes)

The ASIC for the high-granularity pre-shower detector of the FASER experiment at CERN is a full-reticle imaging chip (1.5x2.2 cmˆ2) for TeV-scale electromagnetic showers at the LHC. It features a monolithic pixel sensor with 65 µm side hexagonal pixels in IHP 130nm SiGe BiCMOS. The pixels integrate analog memories for charge measurement (0.5 fC÷64 fC) and the frontend with 100-ps-level jitter and ENC < 200 electrons. The chip features 100 ps time binning, a frame-based 200 MHz readout, and has a power consumption below 150 mW/cmˆ2.
This work presents the design, the corresponding challenges and the first silicon validation results.

Summary (500 words)

The FASER experiment at CERN searches for dark matter candidates in the form of light, Long-Lived, weakly-interacting particles, produced at zero angle from the beam collision axis at the LHC. Its new, high-granularity pre-shower detector will exploit an imaging ASIC to detect and discriminate two collimated and very energetic (˜1 TeV) photons with a resolution down to 200 µm.
The final production full reticle ASIC (1.5x2.2 cmˆ2) will be installed during the 2024 end of the year LHC shutdown, and it results from previous silicon validation iterations on smaller scale designs. The chip is manufactured in a 130 nm SiGe BiCMOS technology and features a monolithic silicon pixel sensor with 65 µm side hexagonal pixels arranged in a 208 x 128 matrix.
The in-pixel circuitry provides a charge measurement on a dynamic memory by charging it with a constant current during the Time-over-Threshold of the discriminated signal. Within a power budget of 150 mW/cmˆ2, the pixel circuitry achieves a 100 ps level jitter, an ENC < 200 electrons, and a large charge dynamic range (0.5 fC to 64 fC). The charge information is used to reconstruct and identify the core of the collimated particles showers.
The stand-alone data processing unit is a super-pixel containing 16x16 pixels and it enables readout parallelization. Each super-pixel provides a fast dynamic memory digitization with a 4-bit flash ADCs via a 256-to-1 analog MUX. This unit also includes masking and test-pulsing logic, and handles the pixels polling process during readout. The super-pixel digital logic is distributed in the pixel matrix creating a non-sensitive column with a size of 1.5 cm x 40 µm accounting for 1/17 of the area.
Each super-pixel has 3 dedicated fast-OR lines, to provide separate outputs for adjacent pixels. The fast-OR signals are digitized by a TDC at the chip periphery with 100 ps time binning. This block recovers the Time-of-Arrival with sub-clock period precision, improving the background rejection and correlating the signals in time. A total of 312 TDC channels for the whole chip imposes the challenging constraint of a sub 100 ps skew on the synchronization signals spanning across the whole width of the ASIC.
The ASIC's periphery logic handles the configuration phase and the readout of the whole matrix. The basic readout block is a super-column, a group of 8 super-pixels.
The matrix level fast-OR triggers the event-driven digital data readout. The whole system runs on a 200 MHz clock propagated to the matrix to reach the super-pixels, requiring stringent timing constraints for the synchronization between the super-column-level distributed logic and the periphery read-out.
Expected physics events in the FASER pre-shower range from few active pixels to high-occupancy events

with thousands of active pixels in a few super-columns. This justifies a frame-based readout at super-column level with a zero suppression of empty columns. An additional bit suppression of empty pixels results in a two-level compression to further reducing the dead-time during a readout.
We present the design implementation details with validation results of the final production chip.

Author: FENOGLIO, Carlo Alberto

Presenter: FENOGLIO, Carlo Alberto

Session Classification: ASIC

Track Classification: ASIC