Contribution ID: **29** Type: **Oral**

FAST3 asic: front-end electronic with ps resolution, designed for thin LGADs read-out

Tuesday 1 October 2024 14:00 (20 minutes)

The FAST3 (Fast Amplifier for Silicon detector for Timing) is a low noise 16-channel ASIC, belonging to the FAST ASIC family. FAST3 has been implemented in UMC 110 nm CMOS technology, and the design has been optimized for the read-out of 50μm-thick LGAD (Low-Gain Avalanche Diode). The figure of merit of FAST3 is the excellent temporal jitter below 20ps in a wide dynamic range of input charge (from 5 up to 60 fC of charge). This contribution presents the characterization of FAST3 in the laboratory and at test beams.

Summary (500 words)

This contribution presents FAST3, a new version of ASIC belonging to the FAST family of ASICs. The design of FAST3 was driven by the need for high-performance read-out electronics optimized for LGAD sensors such as to preserve the excellent temporal resolution (˜30 ps) of this sensor technology. The broad R&D activity on LGADs for 4D particle-tracking (TI-LGAD, iLGAD, AC-LGAD, DC-RSD) in High Energy Physics, Medical, and Space applications require an appropriate read-out electronic, characterized by i) low noise, ii) excellent temporal jitter (< 20 ps) and iii) a moderate number of channels. FAST3 meets these fundamental requirements. FAST3 was designed by the microelectronic group of INFN Turin in UMC 110 nm CMOS technology, with the aim to achieve a timing jitter below 20 ps when coupled to 50 μm-thick LGADs. FAST3 includes 16 channels distributed over a surface of 1.5x5 mm2, its power rail is 1.2 V, and the power consumption for the front-end stage is 2.4 mW/ch and about 5 mW/ch for the output driver. The front-end amplifier implemented in FAST3 is a broad-band architecture, with a frequency bandwidth of ˜ 0.5 GHz, suitable for fast signals with a rise time of the order of ˜0.5 - 1 ns. FAST3 has a wide input and output range, up to 60 fC and 700 mV, respectively. Moreover, FAST3 has an internal simple control logic to program the gain of its internal read-out chain, with 8 available values of gain.

FAST3 was produced in an MPW by TSMC at the end of 2023 and delivered to the Innovative Silicon Sensors of the INFN and Physic Department in Turin in early 2024.

An extensive laboratory characterization campaign, in order to evaluate the temporal performances of FAST3, has been performed. The characterisation campaign involved two different measurement setups: i) the Charge Injection setup (CI-setup), based on a high-performance pulser; this setup was used to evaluate the gain and jitter of the ASIC; ii) the Beta-setup (β-setup), where the temporal performance of FAST3 coupled to a 50 μm-thick LGAD have been investigated.

The test results with CI-setup showed the capability of the ASIC to achieve temporal jitter values below 20 ps for injected charges larger than 8 fC. Finally, a full temporal resolution of 30 ps has been measured for the system FAST3-LGAD, by using β-setup.

The performance of FAST3 was also measured at a test beam carried on at the DESY test beam site.

The excellent results reported in this contribution demonstrate the potentiality of FAST3 as a multi-channel read-out amplifier for pixelated LGADs and provide the LGAD community with a valuable tool for R&D activity.

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Session Classification: ASIC

Track Classification: ASIC