The testing and performance of the ETROC2 for CMS MTD Endcap Timing Layer (ETL)upgrade

Ted Liu (Fermilab)

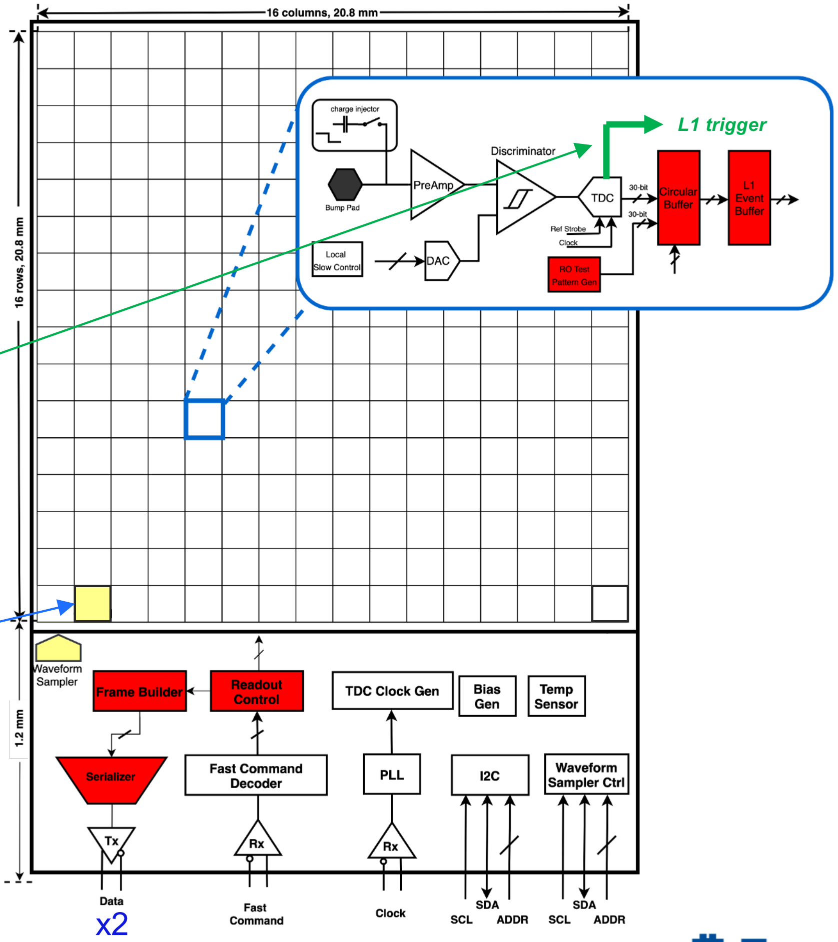
Oct 1, 2024, TWEPP

ETROC is designed to process LGAD signals with time resolution

~ 50ps per hit,

~ 35 ps per track with 2 hits.

- ○ Measuring arrival time of LGAD signal
  - ○ Front-end: PA + Discriminator + TDC
  - ○ L1 latency circular buffer
  - ○ L1A-driven readout with zero suppression
  - ○ A coarse map of (***delayed)*** hits for L1 trigger, monitoring or luminosity
- ○ Interface of ETROC2
  - ○ 40 MHz reference clock
  - ○ I2C-based slow control
  - ○ 320 Mbps fast control
  - ○ Serial data link 320/640/1280 Mbps with two outputs
- ○ Waveform Sampling of preamp output (only 1 pixel)
  - ○ For monitoring purpose



ETROC2 is designed in such a way as if it is the final design, very first full-size prototype, with full functionalities

(with extra flexibilities for performance study purposes)

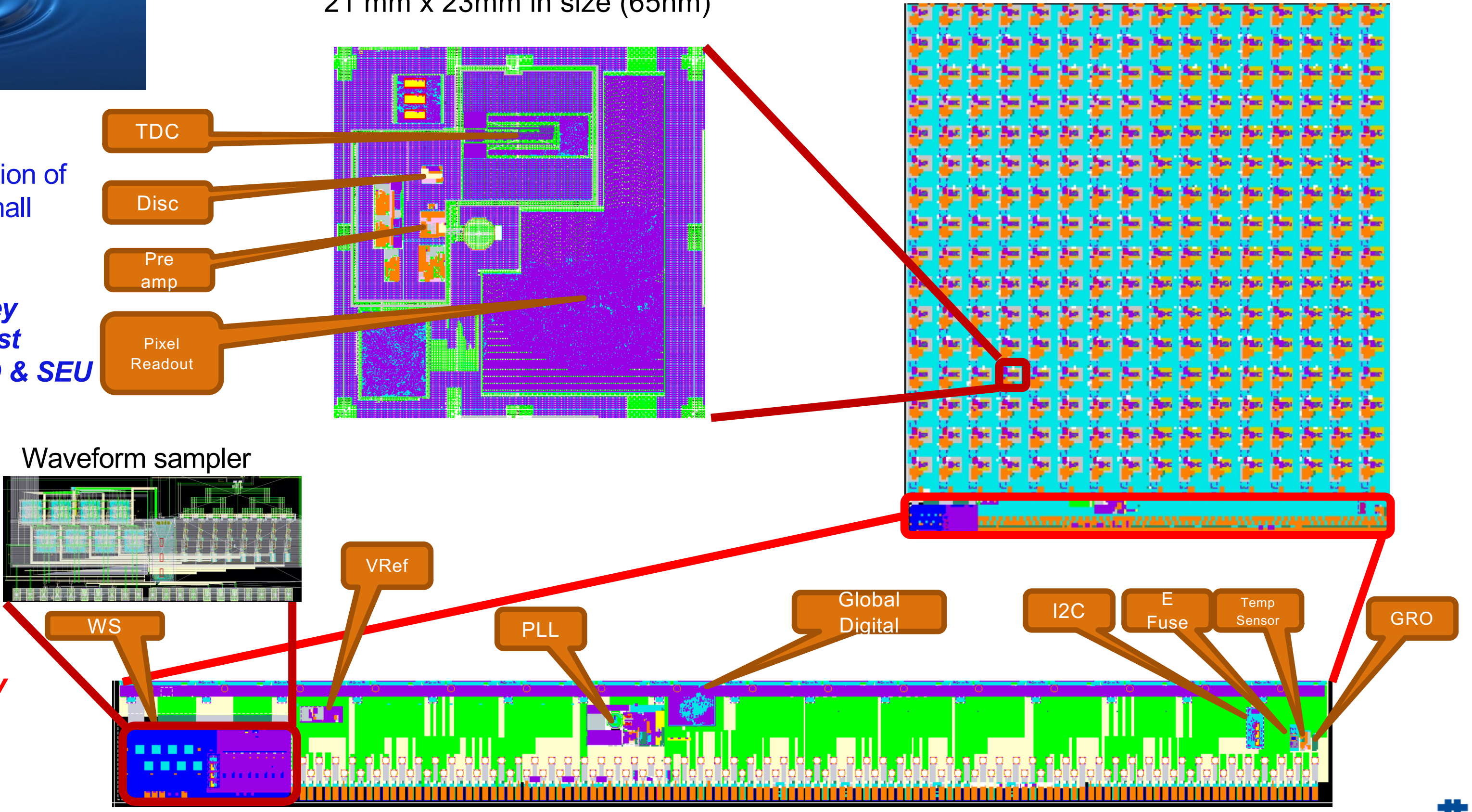
ETROC2 layout (submitted on Oct 21, 2022)

Designed during COVID lockdown, all work done remotely

ETROC:
Precision determination of the arrival time of small water drop ripples

Low noise is the key
Low power is a must
Robust against TID & SEU
….

21 mm x 23mm in size (65nm)



ETROC2 is the first full-size full functionality prototype

Some of ETROC2 key features: from user point of view

- **Each pixel has a low power high performance TDC, automatically *self-calibrated* for every hit recorded**
  - **Important for precision timing performance and uniformity across 16x16 array**
  - **Has large TOA window (effectively up to 11.4ns), can detect long lived or late arriving particles**
  - Paper: https://ieeexplore.ieee.org/document/9446843

- ***Each pixel has auto-threshold scan capability to quickly determine preAmp baseline and noise width***
  - ***User-friendly, save a lot time for manual calibration during detector operation***
  - Paper: https://iopscience.iop.org/article/10.1088/1748-0221/16/09/T09006

- ***Flexible readout design***
  - user-defined window for TOA, TOT and CAL to filter/suppress hits before readout for each pixel
  - user adjustable TOA measurement window (up to 12.5ns, 11.4ns effective)
  - each pixel can be enabled or disabled for DAQ readout
  - Two outputs for readout, each user configurable for 320/640/1280Mbps bandwidth

- ***L1 Trigger path (for monitoring, luminosity measurements or L1 trigger)***
  - a coarse map (user defined) hits continuously sent out every BC (on the same fiber as DAQ readout)
  - user-defined window for TOA, TOT and CAL for triggered hit, ***can trigger on long lived or delayed particles***

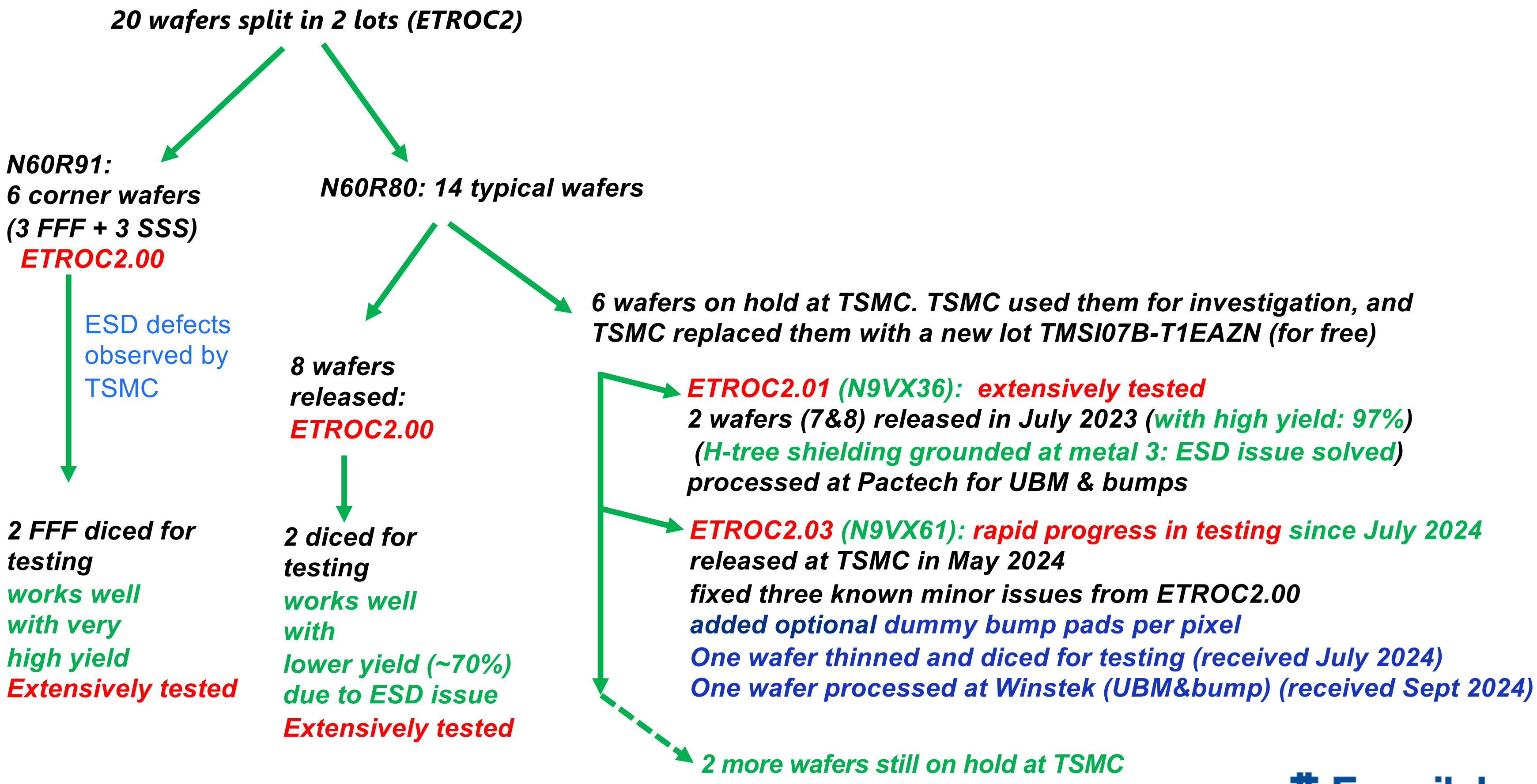
- ***On-chip 2.56 GSPS Waveform Sampler***
  - record waveform for one pixel up to 16 BC (400 ns), start/stop controlled via fast command, readout via I2C
  - power-down when not used, intend for monitoring purpose during detector operation
  - ***ETL has ~ 30k ETROC chips: this means 30k oscilloscope channels available***
  - Paper: IEEE Transactions on Very Large Scale Integration Systems (TVLSI), Volume: 30, Issue: 2, Feb. 2022) Page(s): 123 – 133

- **Charge injection and self-test pattern generator, on-chip PLL (lpGBT), temp sensor, efuse etc**

ETROC2 Engineering Run at TSMC

Submitted
Oct 2022.

Diced chips
received
late April
2023



20 wafers split in 2 lots (ETROC2)

N60R91:
6 corner wafers
(3 FFF + 3 SSS)
ETROC2.00

ESD defects
observed by
TSMC

2 FFF diced for
testing
works well
with very
high yield
Extensively tested

N60R80: 14 typical wafers

8 wafers
released:
ETROC2.00

2 diced for
testing
works well
with
lower yield (~70%)
due to ESD issue
Extensively tested

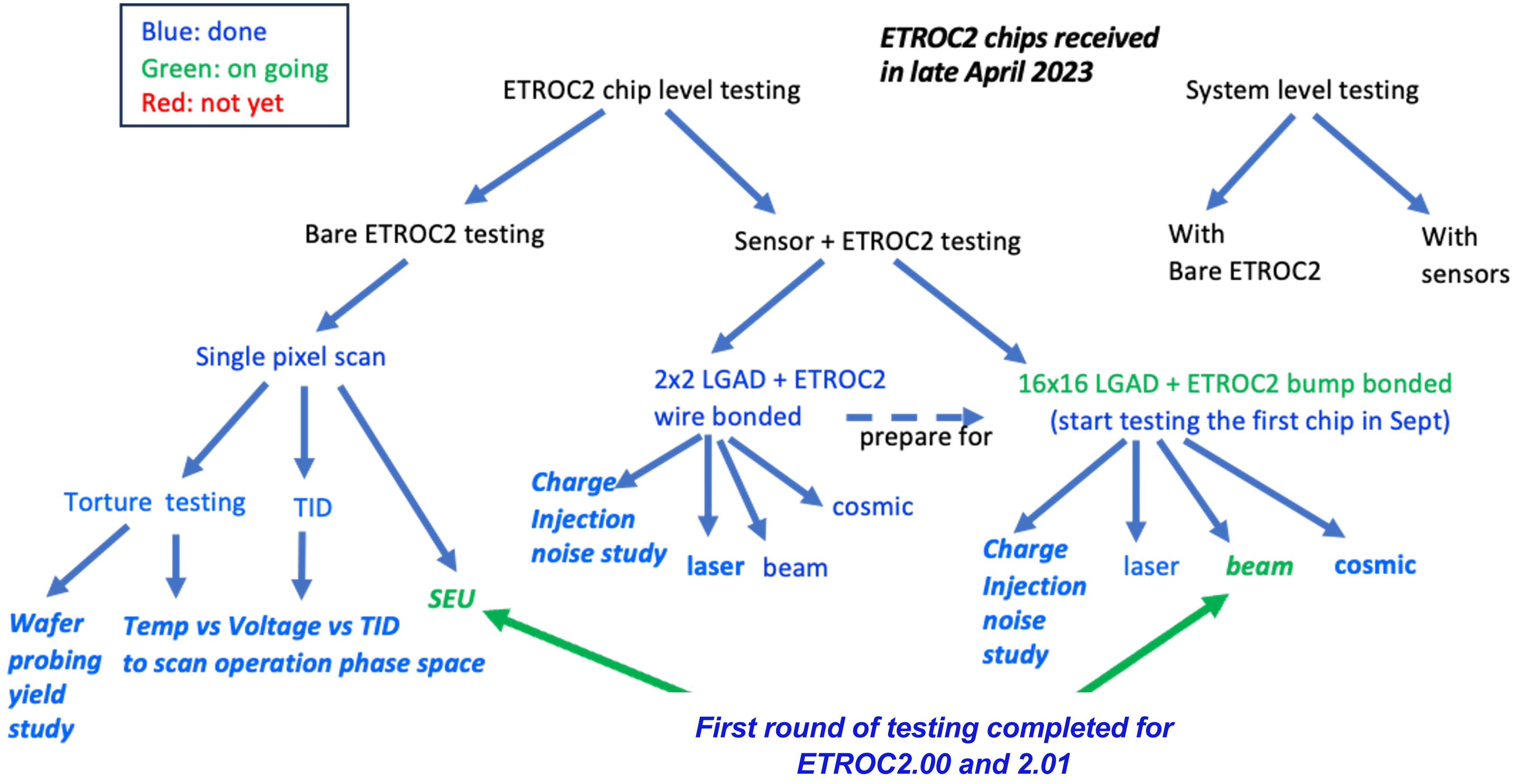
6 wafers on hold at TSMC. TSMC used them for investigation, and
TSMC replaced them with a new lot TMSI07B-T1EAZN (for free)

ETROC2.01 (N9VX36): extensively tested
2 wafers (7&8) released in July 2023 (with high yield: 97%)
(H-tree shielding grounded at metal 3: ESD issue solved)
processed at Pactech for UBM & bumps

ETROC2.03 (N9VX61): rapid progress in testing since July 2024
released at TSMC in May 2024
fixed three known minor issues from ETROC2.00
added optional dummy bump pads per pixel
One wafer thinned and diced for testing (received July 2024)
One wafer processed at Winstek (UBM&bump) (received Sept 2024)

2 more wafers still on hold at TSMC

ETROC2 Testing Road Map



Blue: done
Green: on going
Red: not yet

ETROC2 chips received in late April 2023

ETROC2 chip level testing

Bare ETROC2 testing

Single pixel scan

Torture testing

Wafer probing yield study

Temp vs Voltage vs TID to scan operation phase space

TID

SEU

Sensor + ETROC2 testing

2x2 LGAD + ETROC2 wire bonded

prepare for

Charge Injection noise study

laser

beam

cosmic

16x16 LGAD + ETROC2 bump bonded (start testing the first chip in Sept)

Charge Injection noise study

laser

beam

cosmic

System level testing

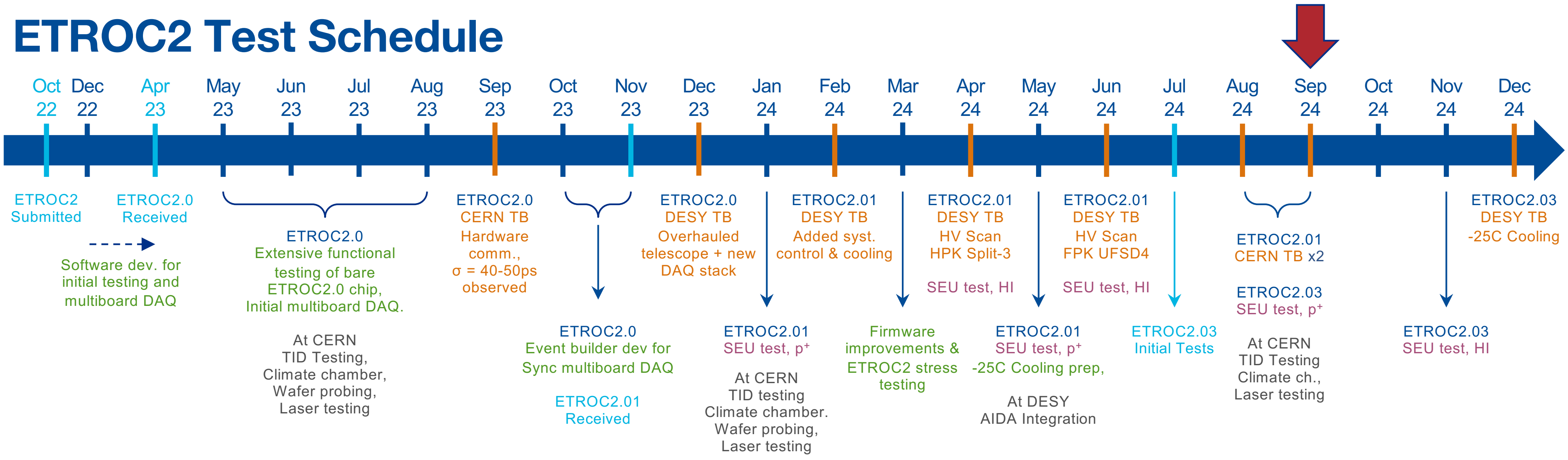
With Bare ETROC2

With sensors

First round of testing completed for ETROC2.00 and 2.01

ETROC2.00/2.01 have been extensively tested, ETROC2.03 is being tested as if it is the final version

ETROC2 Test Schedule



Oct 22
ETROC2
Submitted

Dec 22

Apr 23
ETROC2.0
Received

Software dev. for
initial testing and
multiboard DAQ

May 23 – Aug 23
ETROC2.0
Extensive functional
testing of bare
ETROC2.0 chip,
Initial multiboard DAQ.

At CERN
TID Testing,
Climate chamber,
Wafer probing,
Laser testing

Sep 23
ETROC2.0
CERN TB
Hardware
comm.,
σ = 40-50ps
observed

Oct 23 – Nov 23
ETROC2.0
Event builder dev for
Sync multiboard DAQ

ETROC2.01
Received

Dec 23
ETROC2.0
DESY TB
Overhauled
telescope + new
DAQ stack

Jan 24
ETROC2.01
SEU test, p^+

At CERN
TID testing
Climate chamber.
Wafer probing,
Laser testing

Feb 24
ETROC2.01
DESY TB
Added syst.
control & cooling

Mar 24
Firmware
improvements &
ETROC2 stress
testing

Apr 24
ETROC2.01
DESY TB
HV Scan
HPK Split-3

SEU test, HI

May 24
ETROC2.01
SEU test, p^+
-25C Cooling prep,

At DESY
AIDA Integration

Jun 24
ETROC2.01
DESY TB
HV Scan
FPK UFSD4

SEU test, HI

Jul 24
ETROC2.03
Initial Tests

Aug 24 – Sep 24
ETROC2.01
CERN TB x2

ETROC2.03
SEU test, p^+

At CERN
TID Testing
Climate ch.,
Laser testing

Oct 24

Nov 24
ETROC2.03
SEU test, HI

Dec 24
ETROC2.03
DESY TB
-25C Cooling

ETROC2.00 and 2.01 have been extensively tested over the past year
ETROC2.03 testing on going, so far so good (all three fixes confirmed successful)

To be done:
testing in cold, with irradiated sensors
Improve SEU test setup for one more round of testing
Improve bump bonding yield

Only a few highlights of the test results in this talk

Bump bonded ETROC2 performance with charge injection

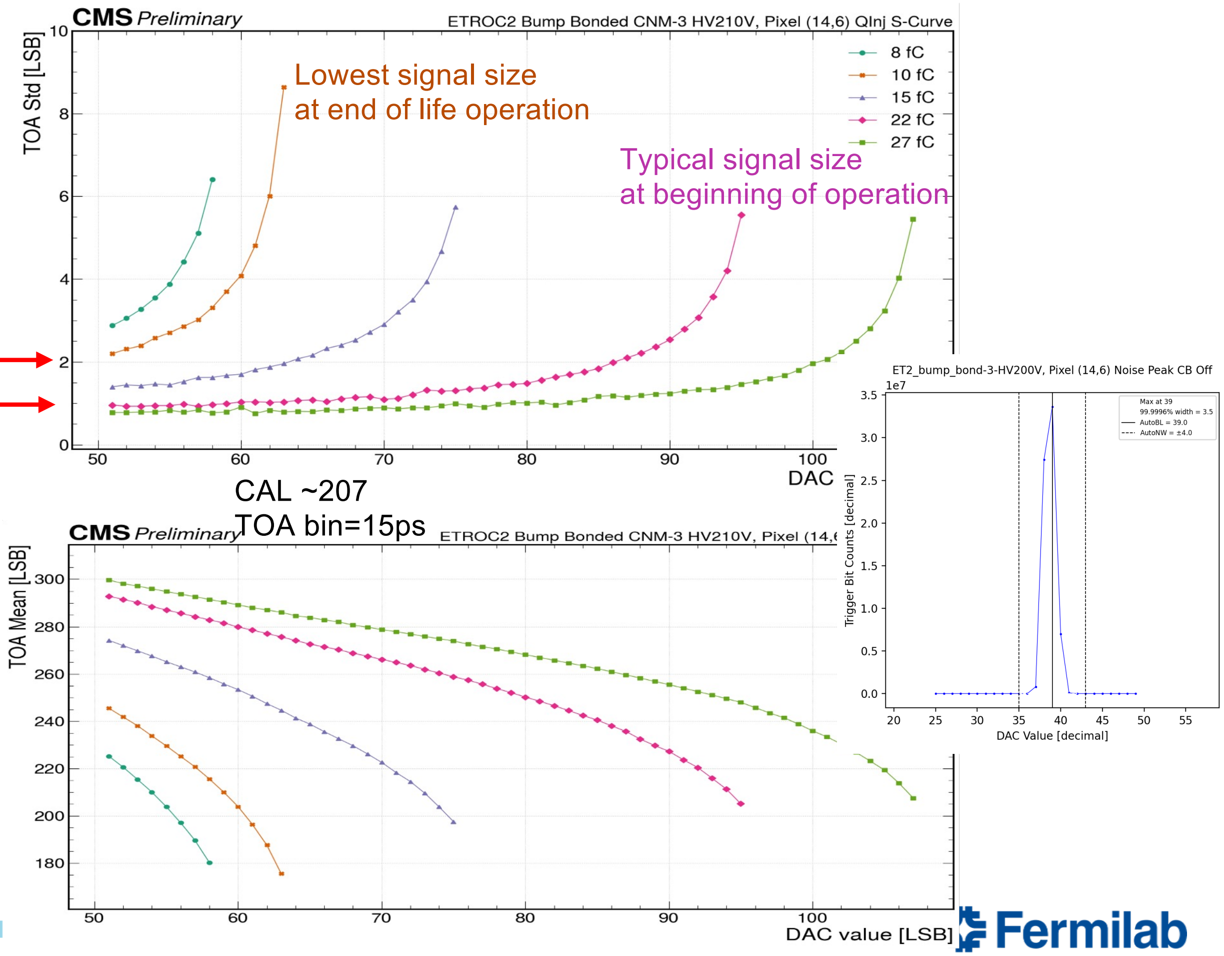
ETL spec is < 50 ps per hit:

LGAD contribution: ~30ps

ASIC contribution:

30ps line

15ps line



Lowest signal size
at end of life operation

Typical signal size
at beginning of operation

CAL ~207
TOA bin=15ps

From charge injection results, the
expected performance with sensor (roughly):

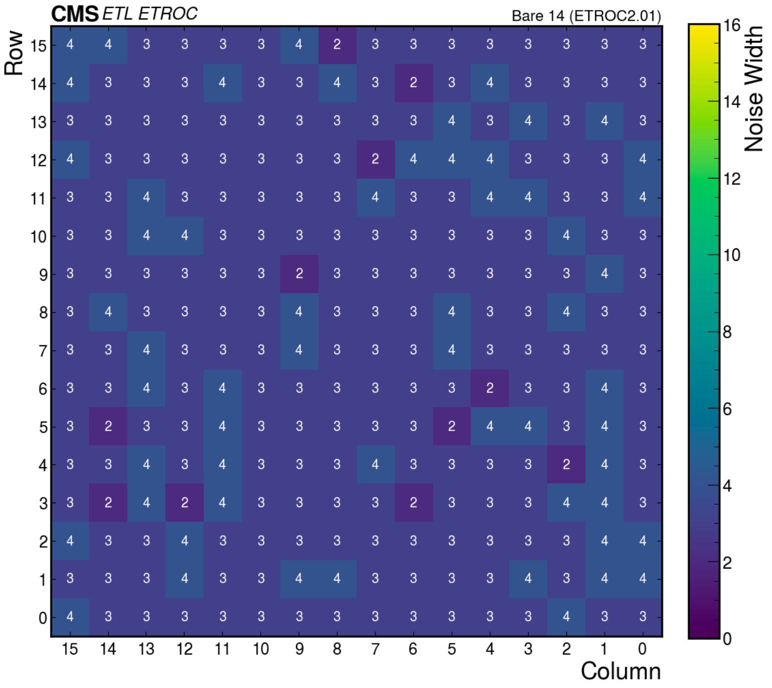
LGAD+ preamp/discriminator + TDC	34 / 42 ps
Time-walk correction residual	< 10 ps
Internal clock distribution	< 10 ps
System clock distribution	< 15 ps
Per hit total time resolution	39 / 47 ps
Per track (2 hits) total time resolution	28 / 33 ps

Initial operation: ~39 ps per hit
End of life operation: ~47ps per hit

ETROC2 has in-pixel automatic threshold scan capability (through I2C command), to determine the baseline and noise width for each pixel (very fast, to map out 16x16 array), see paper below:

https://iopscience.iop.org/article/10.1088/1748-0221/16/09/T09006

Bare ETROC2 noise width map



Row	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
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13	3	3	3	3	3	3	3	3	3	3	4	3	4	3	4	3
12	4	3	3	3	3	3	3	3	2	4	4	4	3	3	3	4
11	3	3	4	3	3	3	3	3	4	3	3	4	4	3	3	4
10	3	3	4	4	3	3	3	3	3	3	3	3	3	4	3	3
9	3	3	3	3	3	3	2	3	3	3	3	3	3	3	4	3
8	3	4	3	3	3	3	4	3	3	3	4	3	3	4	3	3
7	3	3	4	3	3	3	4	3	3	3	4	3	3	3	3	3
6	3	3	4	3	4	3	3	3	3	3	3	2	3	3	4	3
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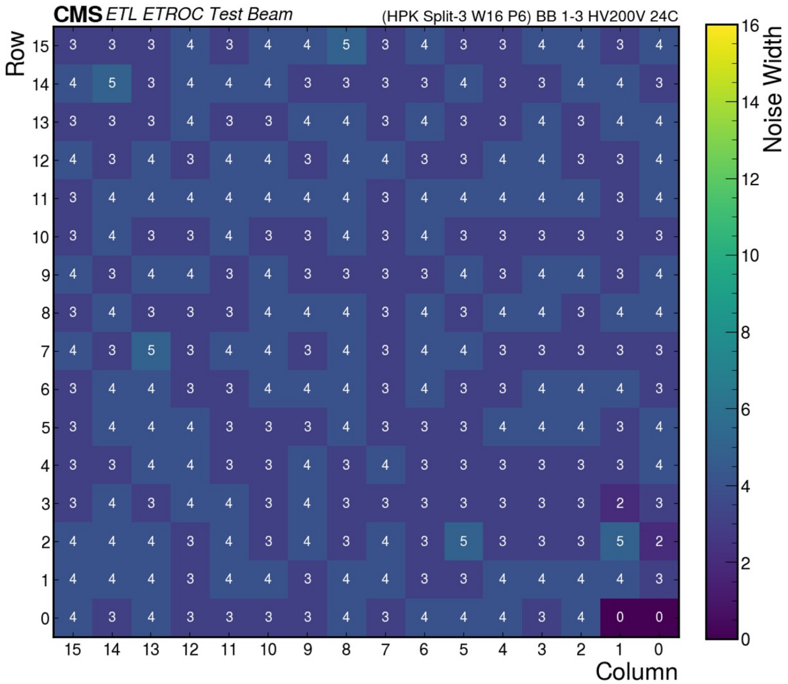
2	4	3	3	4	3	3	3	3	3	3	3	3	3	3	4	4
1	3	3	3	4	3	3	4	4	3	3	3	3	4	3	4	4
0	4	3	3	3	3	3	3	3	3	3	3	3	3	4	3	3

Look very similar

Bump bonded ETROC2 noise width map



Row	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
15	3	3	3	4	3	4	4	5	3	4	3	3	4	4	3	4
14	4	5	3	4	4	4	3	3	3	3	4	3	3	4	4	3
13	3	3	3	4	3	3	4	4	3	4	3	3	4	3	4	4
12	4	3	4	3	4	4	3	4	4	3	3	4	4	3	3	4
11	3	4	4	4	4	4	4	4	3	4	4	4	4	4	3	4
10	3	4	3	3	4	3	3	4	3	4	3	3	3	3	3	3
9	4	3	4	4	3	4	3	3	3	3	4	3	4	4	3	4
8	3	4	3	3	3	4	4	4	3	4	3	4	4	3	4	4
7	4	3	5	3	4	4	3	4	3	4	4	3	3	3	3	3
6	3	4	4	3	3	4	4	4	3	4	3	3	4	4	4	3
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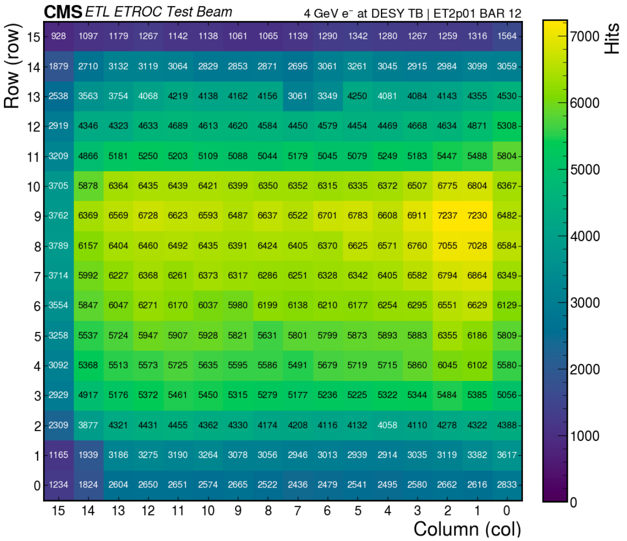
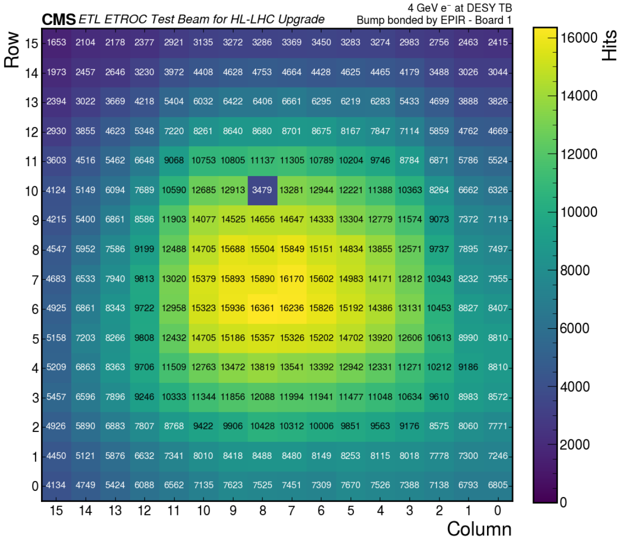
2	4	4	4	3	4	3	4	3	4	3	5	3	3	3	5	2
1	4	4	4	3	4	4	3	4	4	3	3	4	4	4	4	3
0	4	3	4	3	3	3	3	4	3	4	4	4	3	4	0	0

The bump bonded ETROC2 noise is so low that it is NOT easy to tell if a pixel is bump bonded with sensor

Beam spot (hits occupancy map)
on ETROC2 bump bonded with sensor

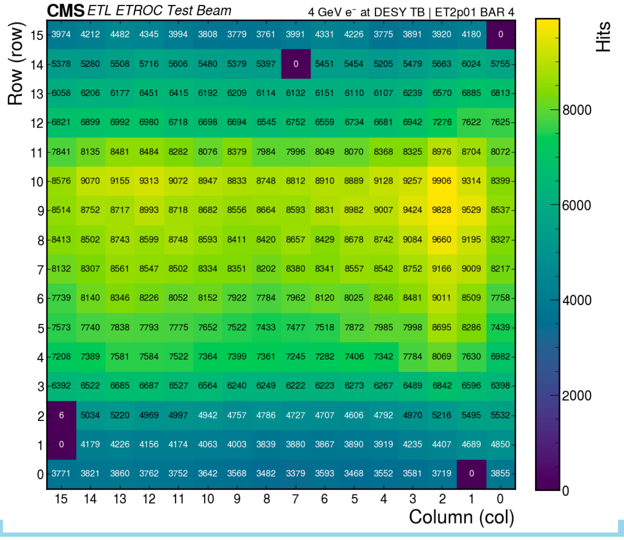


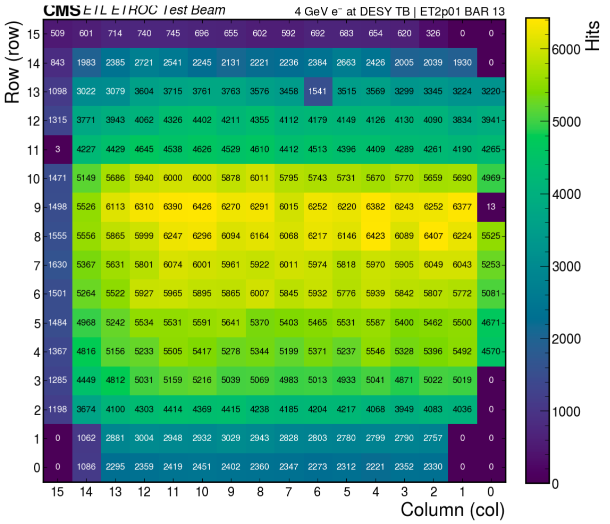


All pixels are connected
(100% bump bonding)

Left: done at Barcelona
Right: fully processed by EPIR (sensor/ASIC)

Just some examples used in beam tests



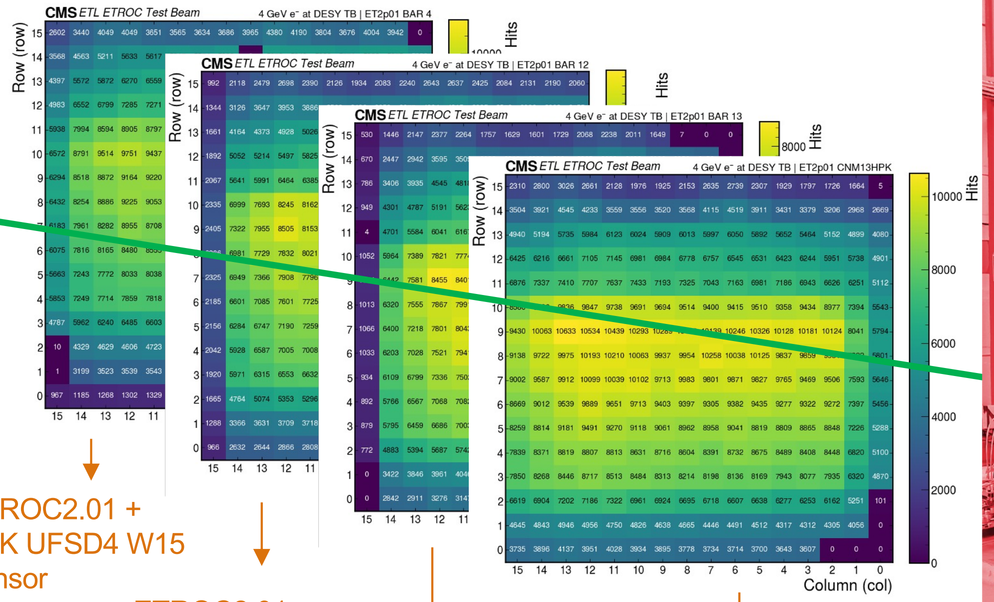


some chips with
pixels not fully connected

(some poorly connected, not shown here)

Bump bonding yield to be improved

ETROC2 Telescope at DESY Jun 2024



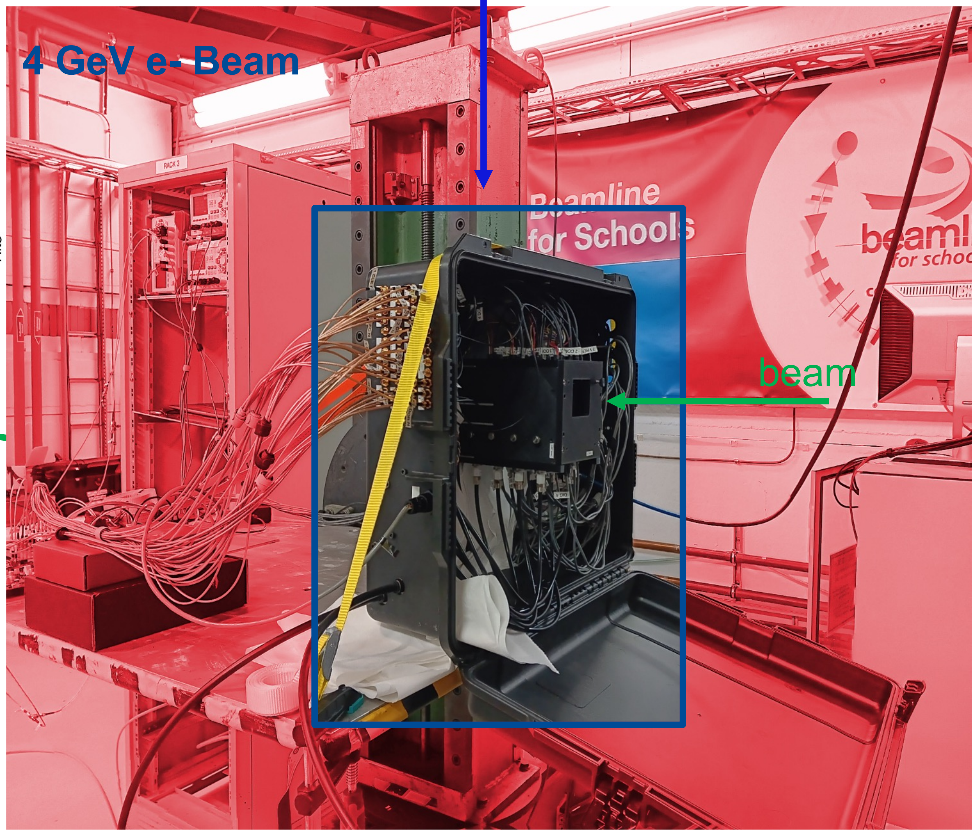
ETROC2.01 +
FBK UFSD4 W15
sensor

ETROC2.01 +
HPK sensor

ETROC2.01 +
HPK sensor

ETROC2.00 (FFF) +
HPK Split-3 sensor

ETROC2 suitcase telescope



Board information inside telescope at DESY in May-June 2024

- Name: Barcelona 4
- ETROC2.01
- Sensor UBM: PacTech
- ETROC UBM/Bumps: Pactech
- Bump bonding: Barcelona
- LGAD: FBK UFSD4 W15 2-3

Trigger

- Name: Barcelona 13
- ETROC2.01
- Sensor UBM: HPK
- ETROC UBM/Bumps: Pactech
- Bump bonding: Barcelona
- LGAD: HPK P6

Reference board

- Name: Barcelona 12
- ETROC2.01
- Sensor UBM: HPK
- ETROC UBM/Bumps: Pactech
- Bump bonding: Barcelona
- LGAD: HPK P5

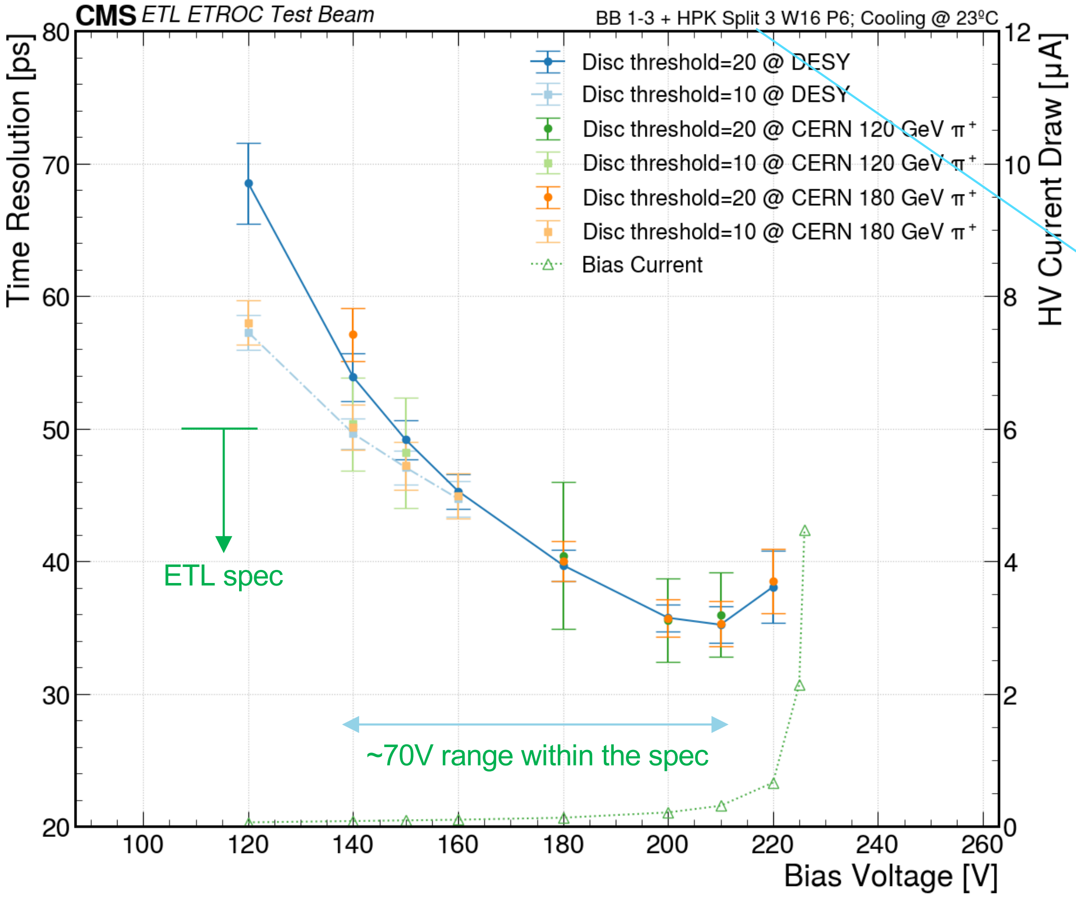
Reference board

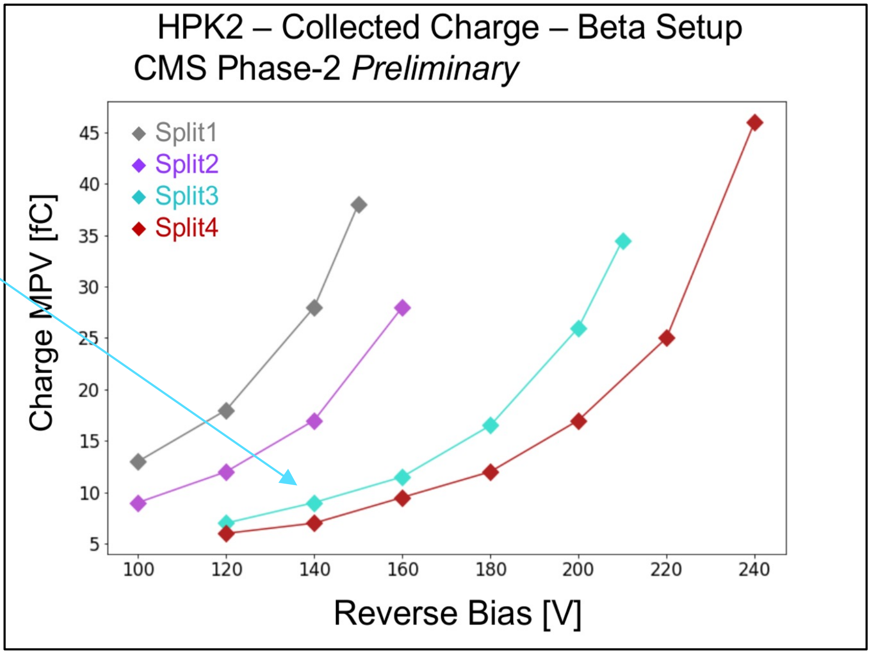
100% pixels connected

- Name: BB 1-3
- ETROC2.00 FFF corner
- Sensor UBM: HPK
- ETROC UBM: CNM; Bumps: Barcelona
- Bump bonding: Barcelona
- LGAD: HPK W16 P6 - Split3

HV Scan

ETROC2 beam test at DESY (June) and CERN (Aug and Sep 2024)

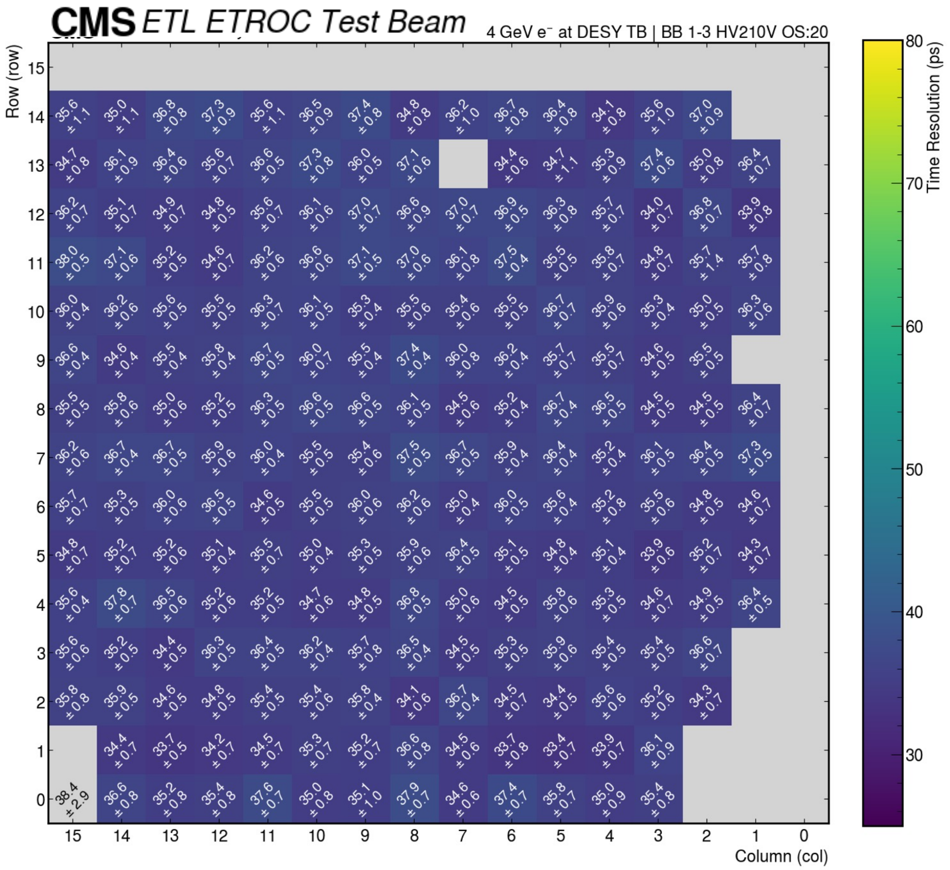




Successfully reproduced ~35ps res. with this board.
Results from CERN 120-180 GeV π^+ beams agree with those from DESY 4GeV e^- beam

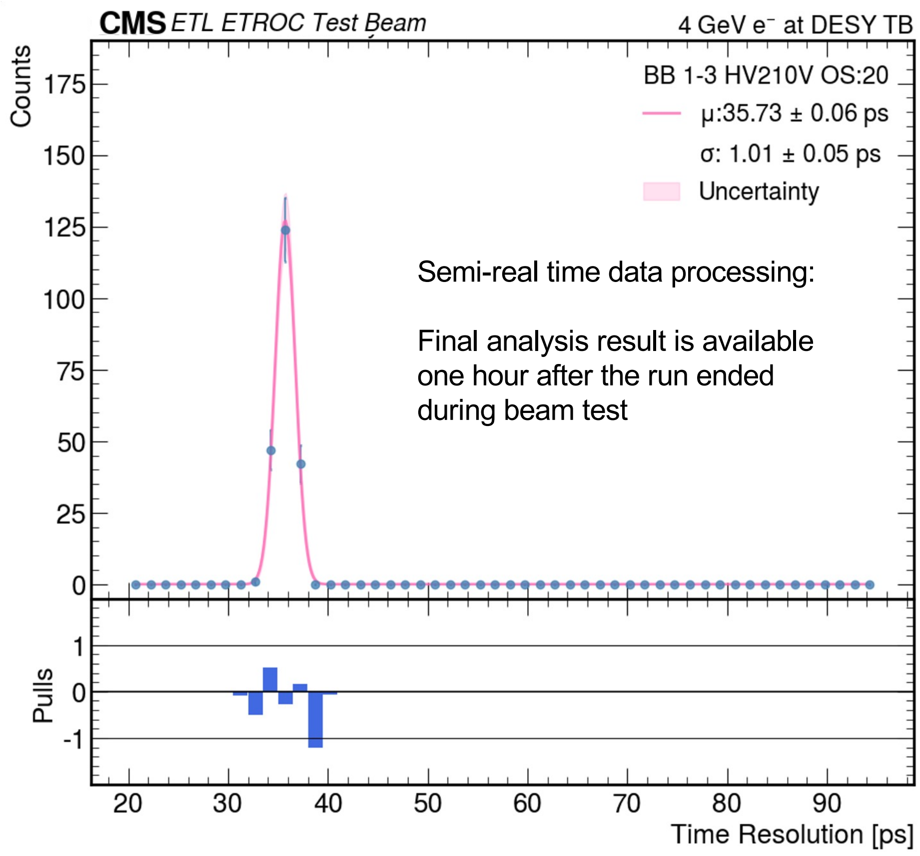
To be done: test in cold, and w/ irradiated sensors

210V HV point for HPK Split-3 + ETROC2.00



Row \ Col	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
15																
14	35.6 ±1.1	35.0 ±1.1	36.8 ±0.8	37.3 ±0.9	35.6 ±1.1	36.5 ±0.9	37.4 ±0.8	34.8 ±0.8	36.2 ±1.0	36.7 ±0.8	36.4 ±0.8	34.1 ±0.8	35.6 ±1.0	37.0 ±0.9		
13	34.7 ±0.8	36.1 ±0.9	36.4 ±0.6	35.6 ±0.7	36.6 ±0.5	37.3 ±0.8	36.0 ±0.5	37.1 ±0.6		34.4 ±0.6	34.7 ±1.1	35.3 ±0.9	37.4 ±0.6	35.0 ±0.8	36.4 ±0.7	
12	36.2 ±0.7	35.1 ±0.7	34.9 ±0.7	34.8 ±0.5	35.6 ±0.7	36.1 ±0.6	37.0 ±0.7	36.6 ±0.9	37.0 ±0.7	36.9 ±0.5	36.3 ±0.8	35.7 ±0.7	34.0 ±0.7	36.8 ±0.7	33.9 ±0.8	
11	38.0 ±0.5	37.1 ±0.6	35.2 ±0.5	34.6 ±0.7	36.2 ±0.6	36.6 ±0.6	37.1 ±0.5	37.0 ±0.6	36.1 ±0.8	37.5 ±0.4	35.5 ±0.5	35.8 ±0.7	34.8 ±0.7	35.7 ±1.4	35.7 ±0.8	
10	36.0 ±0.4	36.2 ±0.6	35.6 ±0.5	35.5 ±0.5	36.3 ±0.7	36.1 ±0.5	35.3 ±0.4	35.5 ±0.6	35.4 ±0.6	35.5 ±0.5	36.7 ±0.7	35.9 ±0.6	35.3 ±0.4	35.0 ±0.5	36.3 ±0.6	
9	36.6 ±0.4	34.6 ±0.4	35.5 ±0.4	35.8 ±0.4	36.7 ±0.5	36.0 ±0.7	35.5 ±0.4	37.4 ±0.4	36.0 ±0.8	36.2 ±0.4	35.7 ±0.7	35.5 ±0.7	34.6 ±0.5	35.5 ±0.5		
8	35.5 ±0.5	35.8 ±0.6	35.0 ±0.6	35.2 ±0.5	36.3 ±0.5	36.6 ±0.5	36.6 ±0.5	36.1 ±0.5	34.5 ±0.6	35.2 ±0.4	36.7 ±0.4	36.5 ±0.5	34.5 ±0.5	34.5 ±0.5	36.4 ±0.7	
7	36.2 ±0.6	36.7 ±0.4	36.7 ±0.5	35.9 ±0.6	36.0 ±0.4	35.5 ±0.5	35.4 ±0.6	37.5 ±0.5	36.7 ±0.5	35.9 ±0.4	36.4 ±0.4	35.2 ±0.4	36.1 ±0.5	36.4 ±0.5	37.3 ±0.5	
6	35.7 ±0.7	35.3 ±0.5	36.0 ±0.6	36.5 ±0.5	34.6 ±0.5	35.5 ±0.5	36.0 ±0.6	36.2 ±0.6	35.0 ±0.4	36.0 ±0.5	35.6 ±0.4	35.2 ±0.8	35.5 ±0.6	34.8 ±0.5	34.6 ±0.7	
5	34.8 ±0.7	35.2 ±0.7	35.2 ±0.6	35.1 ±0.4	35.5 ±0.7	35.0 ±0.4	35.3 ±0.5	35.9 ±0.6	36.4 ±0.5	35.1 ±0.5	34.8 ±0.4	35.1 ±0.4	33.9 ±0.6	35.2 ±0.7	34.3 ±0.7	
4	35.6 ±0.4	37.8 ±0.7	36.5 ±0.6	35.2 ±0.6	35.2 ±0.5	34.7 ±0.6	34.8 ±0.5	36.8 ±0.5	35.0 ±0.6	34.5 ±0.5	35.8 ±0.6	35.3 ±0.5	34.6 ±0.7	34.9 ±0.5	36.4 ±0.5	
3	35.6 ±0.6	35.2 ±0.5	34.4 ±0.5	36.3 ±0.5	36.4 ±0.5	36.2 ±0.4	35.7 ±0.8	36.5 ±0.4	34.5 ±0.5	35.3 ±0.5	35.9 ±0.6	35.4 ±0.5	35.4 ±0.5	36.6 ±0.7		
2	35.8 ±0.8	35.9 ±0.5	34.6 ±0.5	34.8 ±0.5	35.4 ±0.5	35.4 ±0.6	35.8 ±0.4	34.1 ±0.6	36.7 ±0.4	34.5 ±0.7	34.4 ±0.5	35.6 ±0.6	35.2 ±0.6	34.3 ±0.7		
1		34.4 ±0.7	33.7 ±0.5	34.2 ±0.7	34.5 ±0.7	35.3 ±0.7	35.2 ±0.7	36.6 ±0.8	34.5 ±0.6	33.7 ±0.8	33.4 ±0.7	33.9 ±0.7	36.1 ±0.9			
0	38.4 ±2.9	36.6 ±0.8	35.2 ±0.8	35.4 ±0.8	37.6 ±0.7	35.0 ±0.8	35.1 ±1.0	37.9 ±0.7	34.6 ±0.6	37.4 ±0.7	35.8 ±0.7	35.0 ±0.9	35.4 ±0.8			

Pixel resolution map over 16x16 array

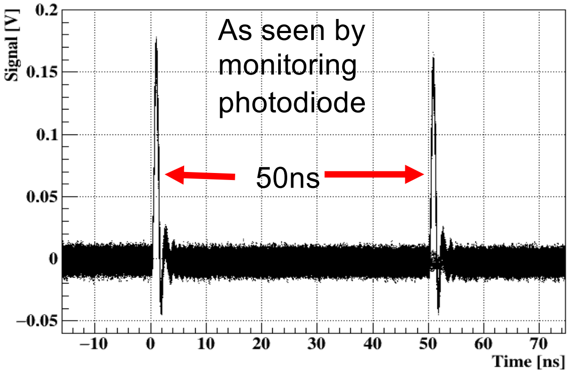


Semi-real time data processing:

Final analysis result is available one hour after the run ended during beam test

Bump bonded ETROC2 performance with a double pulse IR laser at CERN-SSD

$$\sigma^2_{ToA} = \sigma^2_{laser} + \sigma^2_{Clock} + \sigma^2_{sensor} + \sigma^2_{ETROC2}$$



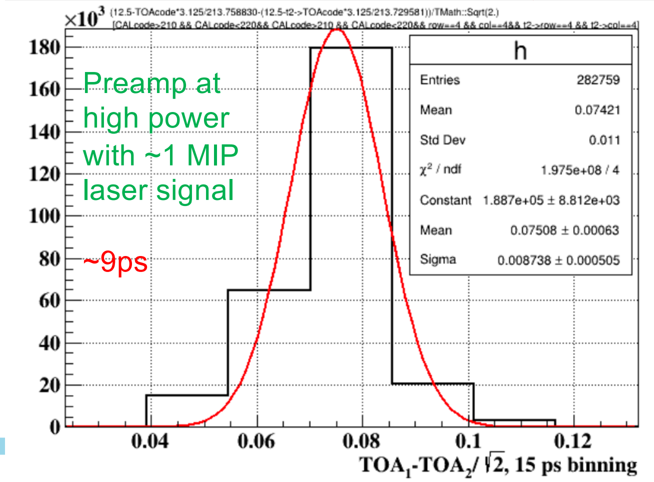
As seen by monitoring photodiode

50ns

Two pulse "timing" configuration

Jitter
is calculated as:

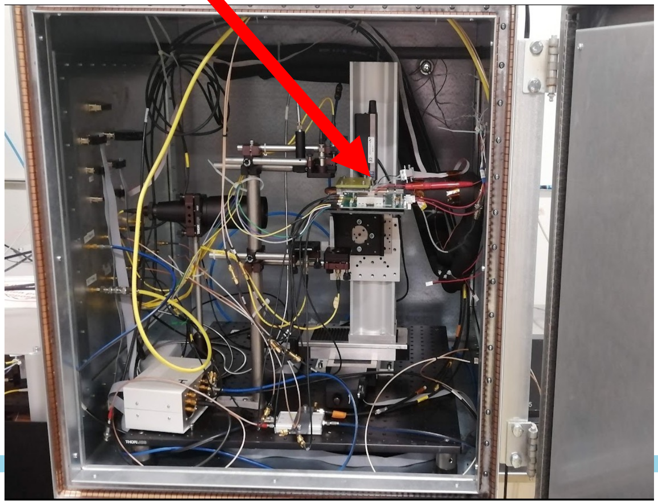
$$\frac{\sigma_{(TOA_1 - TOA_2)}}{\sqrt{2}}$$



Preamp at high power with ~1 MIP laser signal

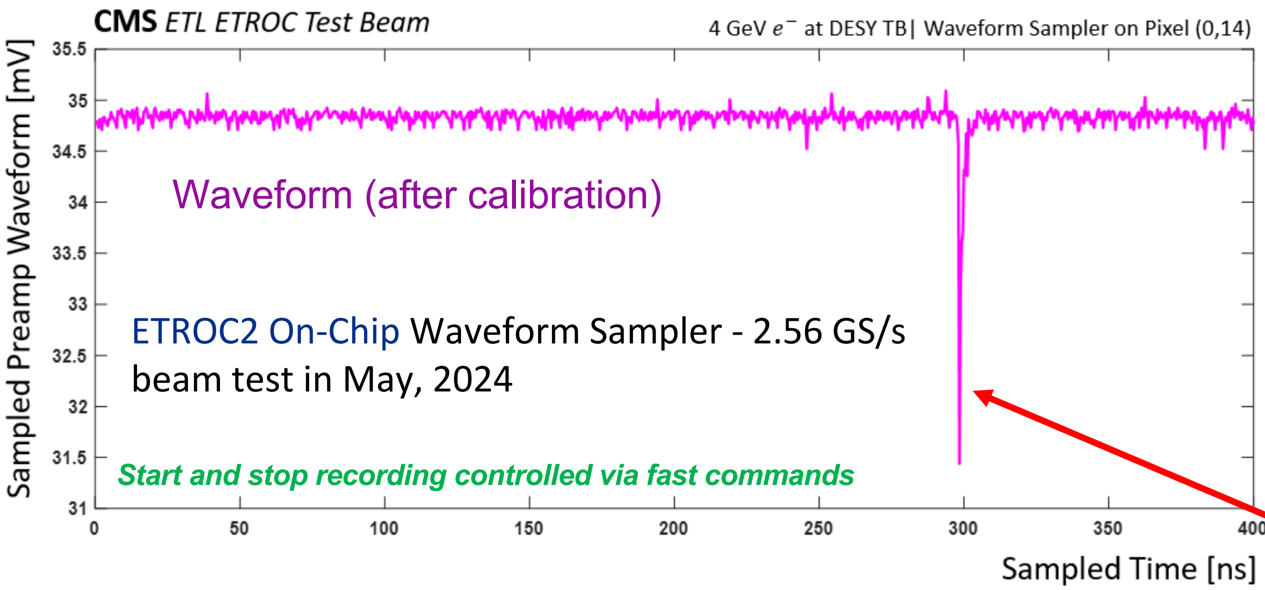
~9ps

ETROC2 bump bonded with 16x16 HPK sensor



ETROC2 Waveform Sampler

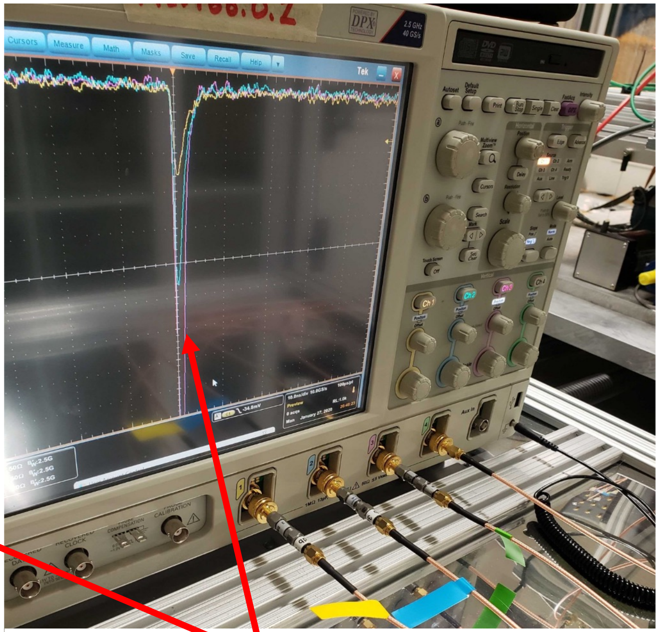
WS Paper: IEEE Transactions on Very Large Scale Integration Systems (TVLSI), Volume: 30, Issue: 2, Feb. 2022) Page(s): 123 – 133



Waveform (after calibration)

ETROC2 On-Chip Waveform Sampler - 2.56 GS/s beam test in May, 2024

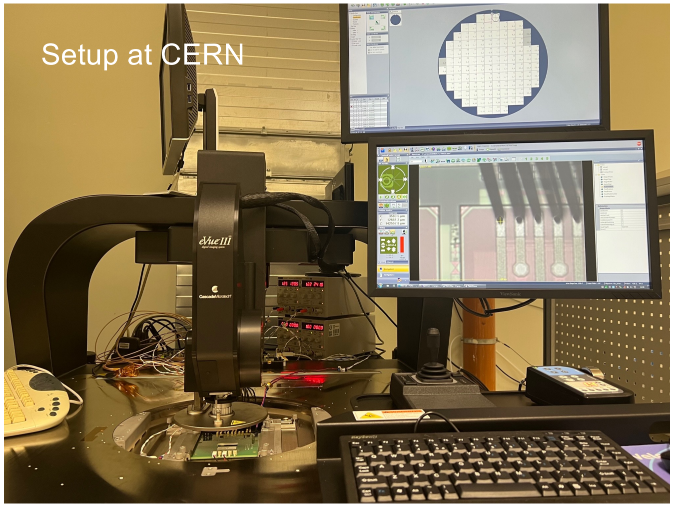
Start and stop recording controlled via fast commands

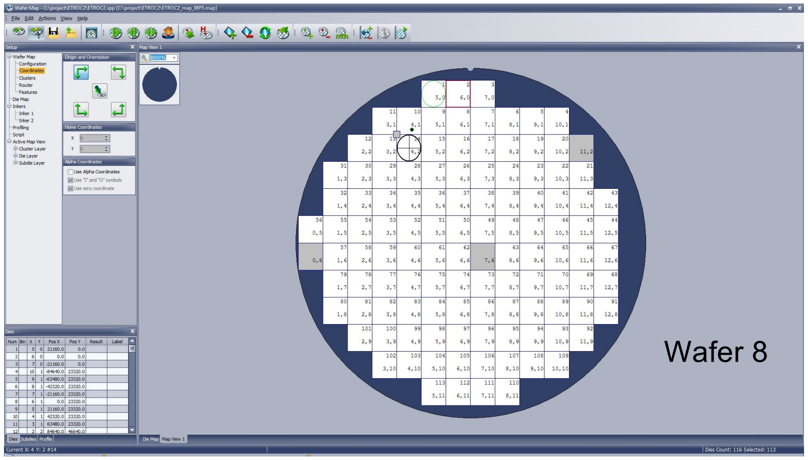


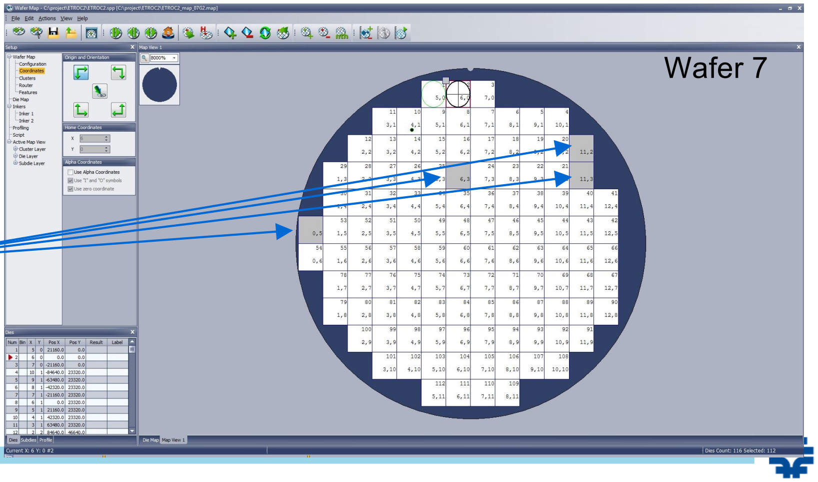
ETROC0 Preamp output waveform by Oscilloscope (40GS/s) in Jan, 2020 (beam test at Fermilab)

- 4 years after the recording of ETROC0 preamp waveforms using high speed Oscilloscope, we can now use ETROC2 on-chip waveform sampler to do the same with ETROC2 self-triggering capability

Wafer probe testing for ETROC2 wafers







Two new ETROC2.01 wafers from TSMC
Arrived CERN in Aug 2023

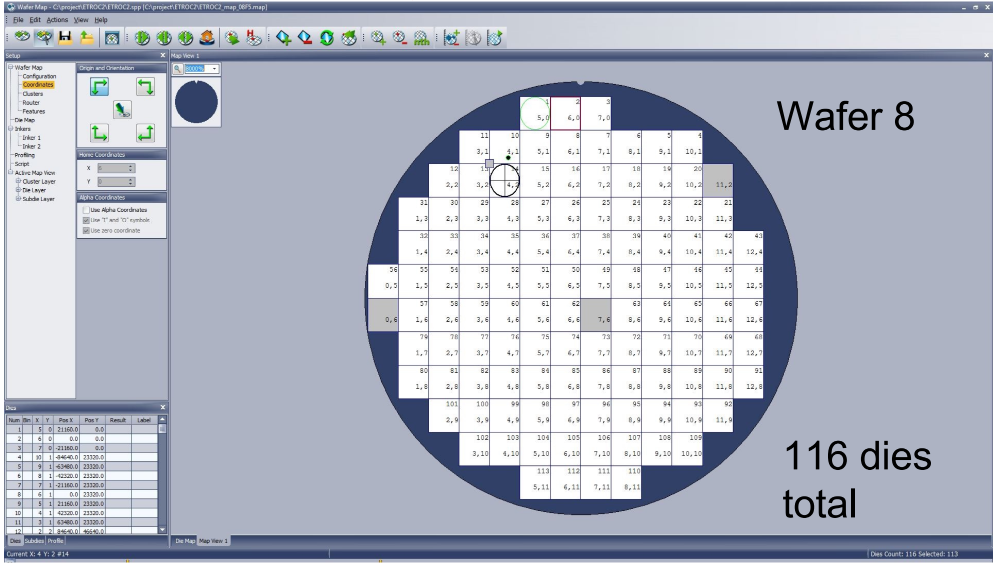
probe testing shows ***only** 4 bad dies*
(out of 116 dies) per wafer in each case

Production QC procedure developed and established for wafer probe testing.

Wafer 7 & 8 processed at Pactech for UBM and bumps, wafer 7 was thinned and diced for testing, while wafer 8 is not diced as a control sample.

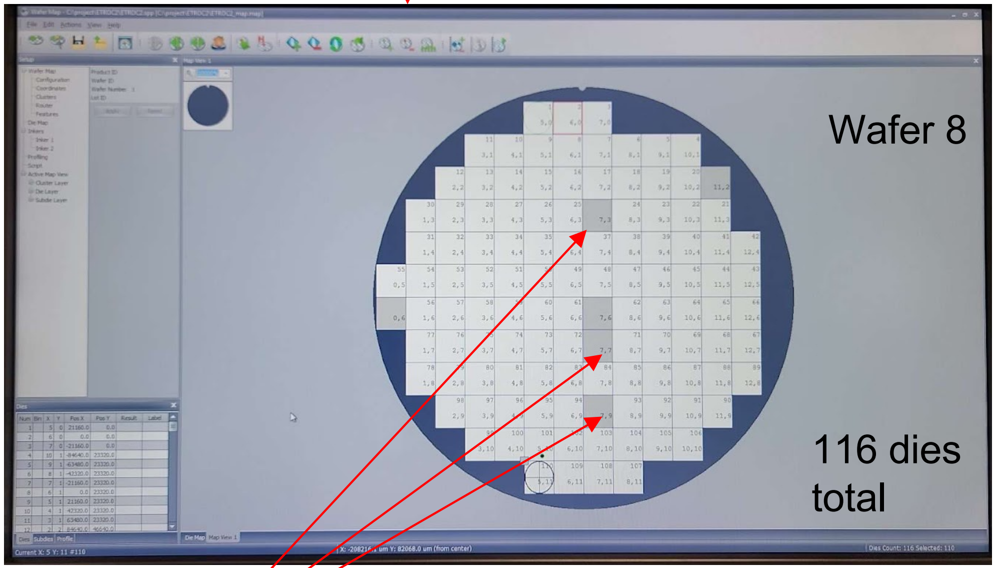
Wafer probing testing results for wafer 8, before and after Pactech UBM/bump processing

Last Aug 2023 → Pactech UBM/bumping at wafer level → Jan 2024 (Jan 13-14 weekend at CERN)



Wafer 8

116 dies total



Wafer 8

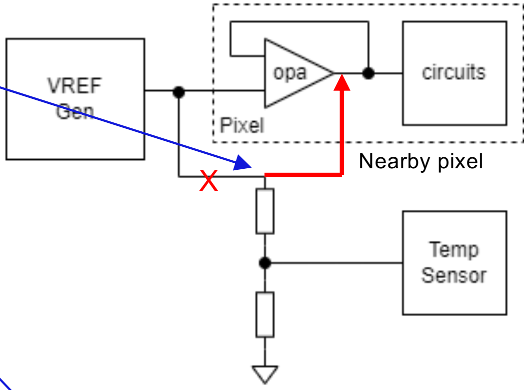
116 dies total

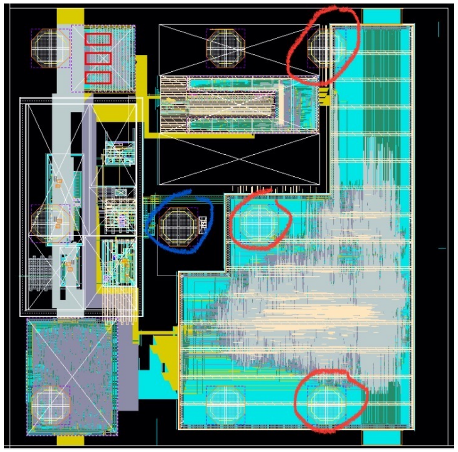
Three new dies with power shorts, the rest all passed testing
(yield is still high, Pactech informed)

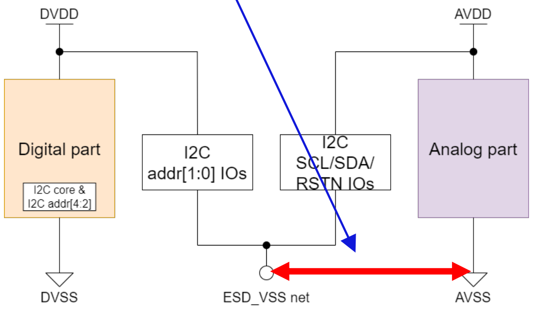
ETROC2.03: three minor modifications at metal layers with wafers on hold at TSMC

Three minor modifications at metal layers implemented in ETROC2.02 in late 2023 (not submitted)
In early 2024, added dummy pads for each pixel, submitted as ETROC2.03 for two wafers on hold at TSMC

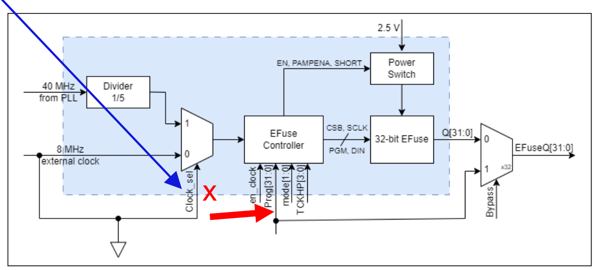
1) Disconnecting the VREF of TS (Temp Sensor).
2) Connecting floating ground net in WS.
3) Change the clock selection for Efuse.







ETROC2.03 chips received in July 2024

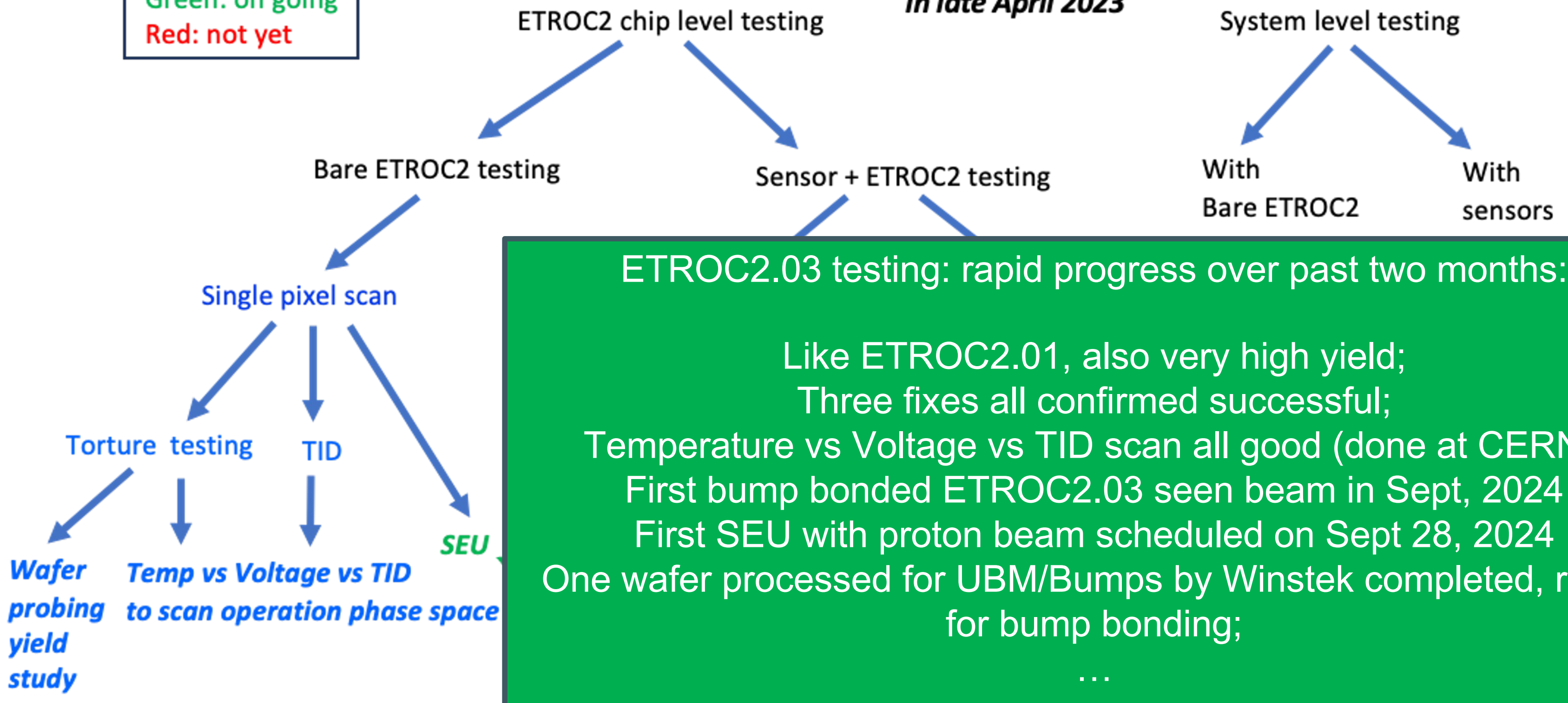


8 dummy/optional pads added, to study bump density vs yield, plan to test with 3 (circled in red)

ETROC2 Testing Road Map

ETROC2.03 chips
received in July 2024

Blue: done
Green: on going
Red: not yet



ETROC2 chips received
in late April 2023

ETROC2 chip level testing

Bare ETROC2 testing

Sensor + ETROC2 testing

Single pixel scan

Torture testing

TID

SEU

Wafer probing yield study

Temp vs Voltage vs TID to scan operation phase space

System level testing

With
Bare ETROC2

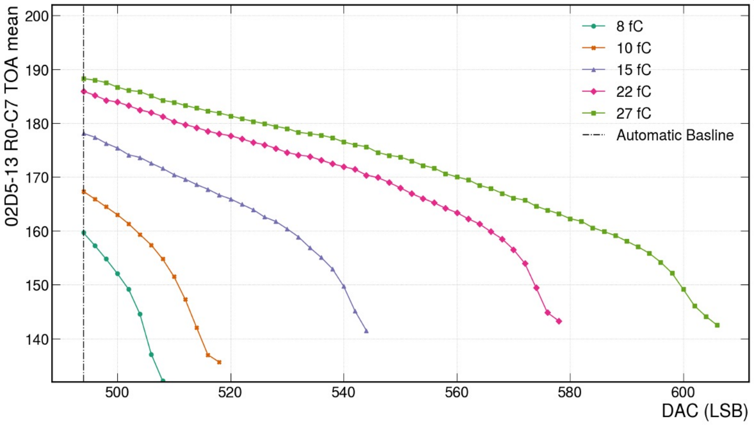
With
sensors

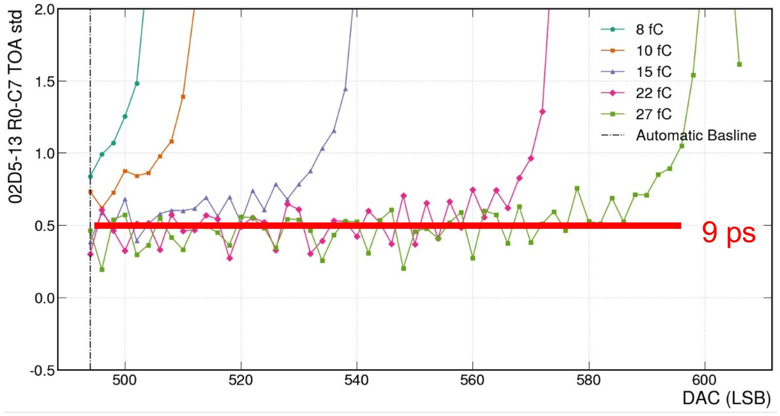
ETROC2.03 testing: rapid progress over past two months:

Like ETROC2.01, also very high yield;
Three fixes all confirmed successful;
Temperature vs Voltage vs TID scan all good (done at CERN);
First bump bonded ETROC2.03 seen beam in Sept, 2024
First SEU with proton beam scheduled on Sept 28, 2024
One wafer processed for UBM/Bumps by Winstek completed, ready for bump bonding;
…

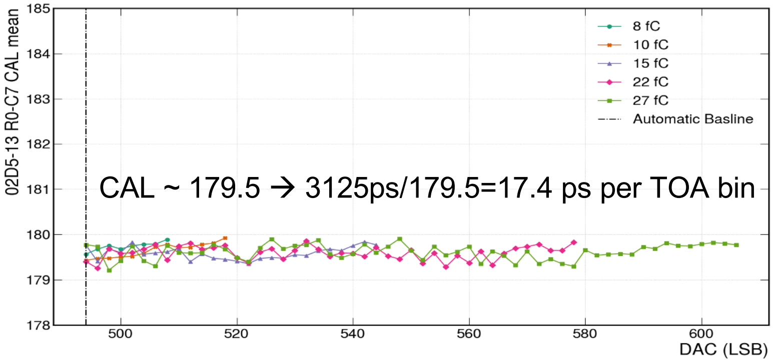
ETROC2.00/2.01 have been extensively tested, ETROC2.03 is being tested as if it is the final version

Charge vs DAC scan after 200 Mrad. (ETROC spec is 100MRad)





ETROC2.01



CAL ~ 179.5 → 3125ps/179.5=17.4 ps per TOA bin

Temperature vs Voltage vs TID scan
done at CERN in Aug 2023 for ETROC2.01
T: from -30C too +30C
V: from 1.3V to 1.0V
TID: from 0 to 200 MRad
All works, pushed TID to 400MRad, still works.

ETROC2.03: repeated the tests in Aug 2024 at CERN and works as well, all the way to 400MRad.

Tested few chips with voltage from 1.0V to 1.4V (analog and digital) and still work

Overview of SEU protection strategy for ETROC2

- Overall readout operation
  - ***Global readout: heavily TMR protected, because it is critical for detector operation***
    - **In addition, CRC code** is used for each data frame/package.
  - Pixel readout: No need for TMR
    - Because the readout architecture is such that all readout is globally coordinated/controlled
      - Save digital power, footprint, and easy for place and route
    - Instead, we use **Hamming code** for each TDC hit data for error detection and correction
- Configuration registers
  - Some configuration bits are critical for detector readout operation
    - Global register could affect whole chip
    - Pixel register would affect only one pixel
  - ***All configuration bits are heavily TMR protected (global and pixel)***
    - Bit-flip should be kept at a minimum level
    - SEU test should pay special attention to them (esp. global configuration bits)
- Status registers
  - Mostly are not used during detector operation
    - ❖ Except of PLL capacitor array configuration and pixelID.
  - They do not affect operation if flipped.
  - Nevertheless, ***they are TMR protected but can be disabled by user***
    - This feature can be used to monitor beam spot during beam testing(16x16 pixels)

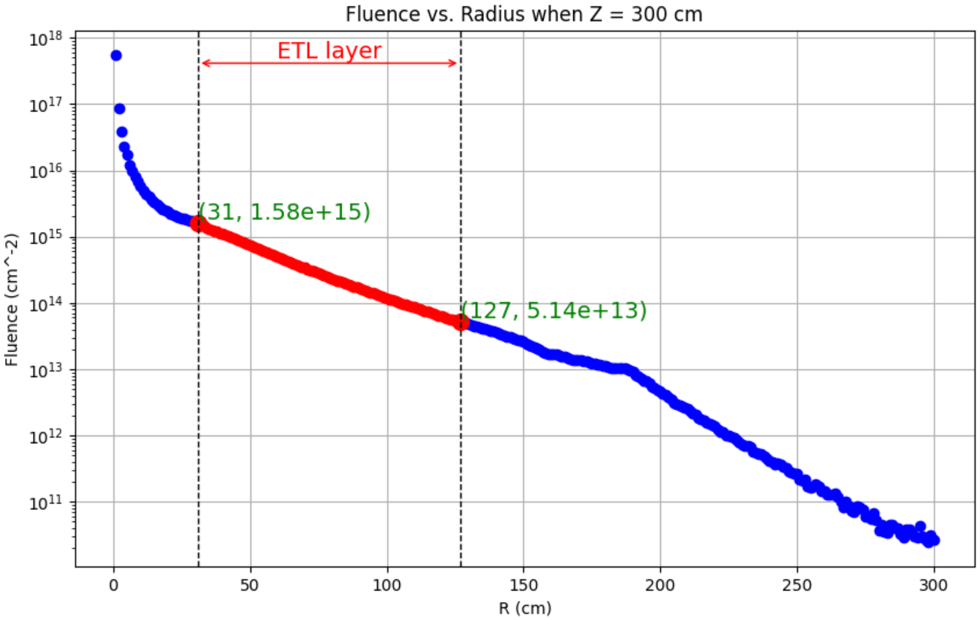
ETROC2 design: everything should be TMRed has been TMRed, and carefully checked/verified at block level.

However, due to lack of person power and expertise, we did not have time to perform full blown TMR verification before submission.

Weighted average fluence for ETL layer

$$F_{avg} = \sum_{i=31}^{127} \frac{F_i \times R_i}{\sum_{k=31}^{127} R_k}$$

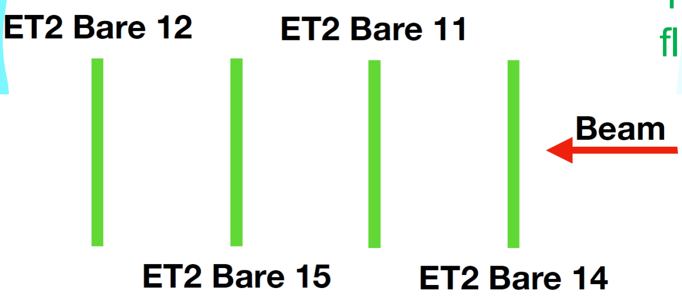
- The larger radius area has more pixels thus has larger weight in calculation the average fluence.
- The weighted average fluence is 2.86×10^{14} h/cm^2



The proton beam SEU campaign

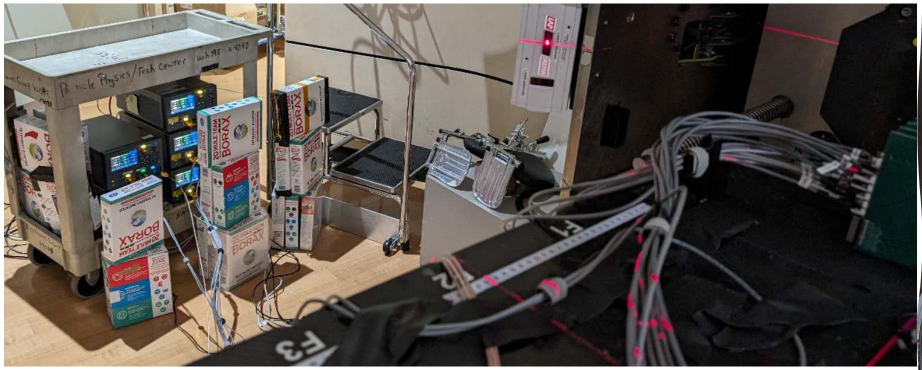
The weighted average ETL fluence is 2.86×10^{14} h/cm^2

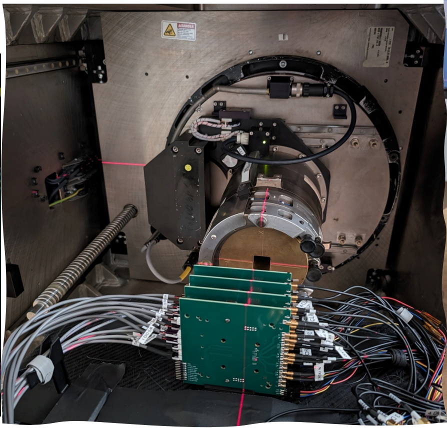
- Beam:
  - Northwestern Medicine Proton Center in Chicago, May 11th, 2024
  - Proton beam @ 217 MeV
  - Beam size 2x2 cm^2 – Measured about 3x3 cm^2
- Setup:
  - 4 “Bare” ETROC chip boards were configurated in Qinj mode. Fixed time delayed L1A commands were sending to ETROC chips during irradiation.
  - ETROC chip was reconfigured before all runs. The I2C configuration/status change were checked for each run



4 “Bare” ETROC chips were irradiated up to 6.82 × 10^{13} p/cm^2 over 17 runs

The setup is rather involved with many long cables … To be improved!



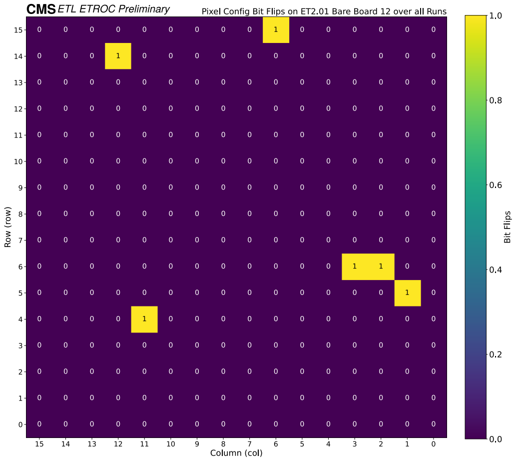


Bit flips of configuration registers

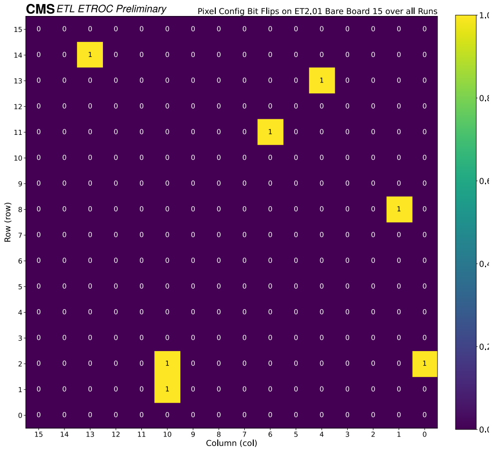
Zero global configuration bit flipping observed (out of 4x32x8 ~ 1024 bits), this is good.

Total of 25 pixel configuration bits flipping observed, only 11 would affect data quality during operation.

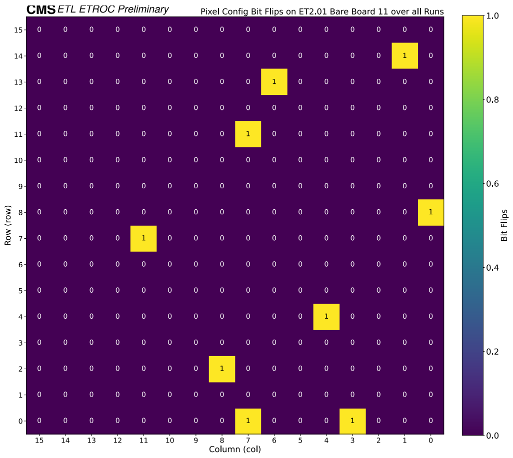

beam



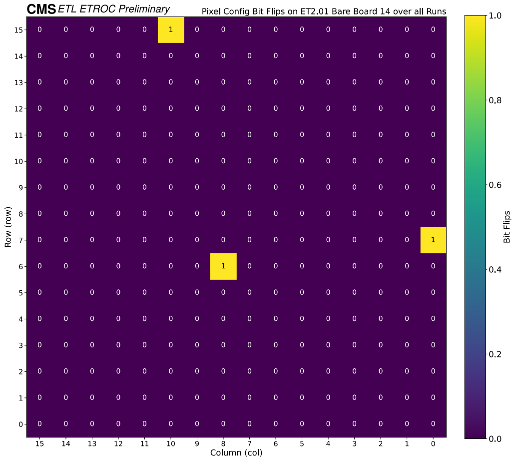
6 bit flips



7 bit flips



9 bit flips



3 bit flips

- The bit flips are randomly distributed on each board
- There is no pixel gets two or more bit-flips for a given upset.
- The pixel is identical at layout level by design.
- Overall 4x256x32x8= 262144 bits of memory cells are exposed to the beam with fluence 6.82x10^{13} p/cm^2.
    - One lpGBT has ~494x8 = ~3952 bits

ETL operation per 24 hours run:
~ 3.22×10^{11} h/cm^2

Cross-section of SEU on pixel configuration

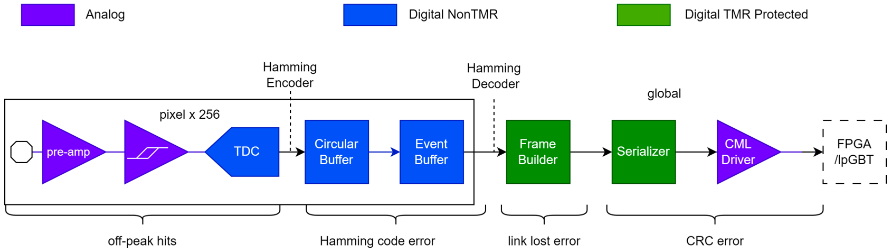
The potential impact on all pixels (7.68 Millions) for ETL is at 10^-5 level for a 24 hours run.
All configuration bits will be reconfigured at the beginning of each run, and can be read-back end of run

Index	Name	Number	Source
1	Pixels impacted in 4 boards (or 1024 pixels)	11	Measurement in beam test
2	Total fluence in proton beam test	6.82×10^{13} p/cm^2	Measurement in beam test
3	Cross section per pixel	**$(1.575\pm0.475)\times10^{-16}$ cm^2**	Compute from 1 and 2
4	Levelled Luminosity	5.00×10^{34} /cm^2/sec	
5	Operation time per run (24 hours)	9×10^{4} sec	
6	Integrated luminosity per run (24 hours)	4.5 fb^{-1}	Compute from 4,5
7	ELT layer fluence (> 20 MeV hadron),4000fb^{-1}	**2.86×10^{14} h/cm^2**	CMS detector simulation
8	Fluence per run (> 20 MeV hadron)	3.22×10^{11} h/cm^2	Compute from 6,7
9	Probability a pixel affected by SEE (pixel only)	$(5.07\pm1.53)\times10^{-5}$	Compute from 3 and 8
10	Total ETL pixels (30 K chips)	7.68×10^{6}	
11	SEE affected pixels per run	**389±117**	Compute from 9 and 10

~ 5x10^-5 level pixels per run

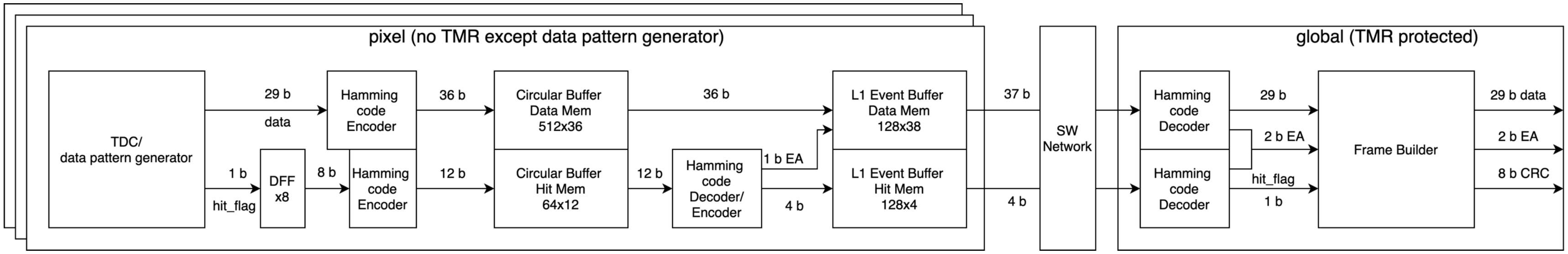
SEU test for readout chain

What types of errors to look for during SEU testing:



- **Off peak hits**: Qinj events are expected to have a fixed TOA and TOT codes. Defines the hits beyond 4 STD deviation of TOT/TOA/CAL code distribution as off-peak hits.
- **Hamming code error**: Check two bits of EA for each TDC data. 00: No error. 01: 1 bit Error, self-corrected in frame builder. 10: 2 bits error, no correction
- **CRC errors**: If the received data frame does not pass the 8-bit CRC check, it is tagged as CRC error
- **Link lost error**: FPGA can not reconstruct data frames or no data frame received.

FRAME HEADER	0	15'H3C5C	2'B00	L1Counter(8B)	TYPE (2B)	BCID (12B)
DATA	1	EA(2B)	Col_ID(4B)	Row_ID(4B)	TDC_DATA/TEST PATTERN(29B)	
FRAME TRAILER	0	CHIPID(17B)	STATUS(6B)	HITS(8B)	CRC (8B)	



Readout error counts during SEU testing

run	duration(sec)	Fluence(p/cm2)	hits#	Off-peak hits	CRC error	Hamming code Error (EA=01)	Hamming code Error (EA=10)	Link Lost error
1	60	0	0	0	0	0	0	0
2	360	0	1954224	4	0	0	0	0
3	10.8	3.90E+10	64080	3	0	0	0	0
4	61	2.24E+11	338016	3	0	0	0	0
5	61	1.24E+12	338432	2	0	0	0	0
6	193	4.03E+12	1077184	0	0	1	0	0
7	208	0.00E+00	1076816	6	0	0	0	0
8	207	0.00E+00	0	0	0	0	0	0
9	67	1.07E+12	1089280	0	0	0	0	0
10	217	4.01E+12	1043072	7	42	26	0	0
11	60	2.26E+12	348112	0	0	0	0	0
12	5	6.41E+10	1072	0	0	0	0	0
13	170	6.39E+12	1076624	2250	5680	0	0	0
14	305	1.14E+13	1749312	0	0	0	0	0
15	300	1.16E+13	1745293	0	0	0	0	0
16	301	1.17E+13	1746528	0	0	0	0	0
17	360	1.42E+13	80400	0	0	0	0	0

Reference runs, no beam

Runs with beam, no CRC error

Runs with beam, with CRC error

Mostly clean,
except potential setup issues,
to be improved.

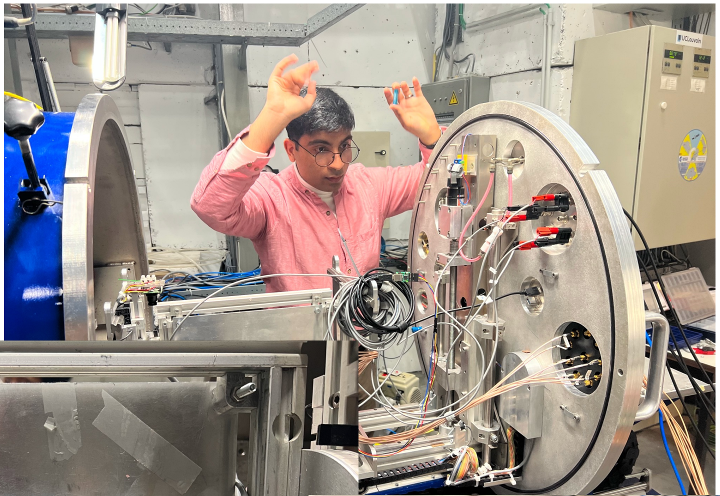
Likely due to (complicated) setup issue (instability), being improved ….

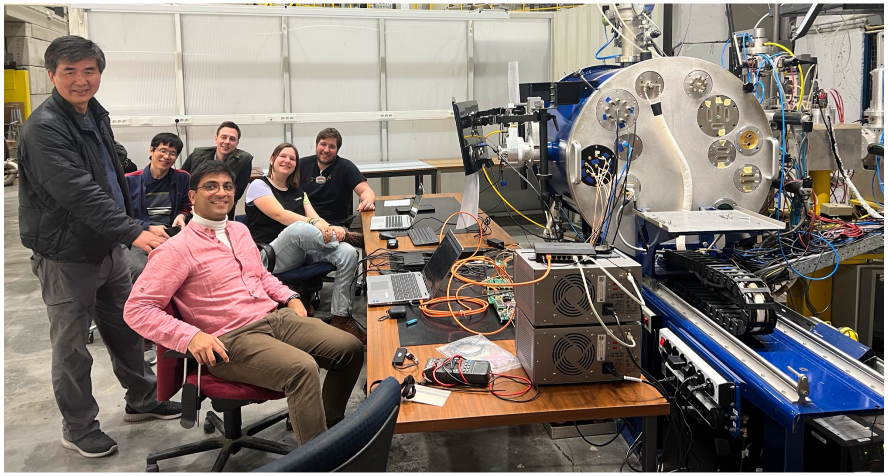
Heavy Ion SEU test at UC Louvain

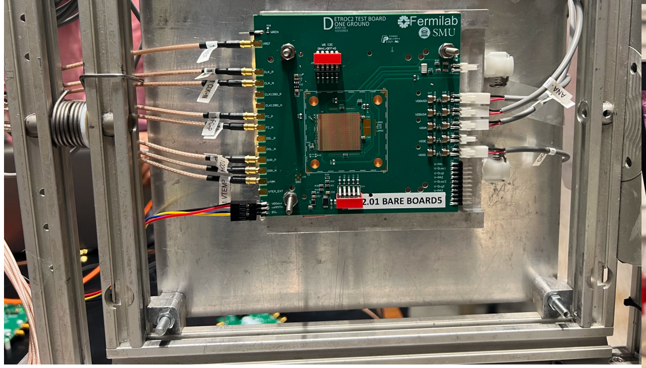
Bits flipping pattern similar with proton beam

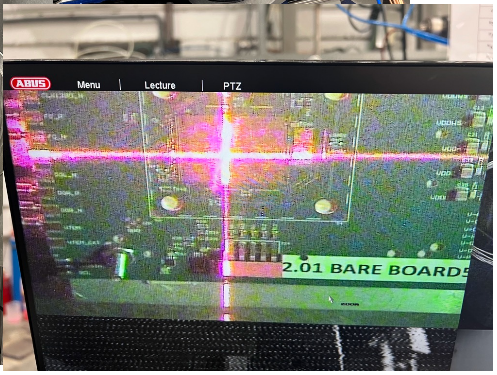
Next time: run additional HI with Al, Cr and Rh, with improved setup

Ion	LET [MeV/mg/cm²]	Fluence [p/cm²]	Time [s]	Important Peripheral Config Bit Flips	Important Pixel Config Bit Flips
Ar	9.9	1.20E+08	8640	0	0
Kr	32.4	4.00E+07	2880	0	1
Xe	62.5	6.50E+07	4935	0	22





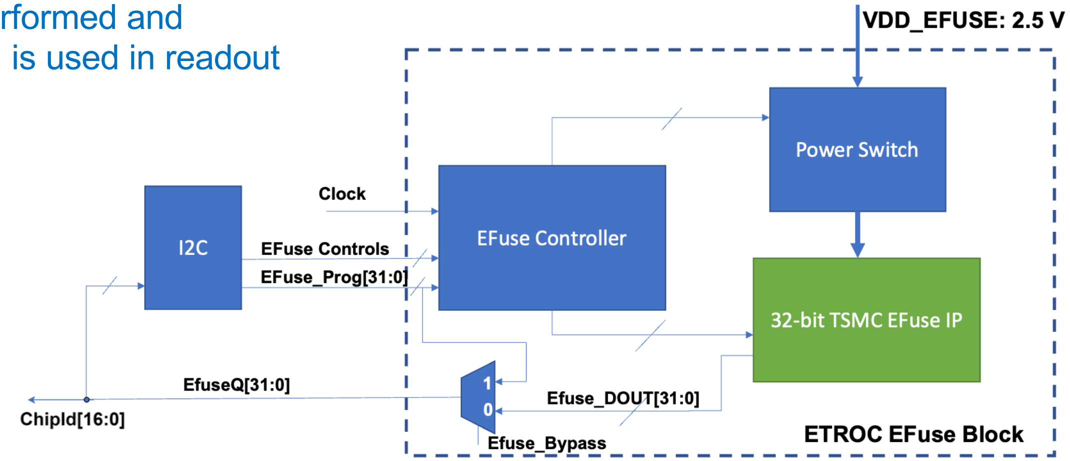




eFuse module in ETROC2.03

- ETROC2 integrated a 32-bit TSMC eFuse IP block to store the chip ID to allow chip tracking from wafer probe testing to end of operation
- The eFuse input clock selection was wrong in ETROC2.00 and fixed in ETROC2.03.

- lpGBT group found that eFuse IP had reliability issue after radiation
  - Less than 1% reading error rate when radiation dose less than 100 MRad
  - About 1.26E-4/bit burning failure rate
- ETROC uses eFuse to store 17 bits of chipID. The remaining 15 bits can be used for FEC code to correct the potential bit error.
  - The FEC code can be calculated and burned into 32 bit of eFuse as well as original chipID.
  - When we read the eFuse, the decoder algorithm is performed and the corrected chipID is written into I2C registers which is used in readout and TMR protected.



ETROC2.03 eFuse register definition

- The codeword is stored in eFuse 32-bit register
- The 32 bits of the word is divided into ChipID(16 bits), reserved bit(1 bit) and error correction bits (15 bits)
- We can further define for production: batch#, wafer #, and chip location on each wafer
  - For example: 3 bits 6 bits, 7 bits
  - Would mark: 8 batch. 2x25=50 wafers ~120 chips per wafer

Efuse ChipID can help us to keep track each ETROC chips for production:

From cradle to grave

More importantly, helps us to keep track of which sensor is bump bonded with which ETROC

From bonding to grave

15 bits of error correction code: 0x1F5E

reserved bit

16 bits of chipID:0x0001

0	0	1	1	1	1	1	0	1	0	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

Initial experience: The first 12 ETROC2.03 chips with eFuse burned

First ETROC2 engineering run, from first ETROC2.03 wafer (for testing purpose)

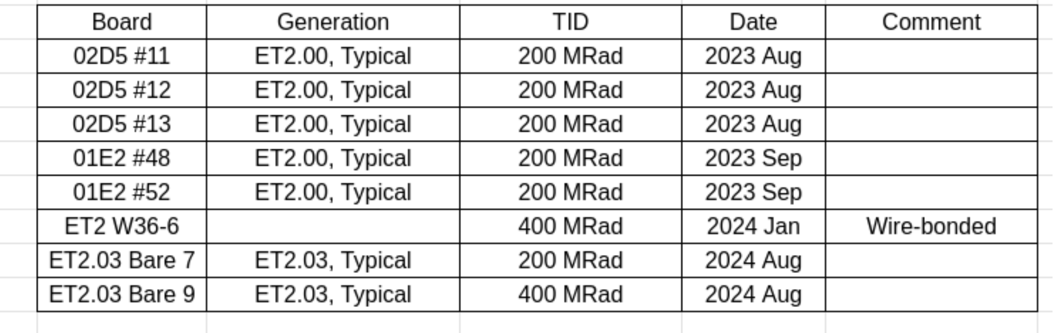
ChipID (16b)	Reserve bit(1b)	ECC(15b)	eFuse Word (32b)
0x0001	0	0x0FAF	0x1F5E0001
0x0002	0	0x1F5E	0x3EBC0002
0x0003	0	0x10F1	0x21E20003
0x0004	0	0x3EBC	0x7D780004
0x0005	0	0x3113	0x62260005
0x0006	0	0x21E2	0x43C40006
0x0007	0	0x2E4D	0x5C9A0007
0x0008	0	0x7D78	0xFAF00008
0x0009	0	0x72D7	0xE5AE0009
0x000A	0	0x6226	0xC44C000A
0x000B	0	0x6D89	0xDB12000B
0x000C	0	0x43C4	0x8788000C

ChipID = 7 chip has been tested to 200MRad, no efuse bit changed during TID

ChipID = 9 chip has been tested to 200 and then 400MRad, no efuse bit changed during TID

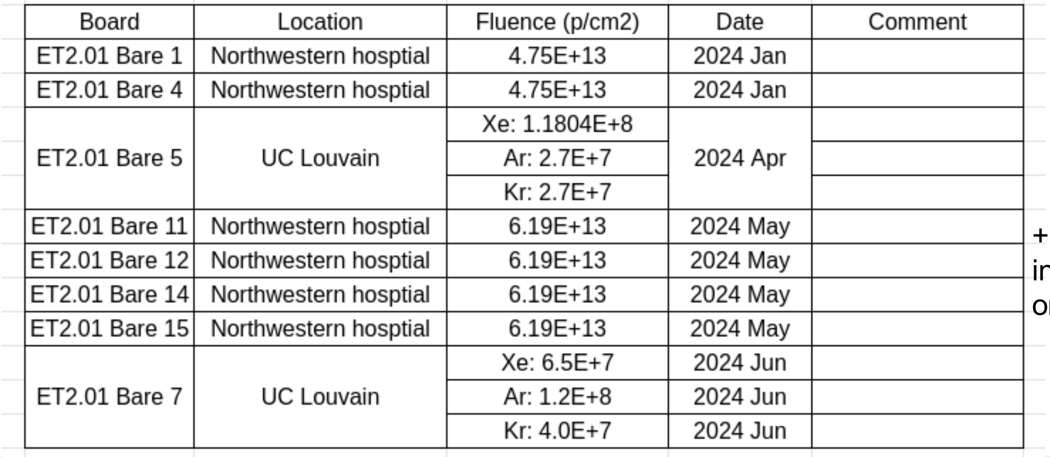
Number of ETROC2 chips tested so far

TID tests



Board	Generation	TID	Date	Comment
02D5 #11	ET2.00, Typical	200 MRad	2023 Aug	
02D5 #12	ET2.00, Typical	200 MRad	2023 Aug	
02D5 #13	ET2.00, Typical	200 MRad	2023 Aug	
01E2 #48	ET2.00, Typical	200 MRad	2023 Sep	
01E2 #52	ET2.00, Typical	200 MRad	2023 Sep	
ET2 W36-6		400 MRad	2024 Jan	Wire-bonded
ET2.03 Bare 7	ET2.03, Typical	200 MRad	2024 Aug	
ET2.03 Bare 9	ET2.03, Typical	400 MRad	2024 Aug	

SEU tests



Board	Location	Fluence (p/cm2)	Date	Comment
ET2.01 Bare 1	Northwestern hosptial	4.75E+13	2024 Jan	
ET2.01 Bare 4	Northwestern hosptial	4.75E+13	2024 Jan	
ET2.01 Bare 5	UC Louvain	Xe: 1.1804E+8	2024 Apr	
		Ar: 2.7E+7		
		Kr: 2.7E+7		
ET2.01 Bare 11	Northwestern hosptial	6.19E+13	2024 May	
ET2.01 Bare 12	Northwestern hosptial	6.19E+13	2024 May	
ET2.01 Bare 14	Northwestern hosptial	6.19E+13	2024 May	
ET2.01 Bare 15	Northwestern hosptial	6.19E+13	2024 May	
ET2.01 Bare 7	UC Louvain	Xe: 6.5E+7	2024 Jun	
		Ar: 1.2E+8	2024 Jun	
		Kr: 4.0E+7	2024 Jun	

+ 8 ETROC2.03
in proton beam for SEU
on Sept 28, 2024.

In total,

8 ETROC2 wafers have been probe tested (~116 dies/wafer)

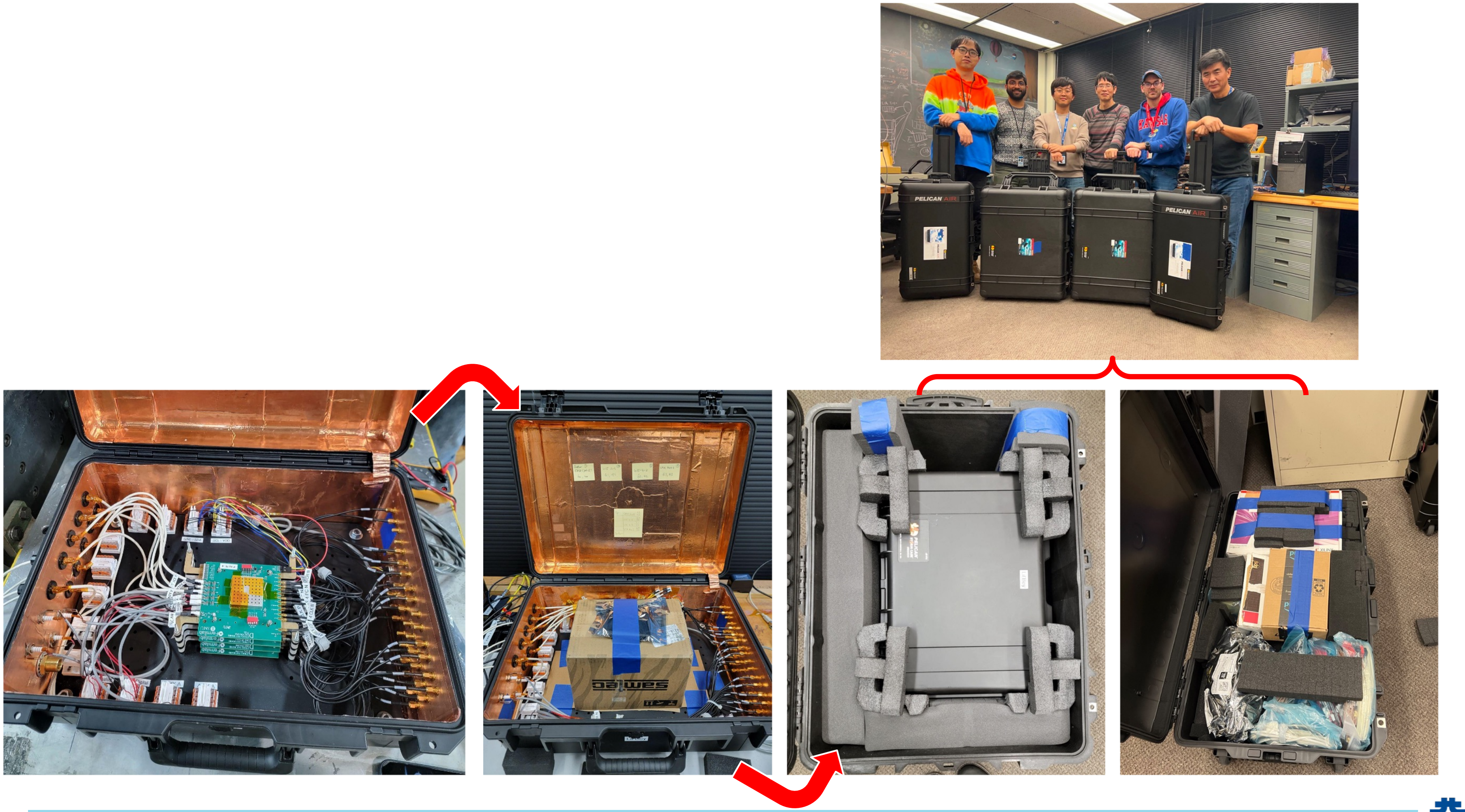
163 chips have been tested on ETROC test boards;

8 chips tested for TID (200-400MRad)

16 chips tested for SEU

Fermilab

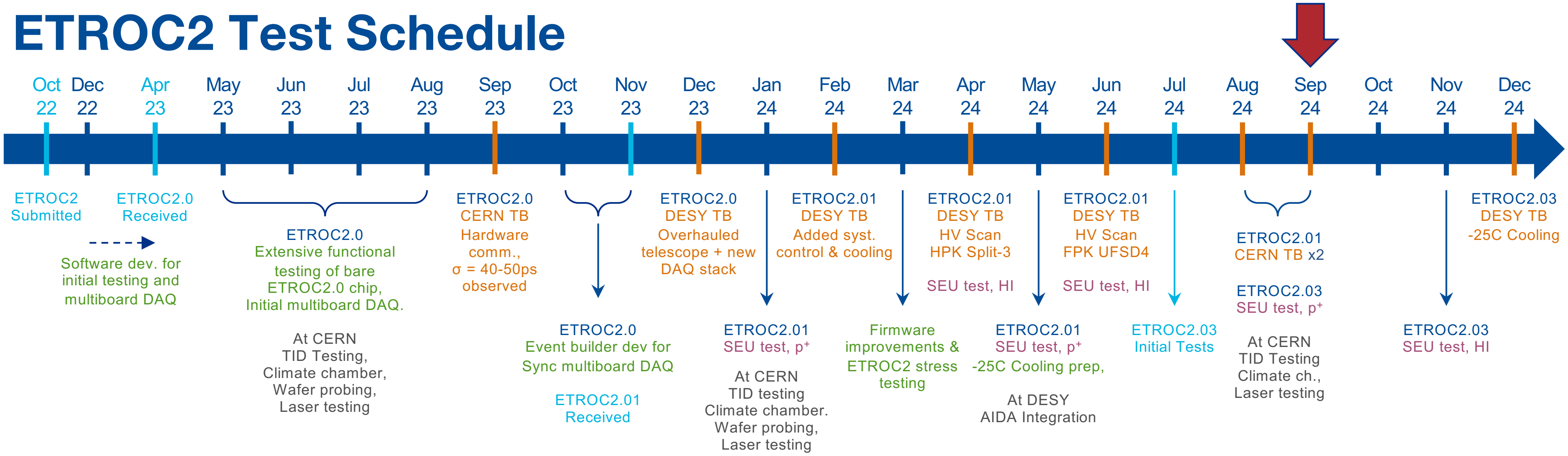
How does one travel with precision timing telescopes?



Many people involved in the ETROC tests (with strong support from CERN and DESY!)

ETROC integration with AIDA telescope at DESY

ETROC2 Test Schedule



ETROC2 Submitted

ETROC2.0 Received

Software dev. for initial testing and multiboard DAQ

ETROC2.0 Extensive functional testing of bare ETROC2.0 chip, Initial multiboard DAQ.

At CERN TID Testing, Climate chamber, Wafer probing, Laser testing

ETROC2.0 CERN TB Hardware comm., σ = 40-50ps observed

ETROC2.0 Event builder dev for Sync multiboard DAQ

ETROC2.01 Received

ETROC2.0 DESY TB Overhauled telescope + new DAQ stack

ETROC2.01 SEU test, p^+

At CERN TID testing Climate chamber. Wafer probing, Laser testing

ETROC2.01 DESY TB Added syst. control & cooling

Firmware improvements & ETROC2 stress testing

ETROC2.01 DESY TB HV Scan HPK Split-3

SEU test, HI

ETROC2.01 SEU test, p^+ -25C Cooling prep,

At DESY AIDA Integration

ETROC2.01 DESY TB HV Scan FPK UFSD4

SEU test, HI

ETROC2.03 Initial Tests

ETROC2.01 CERN TB x2

ETROC2.03 SEU test, p^+

At CERN TID Testing Climate ch., Laser testing

ETROC2.03 SEU test, HI

ETROC2.03 DESY TB -25C Cooling

ETROC2 Testing Summary…

- ETROC2.00 and 2.01 have been extensively tested over the past year, performance meets/exceeds specifications
- ETROC2.03 testing on going, so far so good (all three minor fixes confirmed successful)

To be done: testing with irradiated sensors in beam; Improving SEU test setup for one more round of testing, improving bump bond yield.

Special thanks to the wonderful support provided by CERN/DESY for our testing

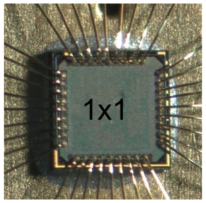
Backup slides

ETROC Early Prototyping Phase

Sept 2018 Dec 2018 May 2019 Aug 2019 March 2020 May 2020 July 2021 Sept 2021 …

Project started

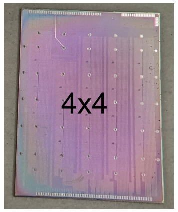
ETROC0 submitted



Preamp + discriminator

ETROC1 submitted

Covid

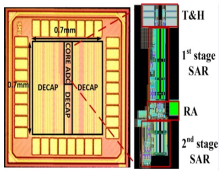


Preamp + discriminator + TDC
4x4 H-tree clock distribution

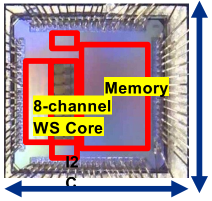
ETROC2: 8x8 → 16x16

Decision to go for full size full functionality ETROC2,
Delay submission and add few test chips …

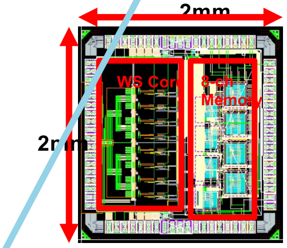
Single channel
ADC submitted



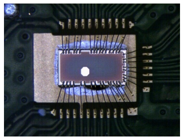
8-channel ADC
Waveform Sampler (WS1)
submitted



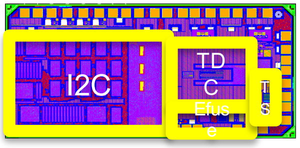
Rad-hard version of
Waveform Sampler (WS2)
submitted

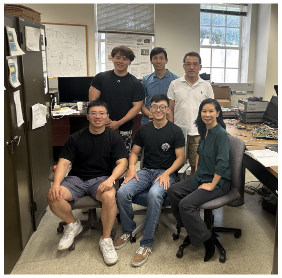


ETROC-PLL mini ASIC
submitted



I2C Test chip submitted





Total of 7 small chips, all successful

All analog blocks have been silicon proven in test chips;
ETROC2 FPGA emulator: has verified digital readout and system interfaces

ETROC2 was submitted (Oct 21, 2022), testing started in later April 2023

Design team: FNAL/SMU/LBNL/UCSB
Testing team: FNAL/SMU/UIC/UCSB/Lisbon/IFCA/KUL with students from KSU/KU

Most recent ETROC1 paper: https://doi.org/10.1088/1748-0221/19/09/p09019
ETROC2 paper(s) draft in progress

ETROC power consumption estimate vs measurements

ETROC0/ETROC1 testing results

ETROC0/1 design simulation results

Table
from TDR

Circuit component	Power per channel [mW]			Power per ASIC [mW]	
Preamplifier (low-setting)	0.67	0.76	0.74	171.5	189.4 (preamp low power)
Preamplifier (high-setting)	1.25	1.31	1.27	320	325.1 (389, the highest power)
Discriminator	0.71	0.87	0.84	181.8	215.0
TDC	0.2	0.07	0.1	51.2	25.6
SRAM (→ memory)	0.35	0.25 (sim)		89.6	64.0
Supporting circuitry	0.2	0.2		51.2	51.2
Global circuitry		(reserve)		200 →	234.5

Sum: ~780/915/980 mW (low/high/highest power)
Use 980mW & add 20% for worst case.

- Measurements agree with simulation of ETROC0 and 1 design
  - ***But should assume up to 20% variation with real production***
  - Note: preamp highest setting (4th gear) power is 1.52mW (measured), the high-setting above is the 3rd gear.

ETROC2 measurements on three bump bonded chips (room temperature):

Earlier estimate during design stage:

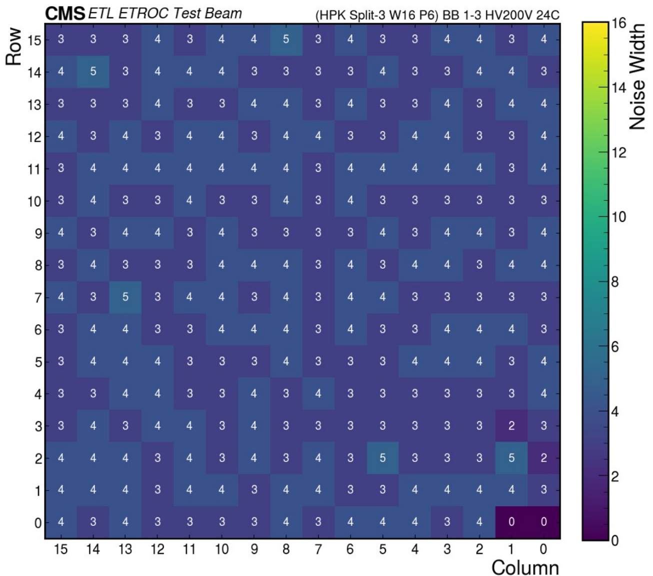
Typical chip low power:	346/138 mA analog/digital	→ 581 mW	↔	780mW (preamp low power)
Corner FFF low power:	402/247 mA	→ 779 mW		
Typical chip high power:	477/138 mA analog/digital	→ 738 mW	↔	980mW (preamp high power)
Corner FFF high power:	525/247 mA	→ 926 mW		

The ETROC2 power consumption meets ETL requirements (the original estimate was conservative enough)
Much of the power saving was due to extensive optimization of the digital activities (to minimize noise)

Lower temperature → lower power

Noise Widths during HV Scan for HPK Split-3 + ETROC2.00

Approaching Breakdown



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1	4	4	4	3	4	4	3	4	4	3	3	4	4	4	4	3
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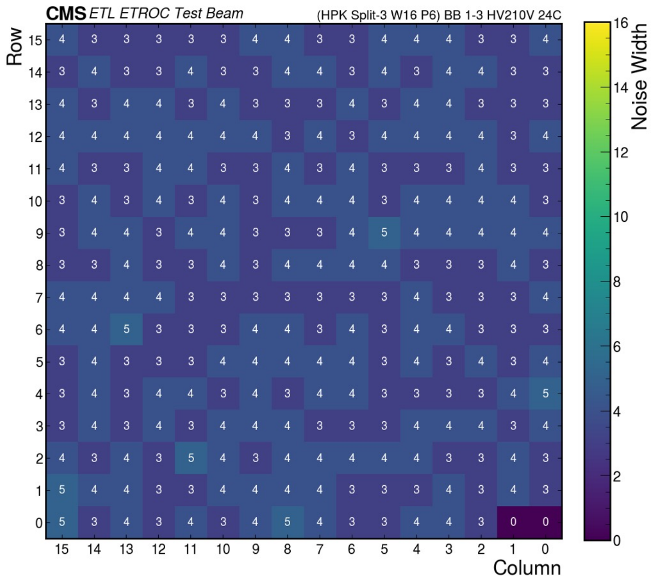
200 V



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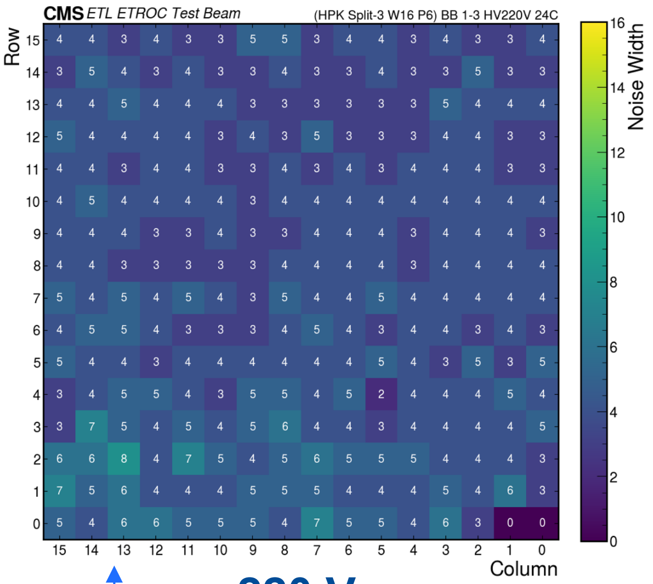
0	5	3	4	3	4	3	4	5	4	3	3	4	4	3	0	0

210 V



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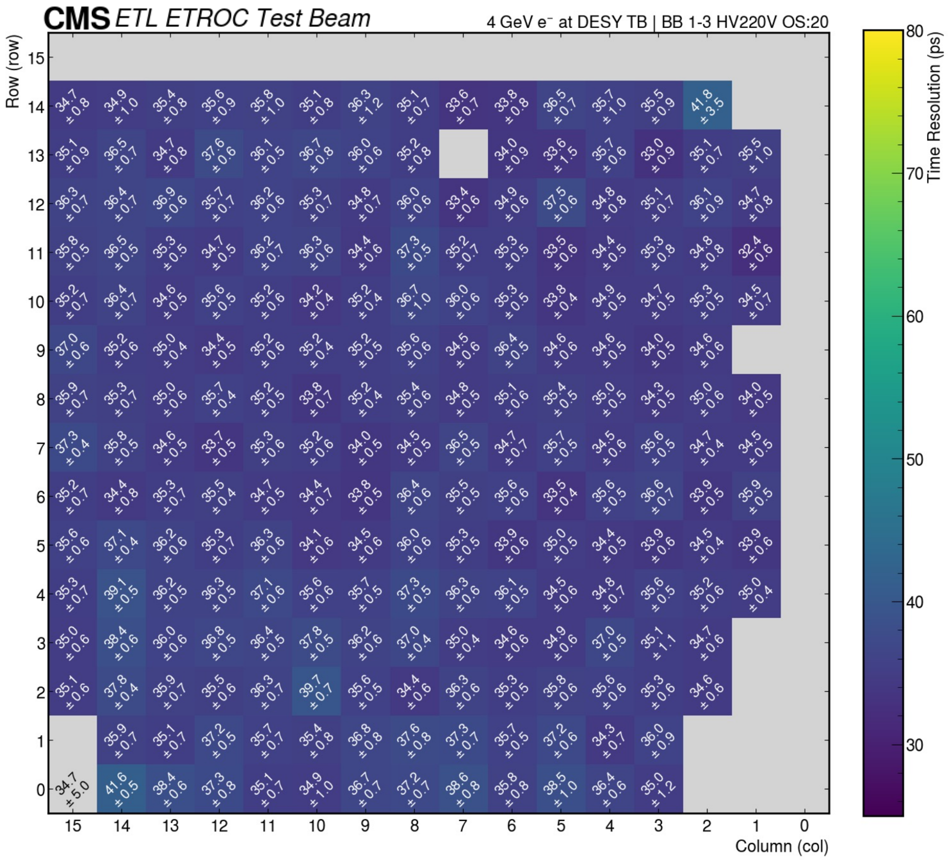
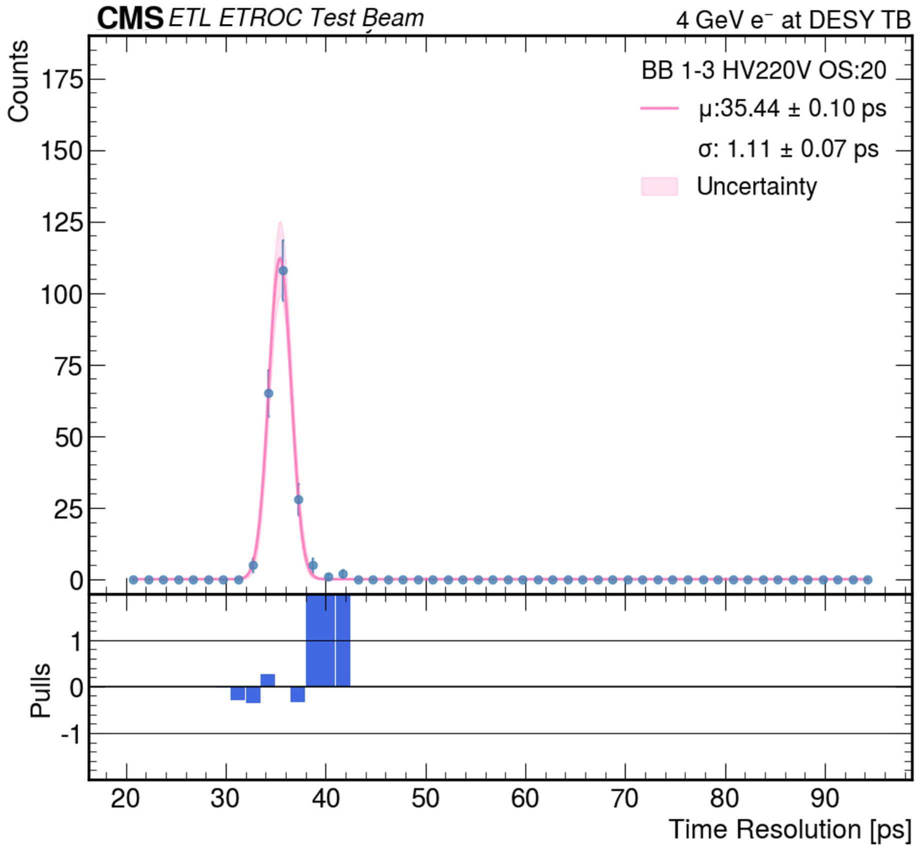
0	5	4	6	6	5	5	5	4	7	5	5	4	6	3	0	0

220 V

Sensor getting close to break down, some pixel noise width gets “warm”

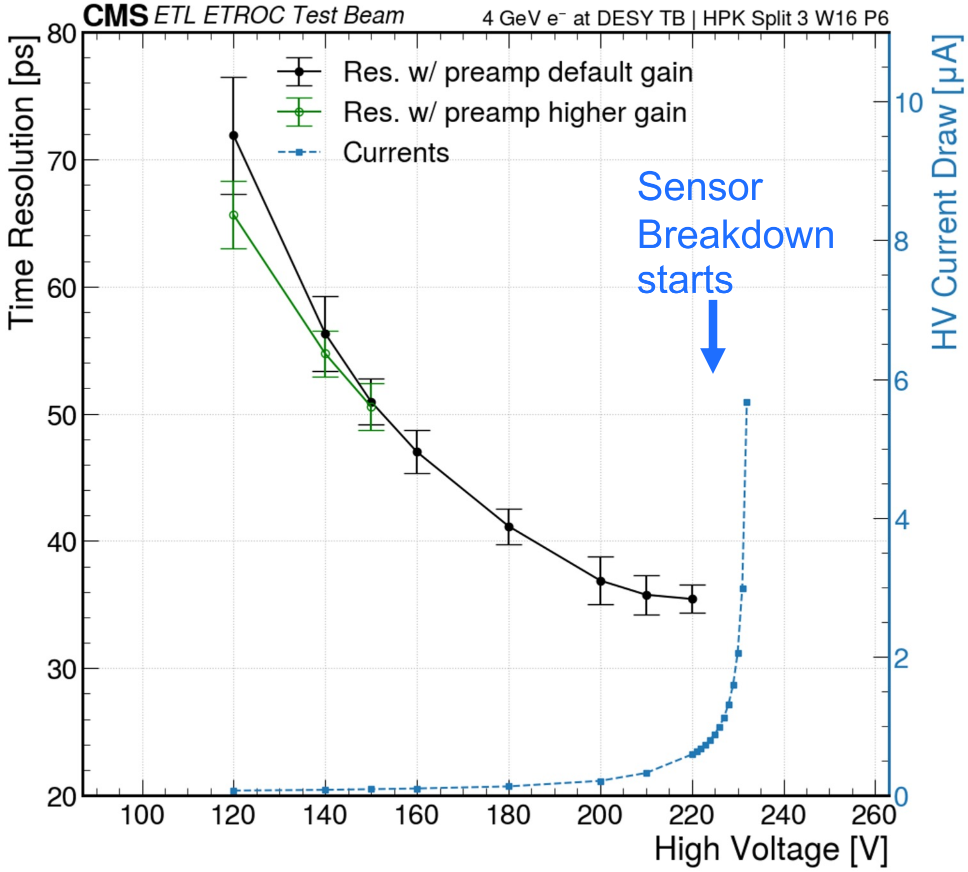
220V HV point for HPK Split-3 + ETROC2.00



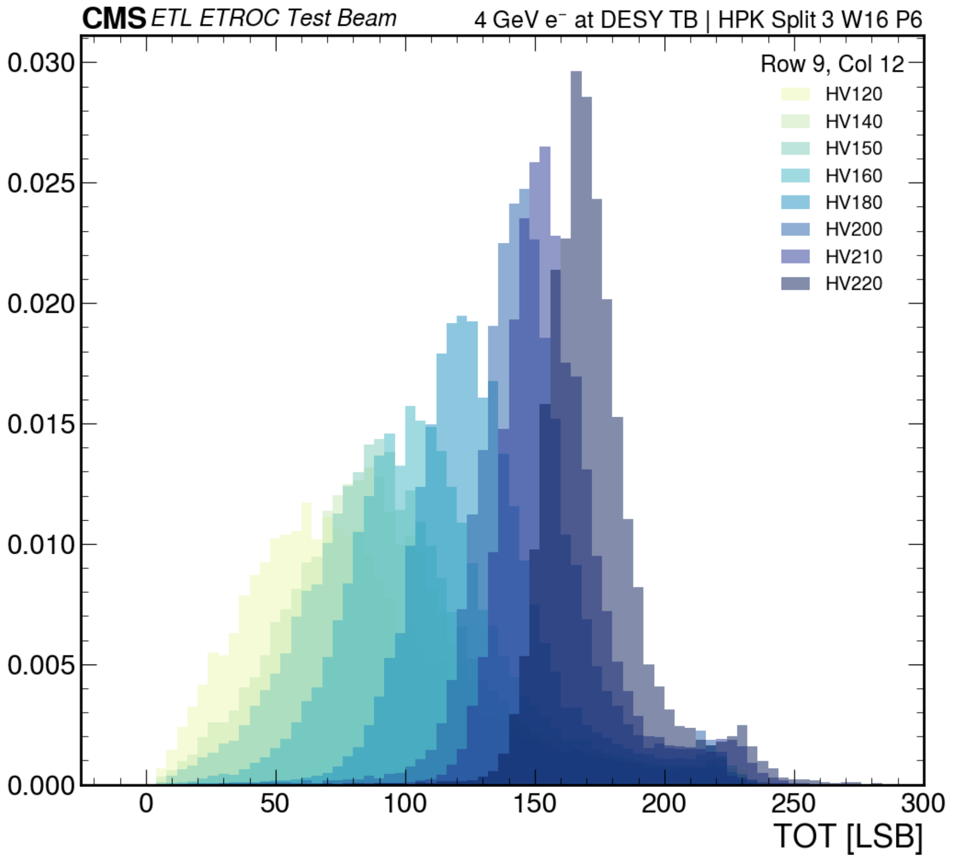


Pixel resolution map over 16x16 array

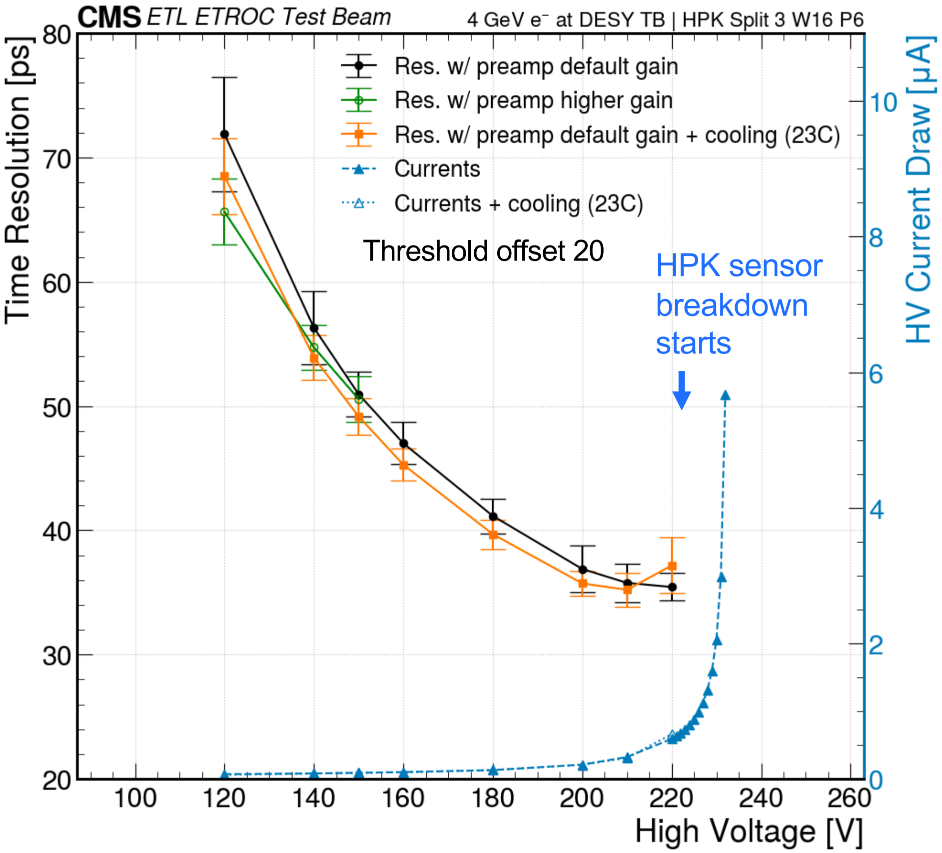
HV Scan for HPK Split-3 + ETROC2.00: w/o temp control



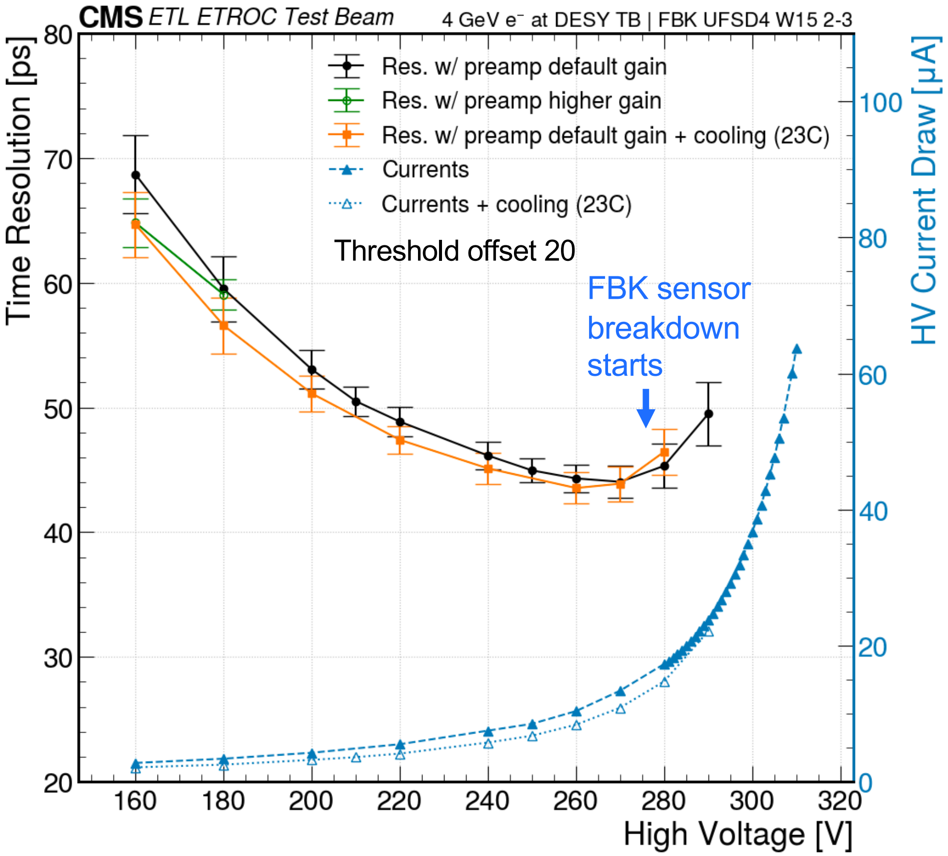
Sensor Breakdown starts



HV Scans for ETROC2: HPK vs FBK (preamp default vs high gain)



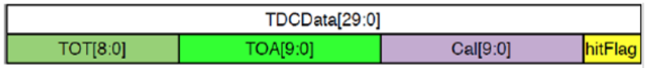
HPK sensor breakdown starts



FBK sensor breakdown starts

Temp control improves ~ few ps,

ETROC TDC



TDCData[29:0]			
TOT[8:0]	TOA[9:0]	Cal[9:0]	hitFlag

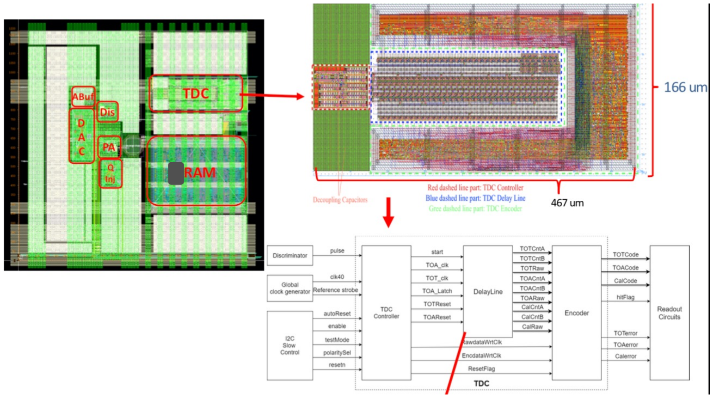
hitFlag: discriminator is fired or not

- ❑ bin= T3/Cal_code
- ❑ TOA=12.5 - bin*TOA_code

T3 is programable with 3.125 ns by default.

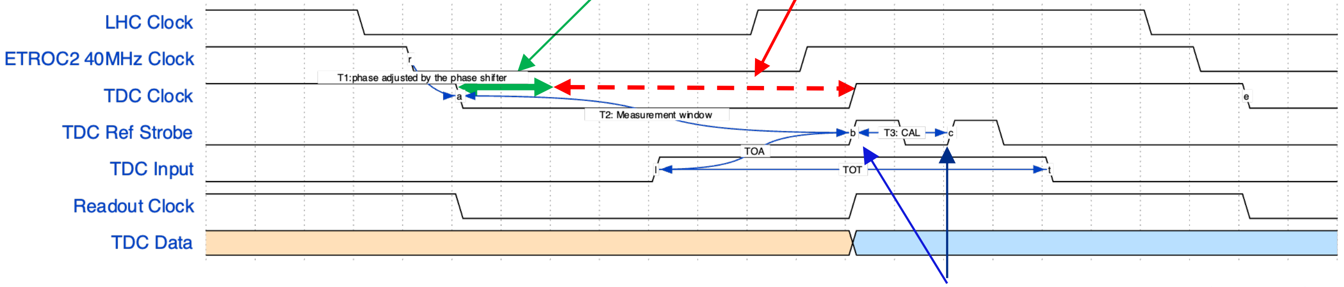
1984 IEEE TRANSACTIONS ON NUCLEAR SCIENCE, VOL. 68, NO. 8, AUGUST 2021

A Low-Power Time-to-Digital Converter for the CMS Endcap Timing Layer (ETL) Upgrade



Normal TOA window for prompted particles from collisions

extended TOA window for long lived particles



Double time-stamps for self-calibration "on the fly", to calibrate TDC bin size in real time for every hit (very important feature of this TDC design)

https://ieeexplore.ieee.org/document/9446843

Less sensitive to temperature changes, IR drops, radiation etc…

One ETROC2.03 wafer processed UBM/bumps/thinning/dicing

Chips received from Winstek on Sept 12, 2024