Contribution ID: **59** Type: **Oral**

The testing and performance of the ETROC2 for CMS MTD Endcap Timing Layer (ETL) upgrade

Tuesday 1 October 2024 14:20 (20 minutes)

The Endcap Timing ReadOut Chip (ETROC) is designed to process LGAD signals with time resolution down to ˜ 40-50ps per hit. The ETROC2 is the first full size prototype design fully compatible with the final chip specifications for CMS ETL. The ETROC2 chips have been extensively tested over the past year since May 2023, with laser, hadron beam at CERN and electron beam at DESY, with temperature vs voltage vs TID scan, with proton beam and heavy ion beam for SEU and wafer probe testing and stress testing using charge injections. The ETROC2 design and test results will be presented.

Summary (500 words)

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The ETROC2 is the first full size (16x16) and full functionality prototype design and its dimensions are 21mm x 23mm making it one of the largest chips in HEP. It is designed to process LGAD signals with time resolution down to ˜ 40-50ps per hit in order to achieve ˜30-35ps per track with two-layer detectors. The analog front-end design for each pixel is based on the ETROC1 pixel design, with a new feature added for the on-chip and in-pixel auto discriminator threshold calibration. The pixel and global readout design is entirely new with a switch-cell based network approach, with built-in self-testing capability with digital pattern generation within each pixel, as well as the capability to provide a coarse map of delayed hits continuously for every bunch crossing for monitoring or Level 1 triggering purposes.

The ETROC2 engineering run included 20 wafers in two lots, with 14 typical wafers (6 wafers on hold), and 6 corner wafers (FFF and SSS). The testing of ETROC2 is divided into two categories. The first category is the testing of bare ETROC2, and the second category is the testing of ETROC2 bump bonded with 16x16 LGAD sensors.

The first category of the testing of bare ETROC2 includes charge injection with stress testing and IR drop study, temperature vs voltage vs TID scan in 2023 and early 2024 at CERN, wafer probe testing on 8 typical and corner wafers in 2023 at CERN, and SEU testing using both proton beam and heavy ion beams in Jan and April of 2024 with two more SEU tests scheduled in May (proton beam) and June (heavy ion beam at UCLouvain) of 2024. The bare ETROC2 testing results so far are promising and the timing performance meets the design specification, the wafer probe testing shows that the yield is at 97% level and the ETROC2 has passed 400 Mad TID testing (with specification at 100 MRad). Three minor issues have been identified during bare ETROC2 testing and all three have been fixed with wafers on hold.

The second category of testing of bump bonded ETROC2 with LGAD sensors includes using laser and hadron beam at CERN and electron beam at DESY, with a few beam tests performed between Sept 2023 and April of 2024, with improvements of the ETROC2 beam telescope setup and the telescope is being integrated with the AIDA telescope at CERN and DESY. Three more beam tests are scheduled in May (DESY) and June (DESY) and Aug (CERN) in 2024, to take advantage of the AIDA telescope tracking information. The beam test results so far have shown that the time resolution meets the requirements, and more extensive testing will be done over the next three months (May to Aug 2024) with the goal to also study the bump bonding options.

In this presentation, the main ETROC2 design features along with the testing results will be summarized, followed by lessons learned from ETROC2 design, fabrication, bump bonding and testing experiences.

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Session Classification: ASIC

Track Classification: ASIC