Development of the MOSAIX chip for the ALICE ITS3 upgrade

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1 Abstract (max 100 words)

Following the ALICE ITS3 detector development line of wafer-scale monolithic stitched pixel detector prototypes (MOSS & MOST) in the TPSCo. 65nm CMOS imaging technology, the MOSAIX chip is the prototype of the final full-size and full-functionality ITS3 sensor. MOSAIX has a die size of 26.6 x 1.96 cm^2 with $\geq 94\%$ of active area. It has 144 sensor tiles which can be powered down individually to compensate for manufacturing defects, where each tile has 69.2k pixels with a 22.8 x 20.8 μm^2 pixel size. This contribution highlights the lessons learnt from the predecessors MOSS and MOST chips, summarizing the architectural decisions of the MOSAIX implementation and focusing on the adopted yield enhancement techniques.

2 Summary (max 500 words)

The ALICE collaboration develops a novel and considerably improved vertexing detector, the ITS3, to replace the three innermost layers of the Inner Tracker System during the LHC Long Shutdown 3 at CERN. This upgrade aims to achieve two primary objectives: reduce the material budget per layer to 0.07 $\%X_0$ and position the first layer closer to the interaction point at 19 mm. Each layer is composed of segments of a wafer-scale monolithic pixel sensor chip measuring 26.6 x 1.96 cm^2 with an active area of ≥ 94 %.

Given the size of the wafer-scale sensor it cannot be expected to be produced free of manufacturing defects. In order to study the yield of such devices the MOSS (Monolithic Stitched Sensor) and MOST (Monolithic Stitched Sensor with Timing) prototypes were submitted as proofs of concept using the TPSCo. 65nm CMOS imaging process with stitching technology. Both chips employ a granular power domain scheme which allows to switch off sections of the chip in case of manufacturing defects which would otherwise render the chip inoperable. The MOSS employs a coarse power modularity but implements conservative design rules and the MOST has a fine power modularity but uses minimum spacing design rules.

The MOSAIX chip is the second generation of the stitched sensor development and is the full-size, full-functionality prototype of the final ITS3 sensor ASIC. Following the lessons learned from its predecessors, each MOSAIX contains 144 identical tiles in the sensitive region which can be independently powered, controlled, and read out, providing a granular control of 0.7 % of the chip's sensitive region. Each tile features a pixel matrix array of 444 x 156 pixels with a pixel size of 22.8 x 20.8 µm^2. The chip's substrate can be reversed biased enhancing the sensor performance by decreasing the input capacitance which effectively increases the signal over noise ratio. The analog front-end biasing is self-contained within each sensor tile. The pixel matrix is read out via a double-column priority encoder with zero suppression, and the pixel hit data is transmitted over 26 cm on-chip at 160 Mb/s to a data aggregator positioned on the chip's left endcap. To comply with the power budget of 40 mW/cm^2, custom standard cells were designed to both increase the yield and decrease the leakage. The digital periphery is entirely triplicated for yield improvement and robustness against Single-Event-Effects. The sensor tile is powered via on-chip switches and a monitoring ADC on the left endcap allows for short circuit detection during power ramp-up by monitoring the power supply of each tile. Two slow control paths are implemented, separating the functions of chip control and power management. Configurable data routing options provide redundancy both on- and off-chip with serializer line rates of 10.24 Gb/s or 5.12 Gb/s for off-chip data transmission.

This contribution highlights the lessons learned from the predecessors MOSS and MOST chips, summarizing the architectural decisions of the MOSAIX implementation and focusing on the adopted yield enhancement techniques.

3 Extended summary (700 words)

The ALICE collaboration develops a novel and considerably improved vertexing detector, the ITS3, to replace the three innermost layers of the Inner Tracker System during the LHC Long Shutdown 3 at CERN. The primary goals of the upgrade are to reduce the material budget (0.07 %X_0 per layer) and to place the first out of three layers closer to the interaction point (19 mm). The ITS3 detector consists of three 50 µm thick true cylindrical layers which are based on bent wafer-scale monolithic pixel sensor chips. Each layer is composed of 2 half layers which vary in width based on its proximity to the interaction point. Each half layer contains of 3, 4, or 5 detector segments measuring 26.6 x 1.96 cm^2 with an active area of $\geq$ 94 %. The ITS3 electro-mechanical integration scheme only allows data and power to be provided via the short segment edges (1.96 cm) imposing a chip integration challenge.

Given the size of the wafer-scale sensor it cannot be expected to be produced free of manufacturing defects. The first step towards the development of such a wafer-scale monolithic pixel sensors was done using the TPSCo. 65nm CMOS imaging process with stitching technology. In order to study stitching techniques, interconnects, design for manufacturing and ultimately yield, the

MOSS (Monolithic Stitched Sensor) and MOST (Monolithic Stitched Sensor with Timing) prototypes were submitted as proof of concept. To compensate for the production of regional failures which would otherwise render the chip inoperable, a granular power domain scheme architecture was adopted for both chips. The MOSS employs a coarse power modularity but implements conservative design rules, where the MOST has a fine power modularity but uses minimum spacing design rules.

The MOSAIX chip is the second generation of the stitched sensor development and is the full-size, full-functionality prototype of the final ITS3 sensor ASIC. It integrates valuable insight and lessons learnt from its predecessors, MOSS and MOST, amongst them how to design the adopted granular power scheme architecture which foresees the option to power down and operate independent tiles. Each segment contains 144 identical tiles in the sensitive region which can be independently powered, controlled, and read out, providing a granular control of 0.7 % of the chip's sensitive region. Each tile features a pixel matrix array of 444 x 156 pixels with a pixel size of 22.8 x 20.8 μm^2. The circuitry is designed to enable reverse bias of the substrate, enhancing the sensor performance by decreasing the input capacitance and effectively increasing the signal over noise ratio. The analog front-end biasing is self-contained within each sensor tile. The pixel matrix is read out via a double-column priority encoder with zero suppression, and the pixel hit data is transmitted on-chip over 26 cm at 160 Mb/s to the data aggregator positioned on the chip's left endcap. To comply with the power budget of 40 mW/cm^2, custom standard cells were designed to both increase the yield and decrease the leakage. Furthermore, the digital periphery is entirely triplicated for yield improvement and robustness against Single-Event-Effects. The sensor tile is powered via on-chip switches, and the local power of the tile is derived from the global power distribution. A monitoring ADC on the short edge allows monitoring of the pixel matrix biasing and the local power supply of the 144 sensor tiles, detecting shorts at power-on.

The segment readout in the left endcap receives the data stream of the 144 sensor tiles. To increase on- and off-chip redundancy, the data routing is configurable via 3 out of 8 serializers using a line rate of 10.24 Gb/s or 6 out of 8 serializers configured to operate at 5.12 Gb/s.

Each serial stream is encoded using the lpGBT protocol and is directly connected off-chip to a radiation-hard opto-electronic $VTRX^+$. The on-chip lpGBT core is inherited from the lpGBT project, facilitating the integration of MOSAIX with pre-existing systems in the LHC. Two slow control paths are implemented, separating the functions of chip control and power management.

This contribution highlights the lessons learnt from the predecessors MOSS and MOST chips, summarizing the architectural decisions of the MOSAIX implementation and focusing on the adopted yield enhancement techniques.