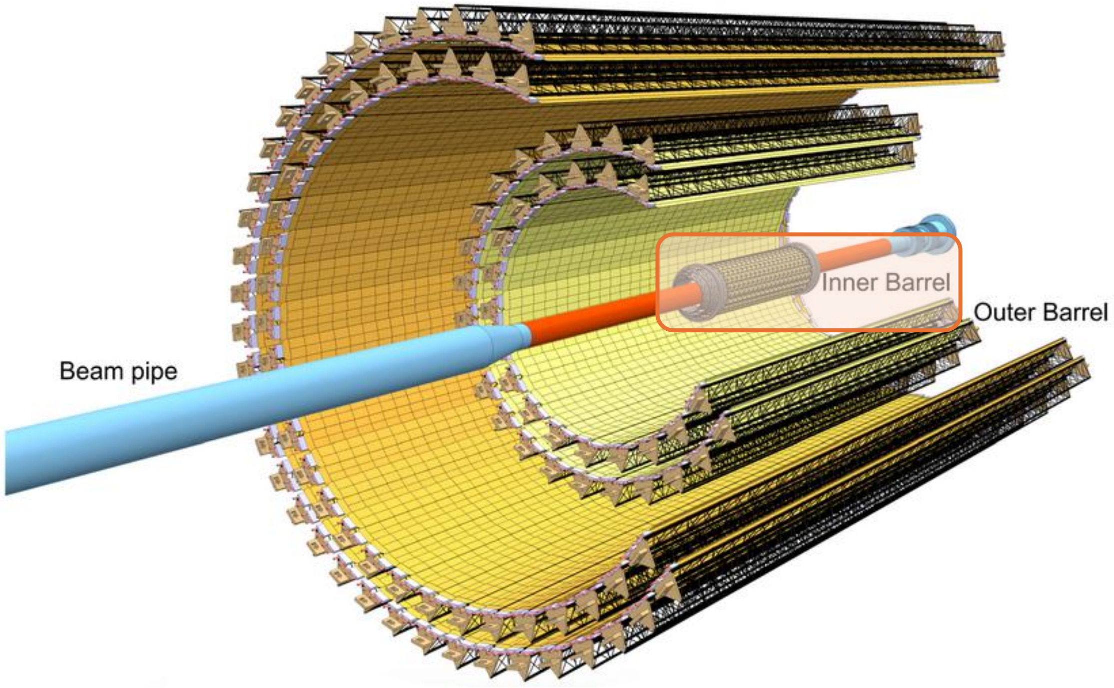
Development of the MOSAIX chip for the ALICE ITS3 upgrade

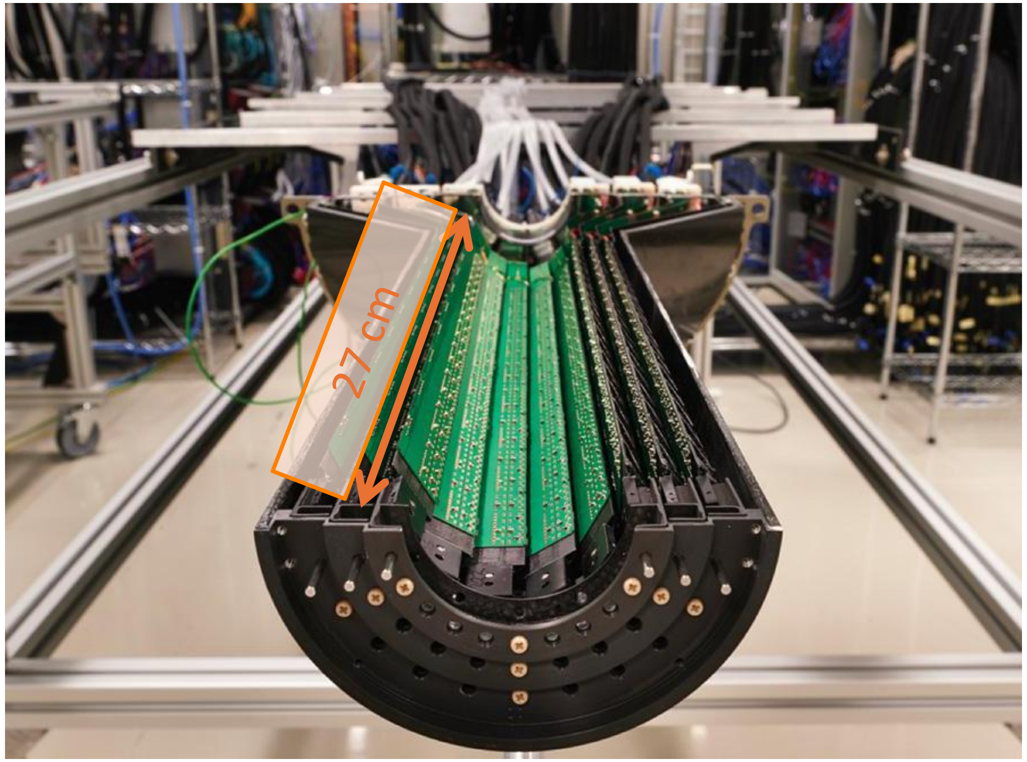
TWEPP, Glasgow, Scotland. October 2nd 2024

Pedro Vicente Leitao, CERN, Switzerland

On behalf of the MOSAIX design team and the ALICE collaboration

ALICE ITS

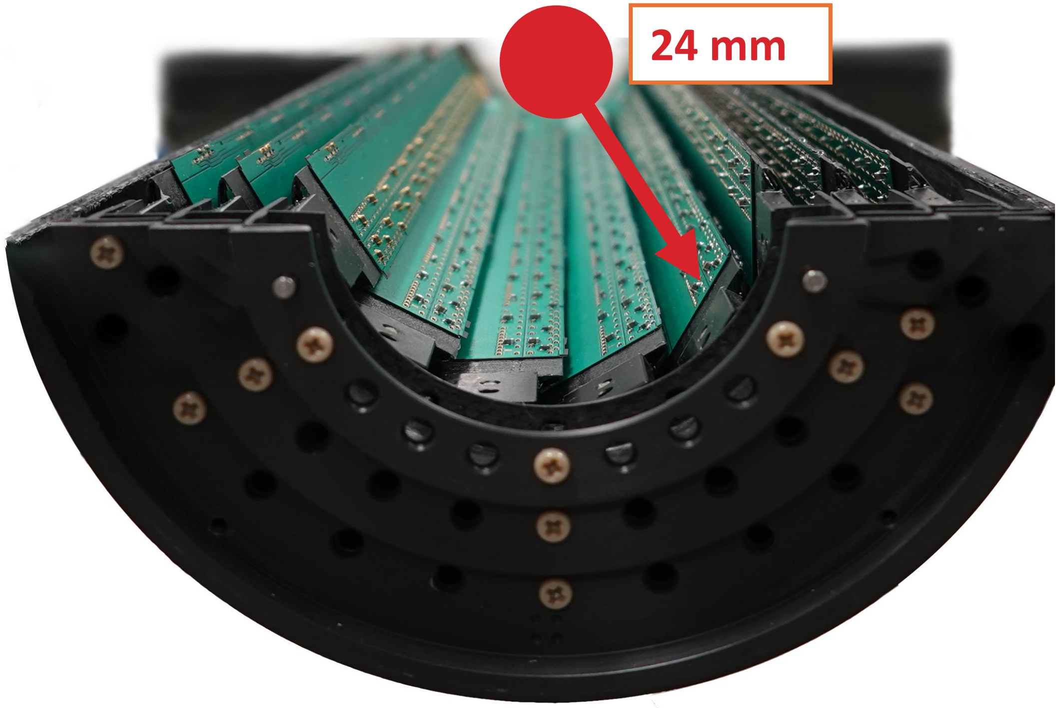




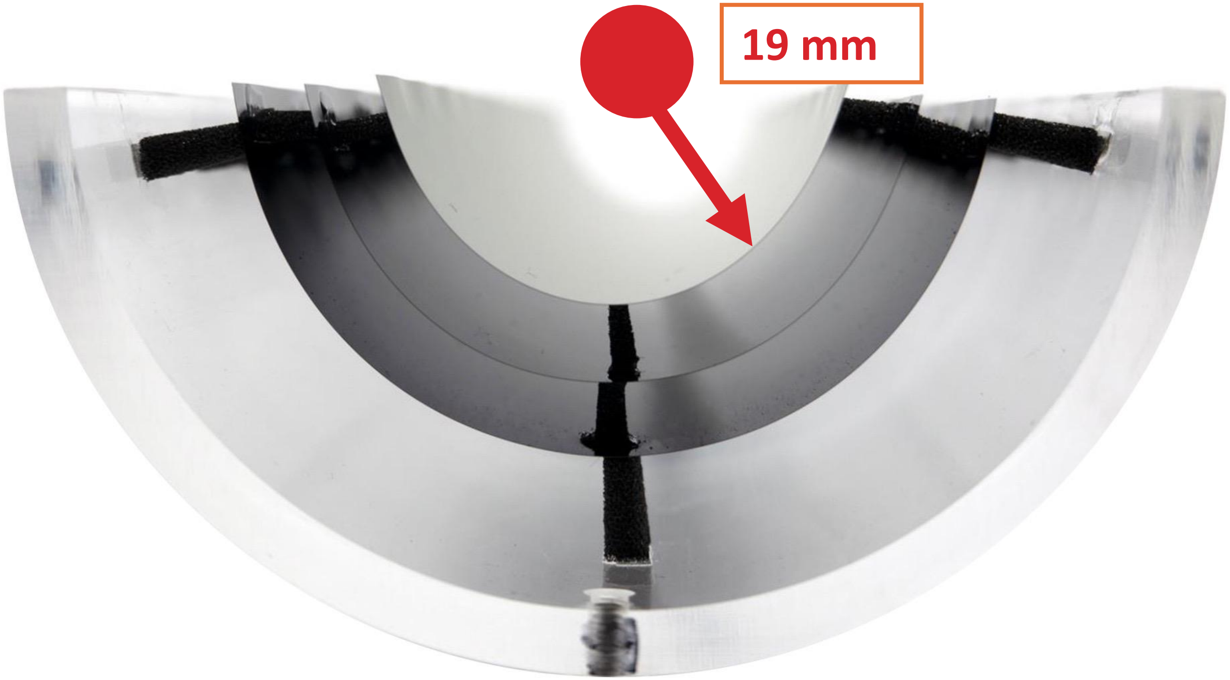
ALICE ITS2
half inner barrel

What can we do better?

Everything is on-chip: silicon-only pixel detector



24 mm from the beam pipe
0.35 % X_0 per layer

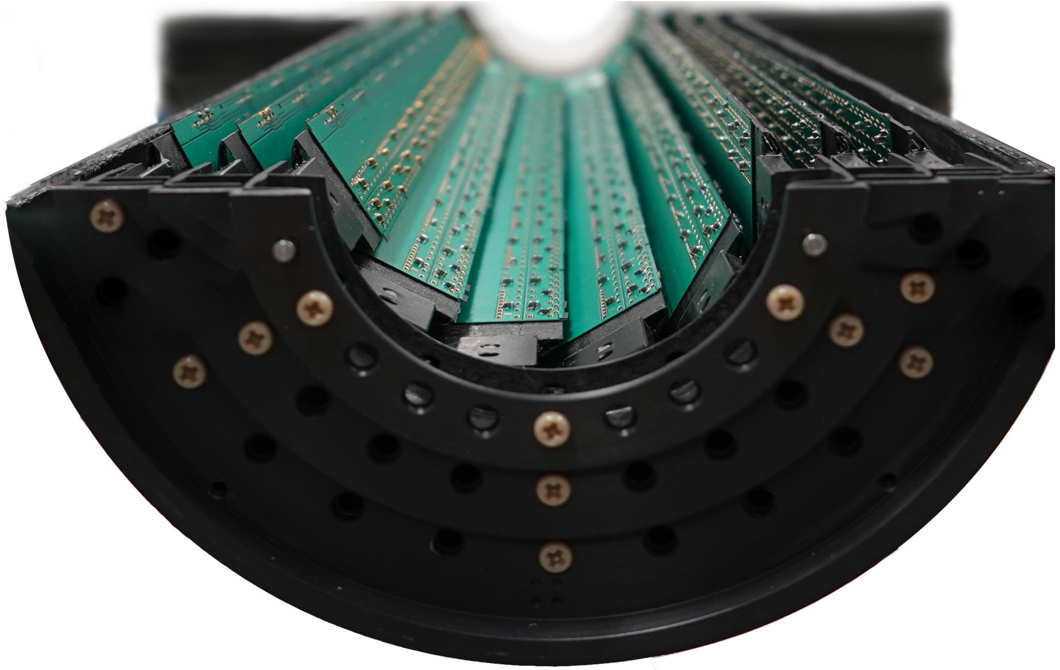


19 mm from the beam pipe
0.07 % X_0 per layer

What are the challenges?

Everything is on-chip

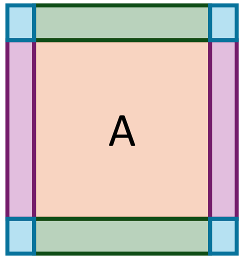
- Power distribution on-chip
- Data communication on-chip
- No active cooling
- Manufacturing defects



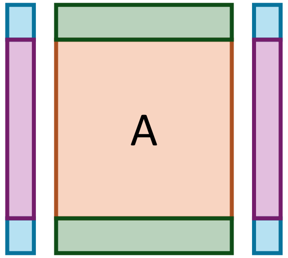
Design a large area silicon-only bent pixel detector

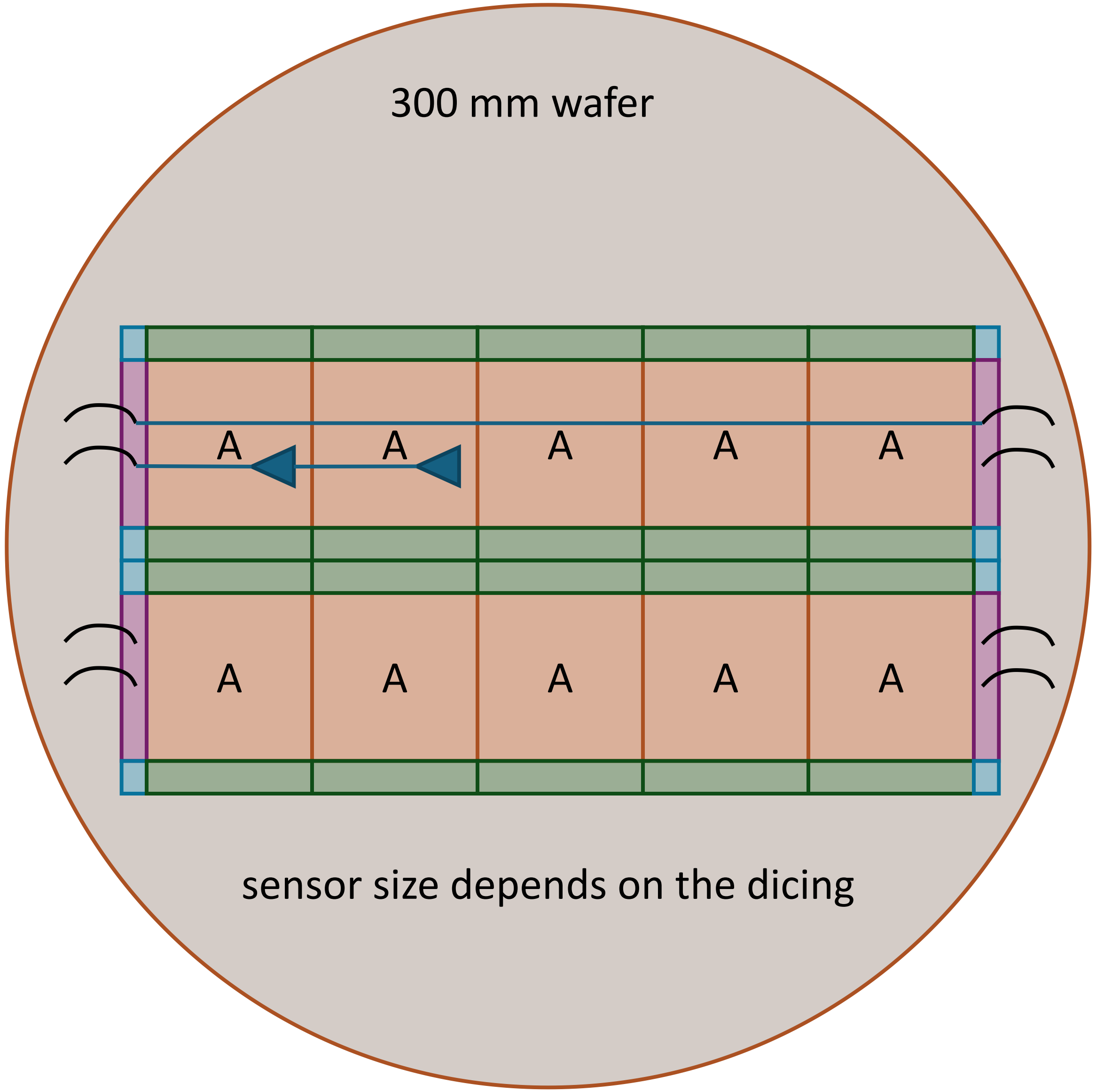
How to design a wafer scale bent pixel detector?

Max reticle size



split design



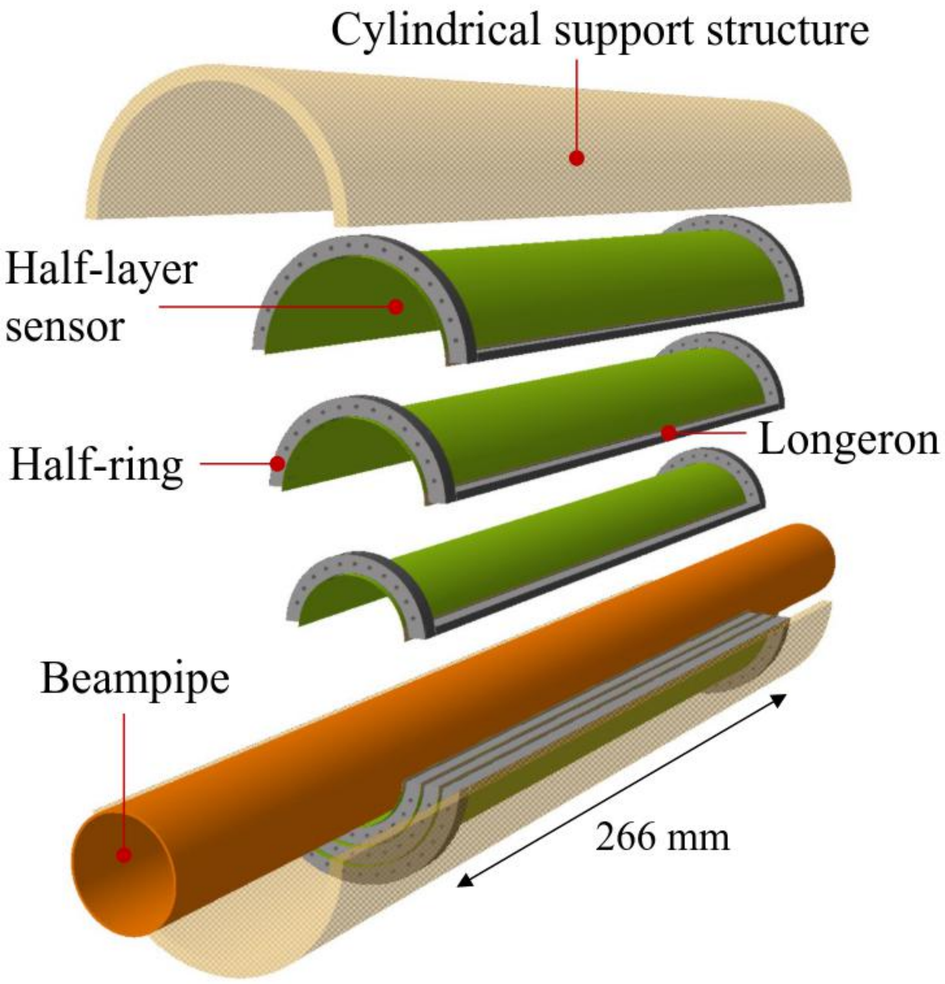

300 mm wafer

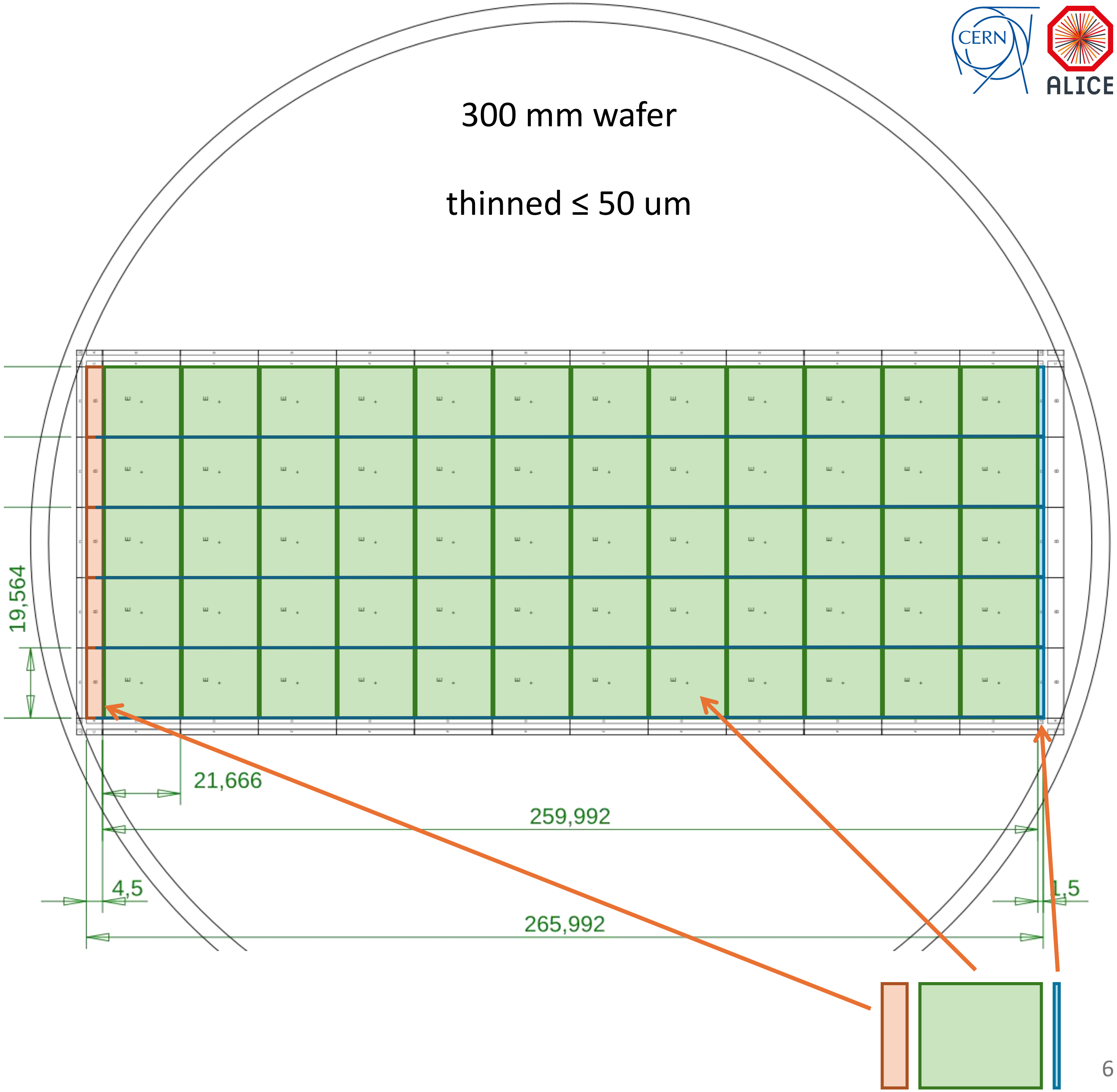
sensor size depends on the dicing

Only possible if the technology allows stitching

A = sensitive area

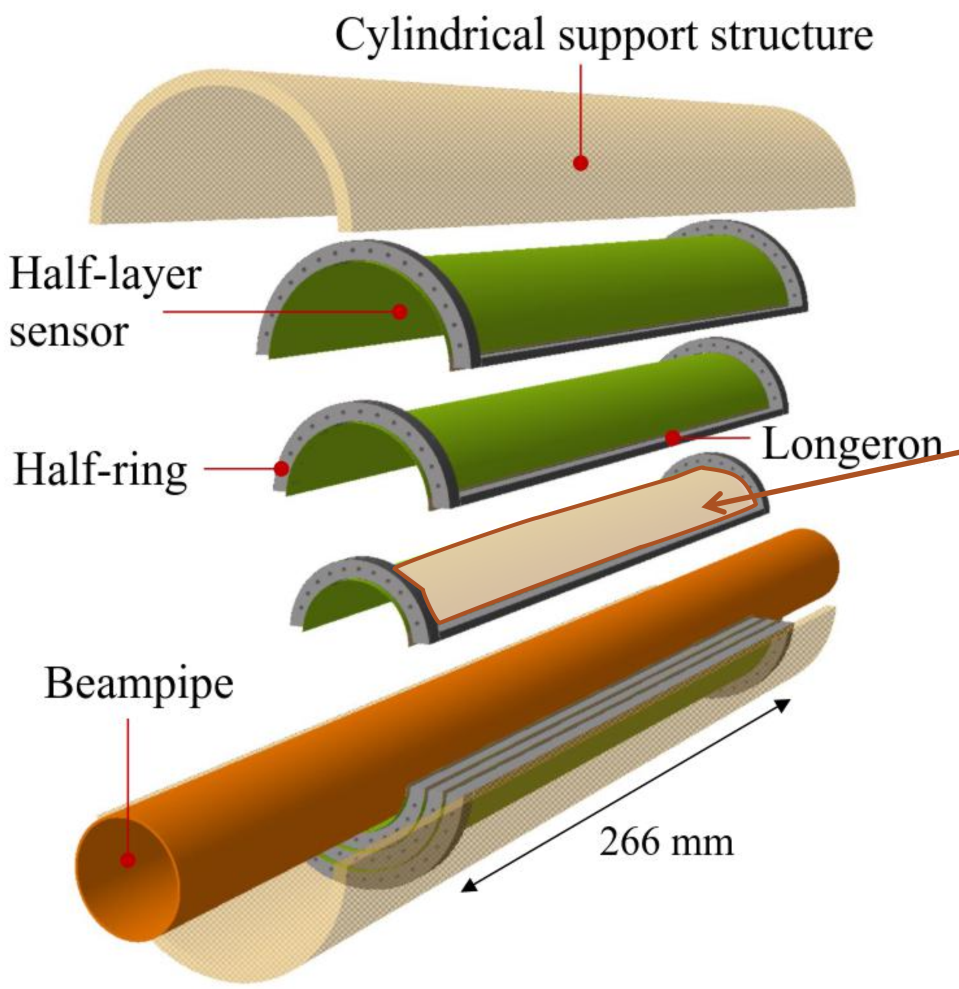
ITS3 detector

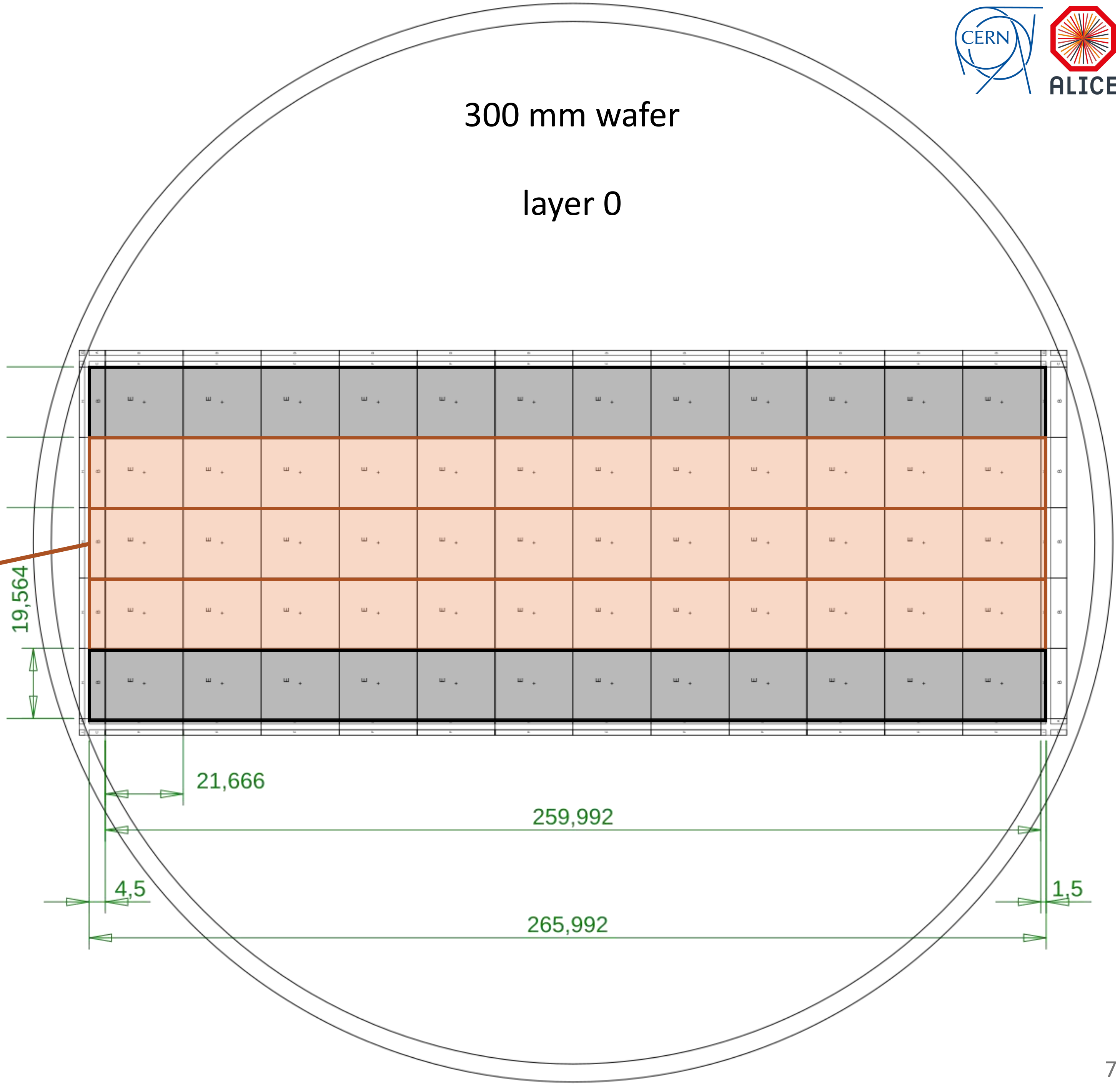



300 mm wafer

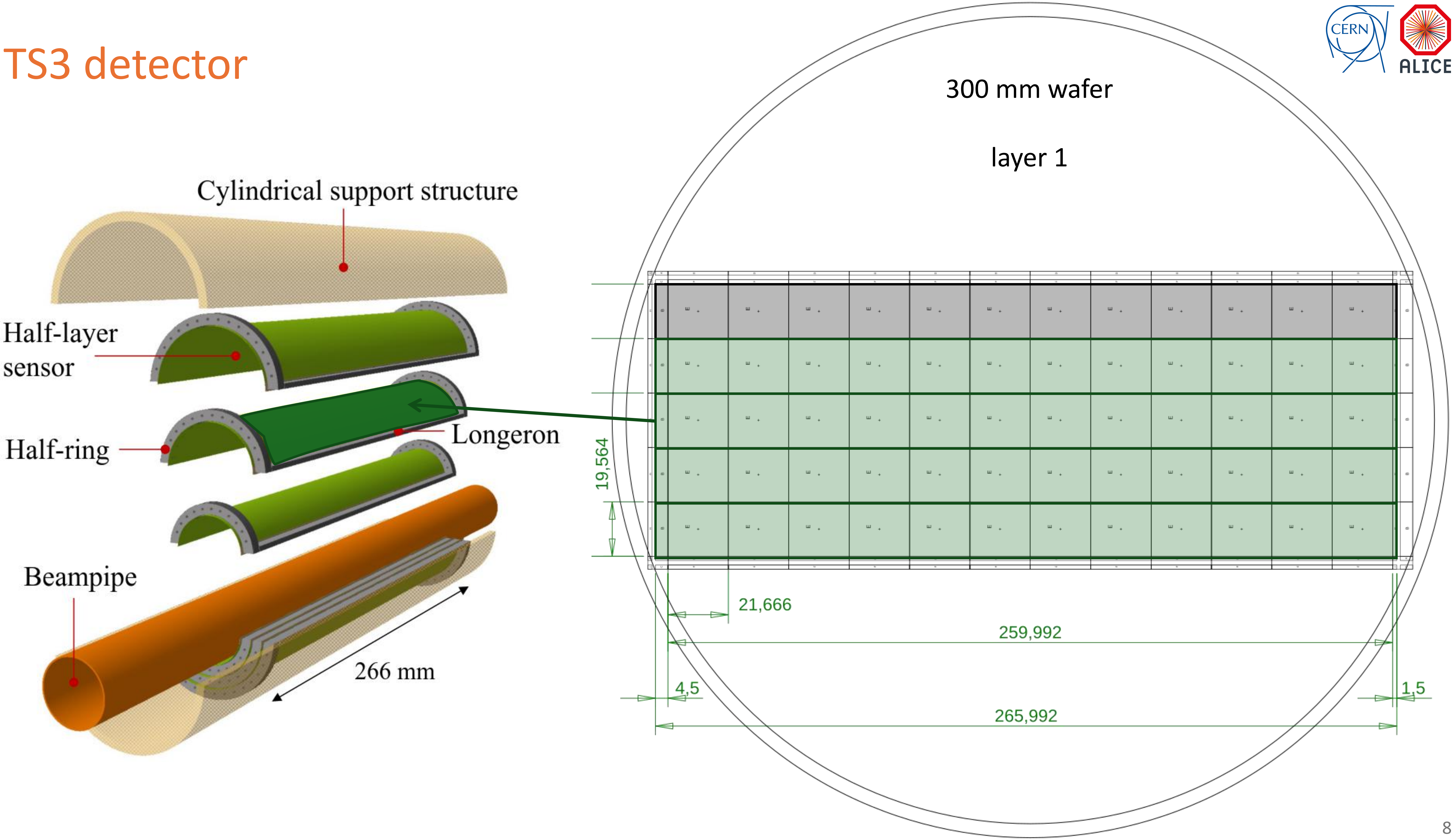
thinned ≤ 50 um

ITS3 detector

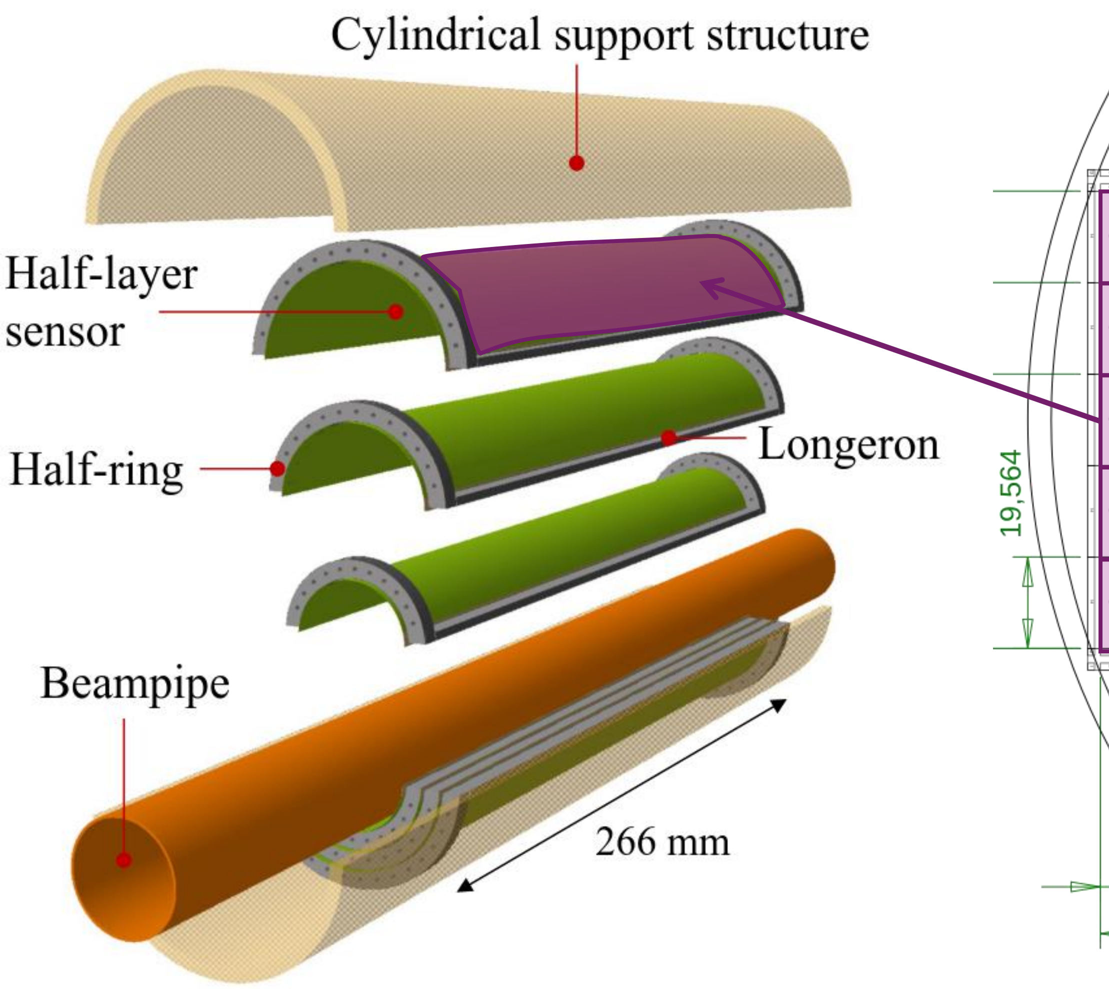


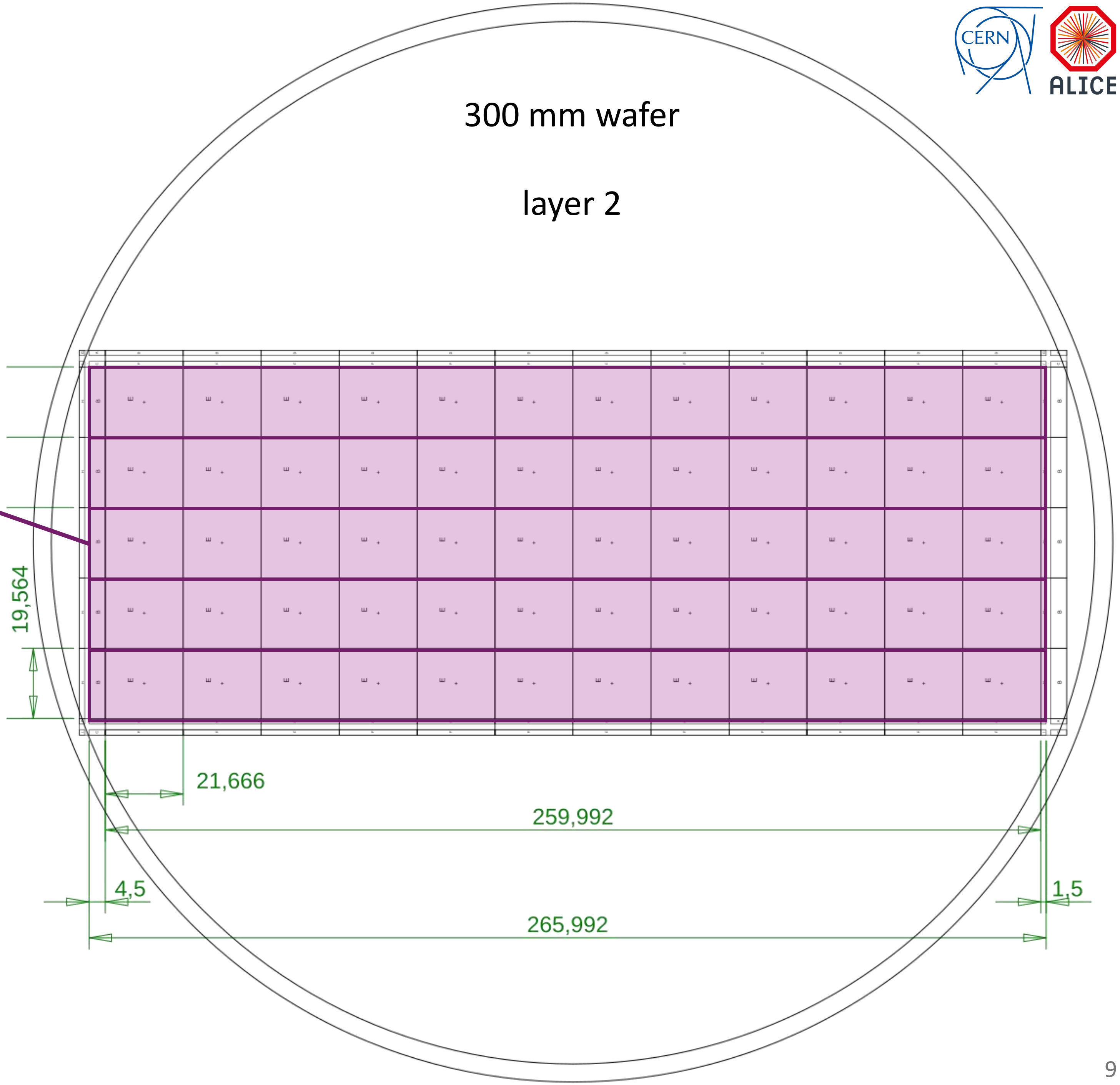


ITS3 detector

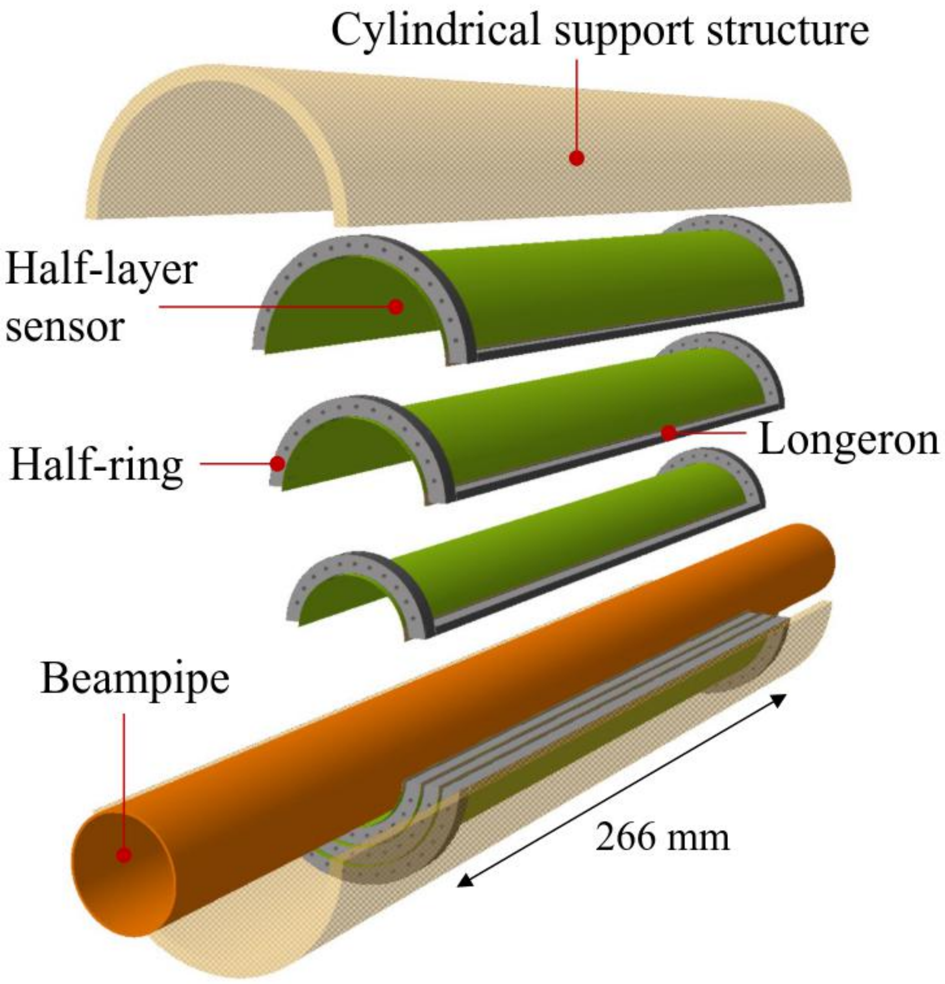


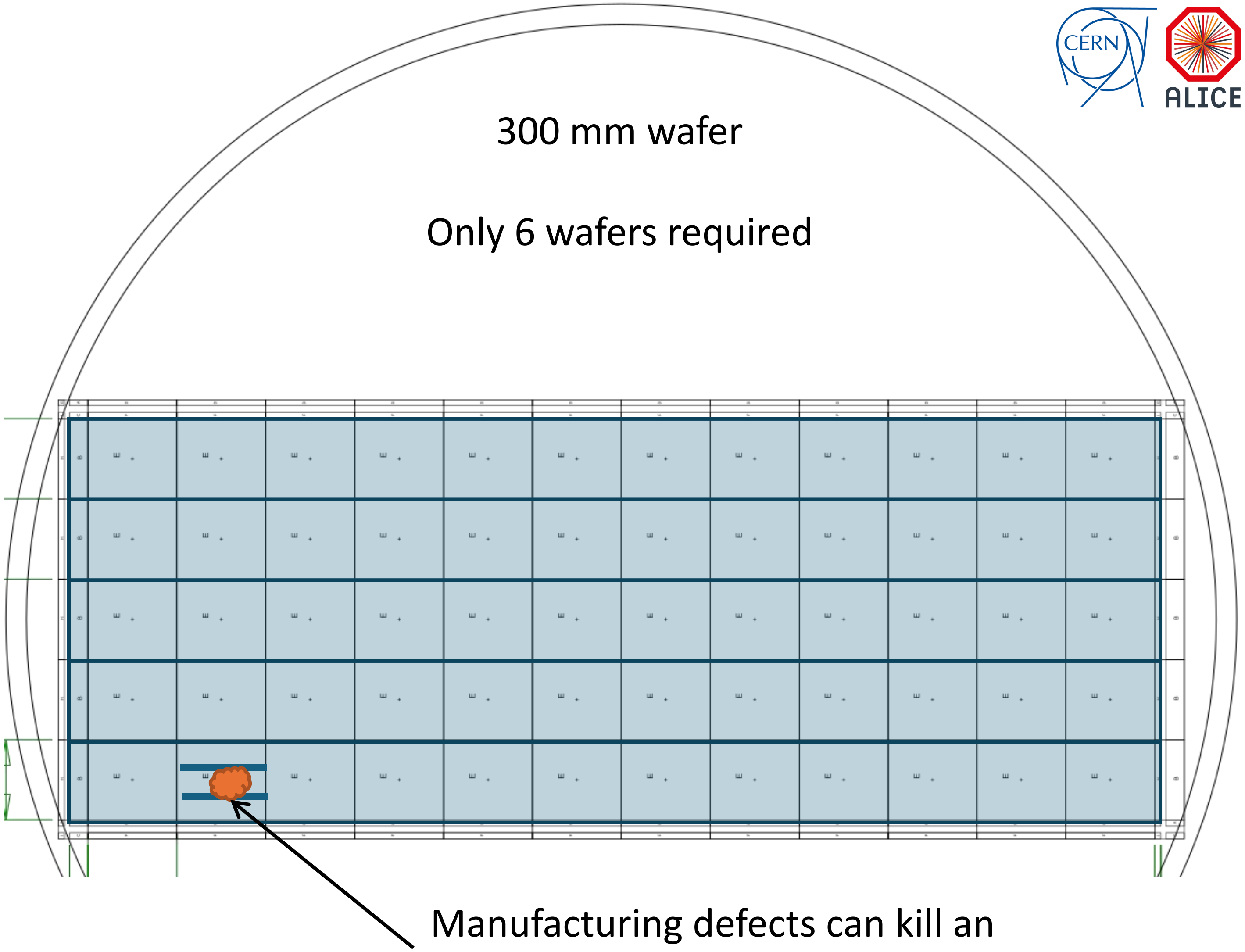
ITS3 detector





ITS3 detector





300 mm wafer

Only 6 wafers required

Manufacturing defects can kill an entire sensor

high yield is required

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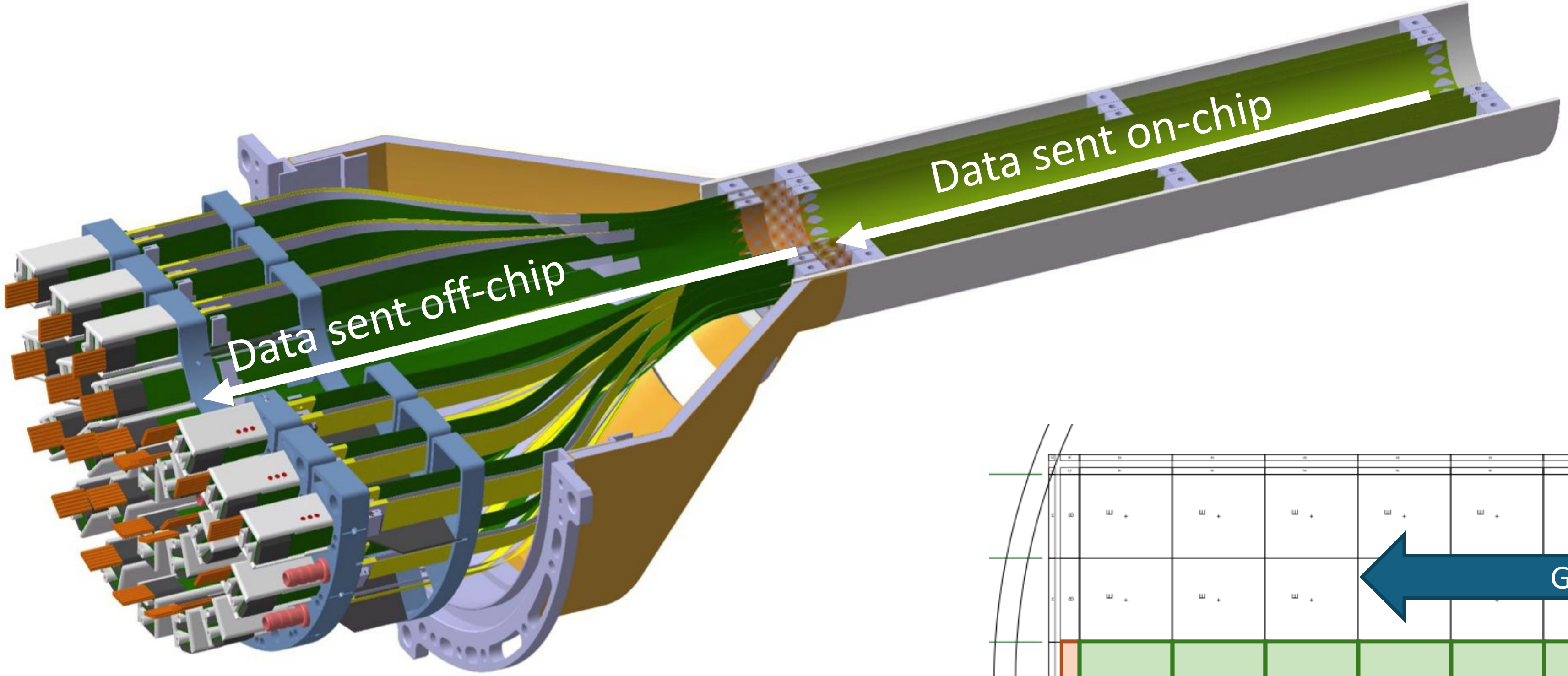
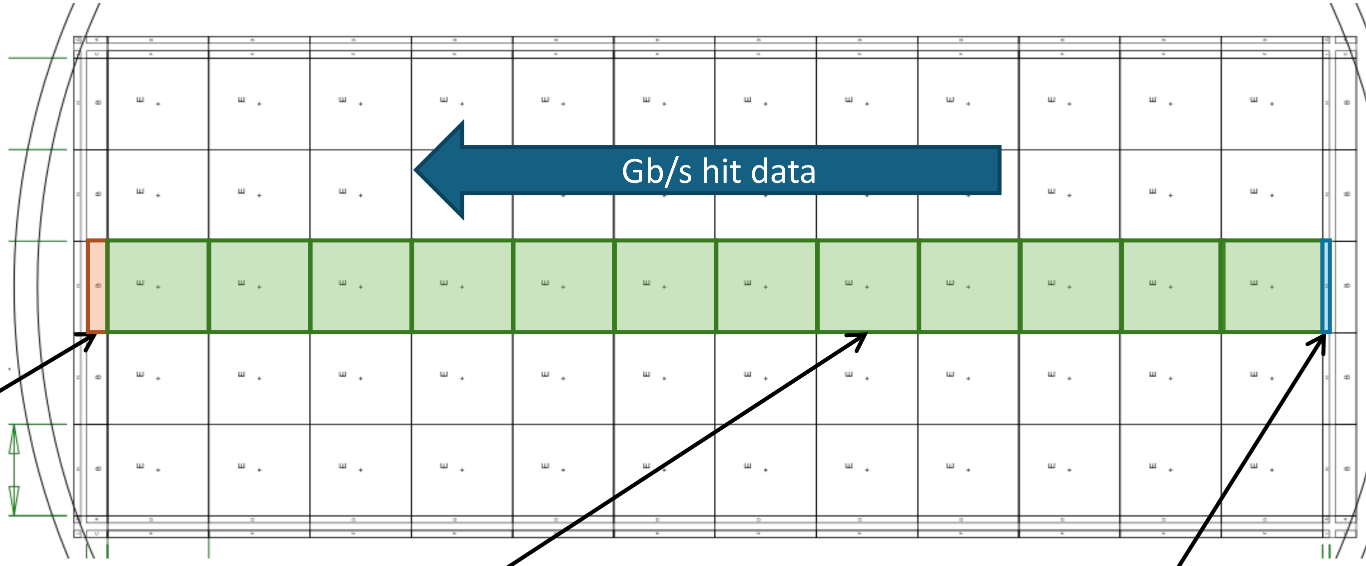
* see Gregor Eberwein's talk on how interesting these type of faults can be

ITS3 detector



4.4 MHz/cm² particle rate

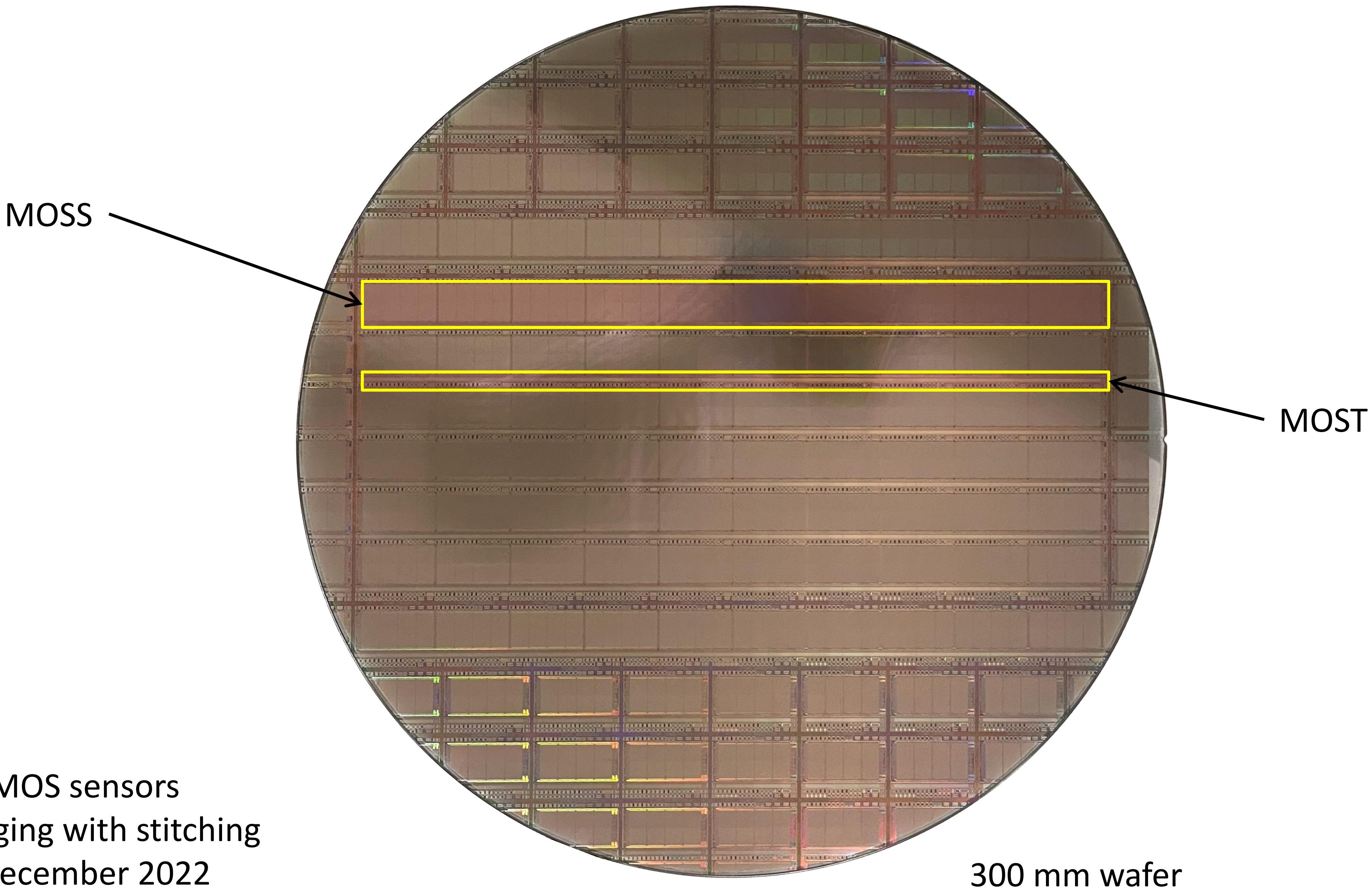


power pads
I/O pads
Gb/s offchip transmitters

sensitive area
readout circuitry

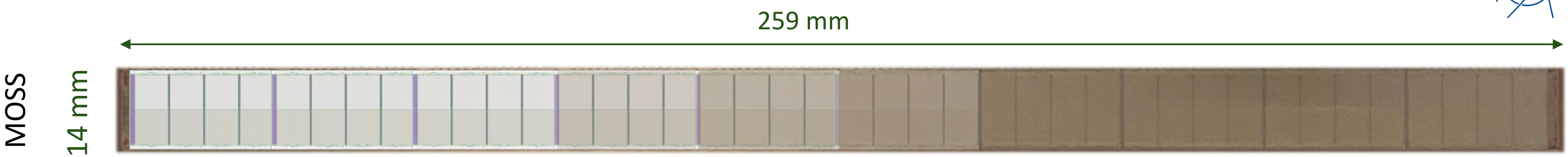
power pads

Wafer scale stitched pixel sensor prototypes



300 mm wafer

ER1 wafer
Monolithic CMOS sensors
TPSCo65 imaging with stitching
Submission December 2022



Study yield and uniformity of large sensing areas
Characterization of pixel frontends

Enlarged spacing design
Coarse power modularity

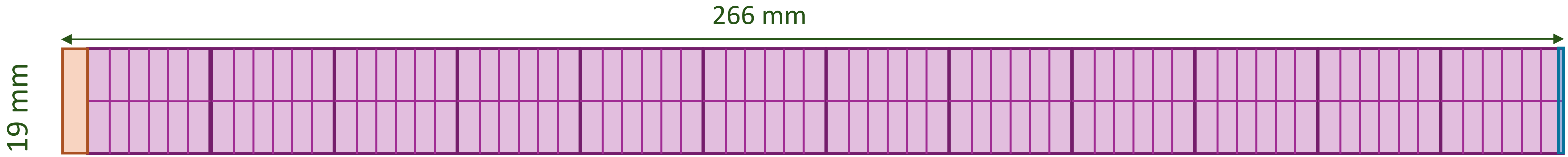
Two different goals

Two different approaches regarding defects

Study detach of pixel groups from the global power grid via switches
Gb/s on-chip data transmission

Minimum spacing design
Fine power modularity

MOSAIX is the full size, fully functional, stitched sensor prototype for the ITS3



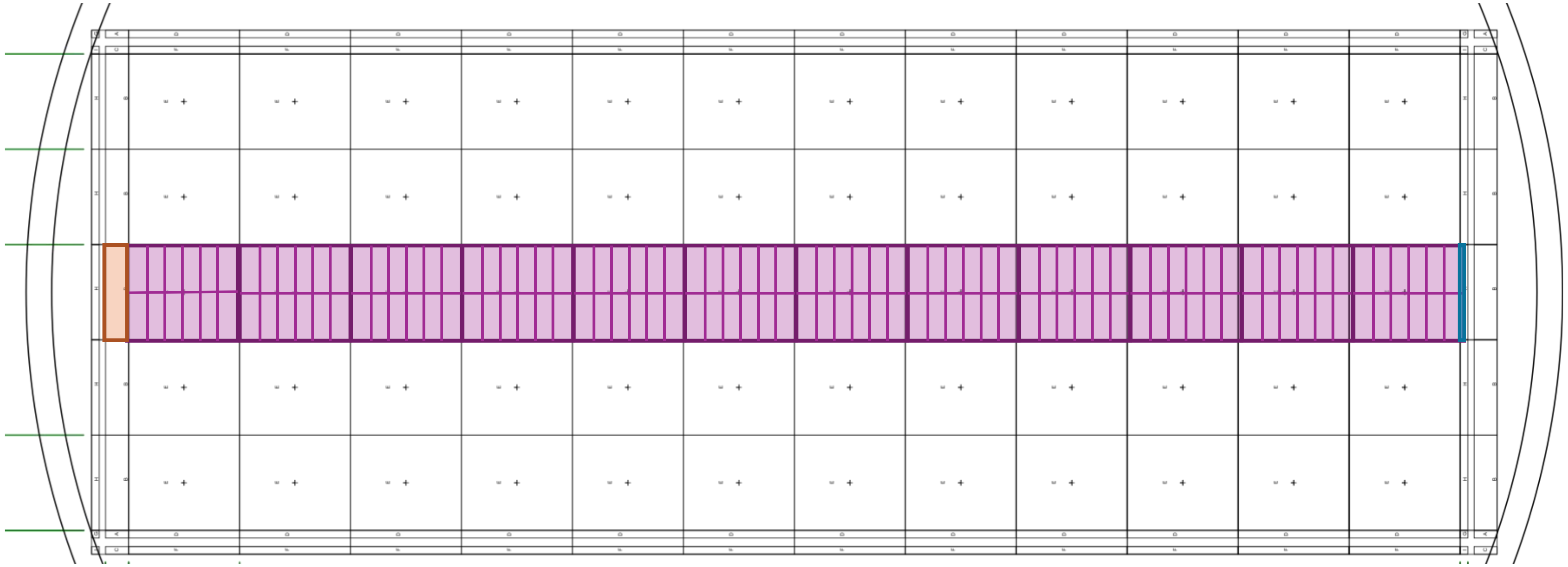
93 % sensitive region
0.7 % sensor area modularity
144 tiles (independent units)

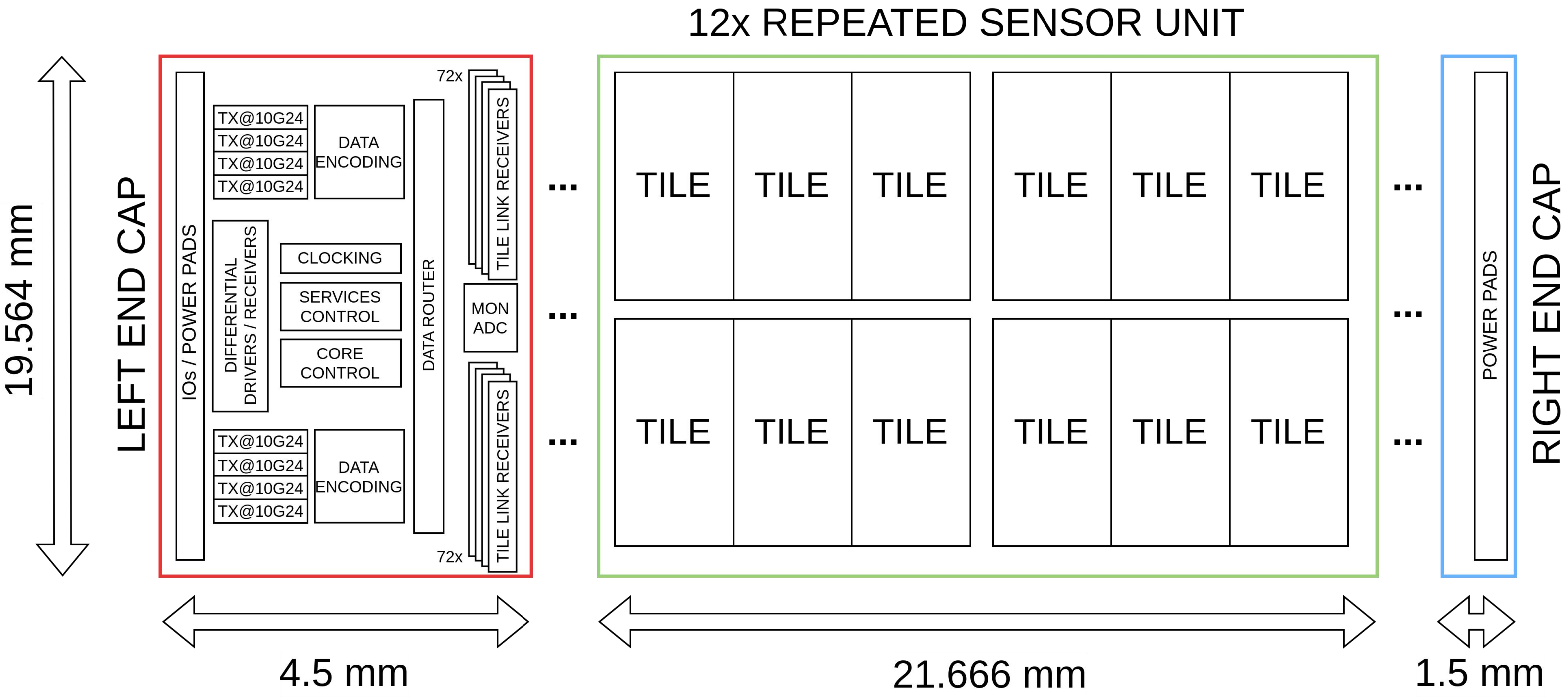
10^{13} NIEL (1 MeV neq cm^{-2})
10 kGray TID
Triple modular redundancy

4.4 MHz/cm^2 particle rate
30.72 Gb/s off-chip data transmission
minimum 2 µs integration time
< 40 mW/cm^2

20.8 x 22.8 μm^2 pixel size
Detection Efficiency > 99 %
Fakehit rate < 0.1 $pixel^{-1}s^{-1}$

MOSAIX





12x REPEATED SENSOR UNIT

19.564 mm

LEFT END CAP

IOs / POWER PADS

TX@10G24
TX@10G24
TX@10G24
TX@10G24

DATA ENCODING

DIFFERENTIAL DRIVERS / RECEIVERS

CLOCKING

SERVICES CONTROL

CORE CONTROL

TX@10G24
TX@10G24
TX@10G24
TX@10G24

DATA ENCODING

DATA ROUTER

72x

TILE LINK RECEIVERS

MON ADC

TILE LINK RECEIVERS

72x

TILE TILE TILE TILE TILE TILE

TILE TILE TILE TILE TILE TILE

POWER PADS

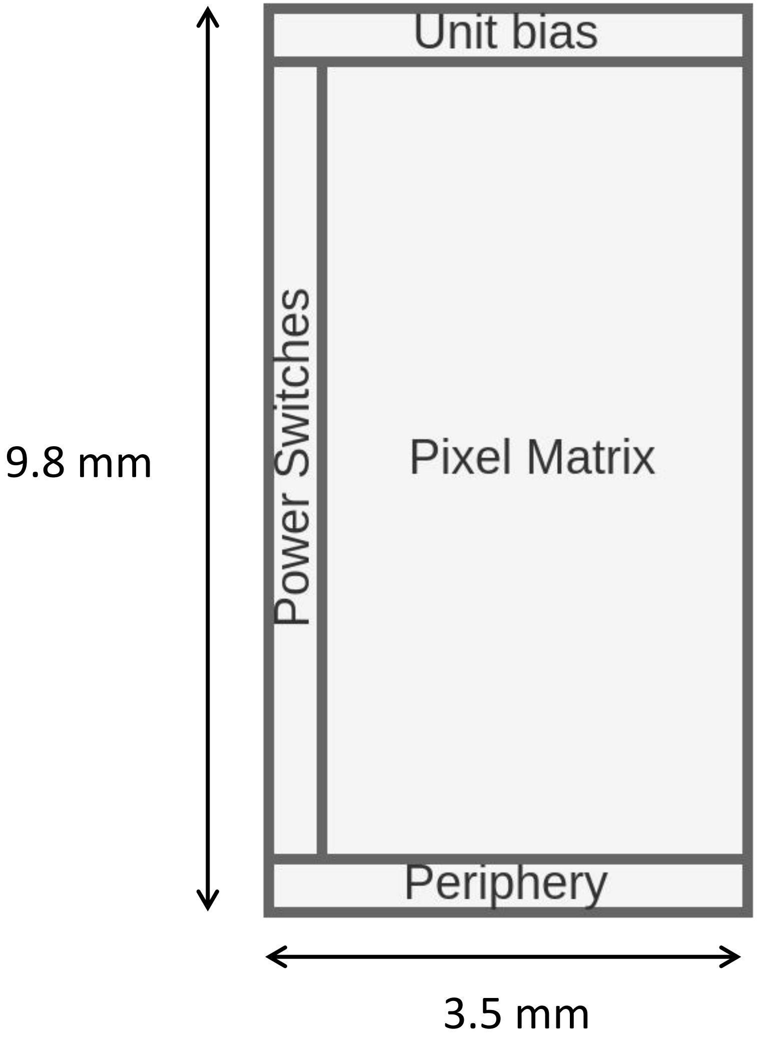
RIGHT END CAP

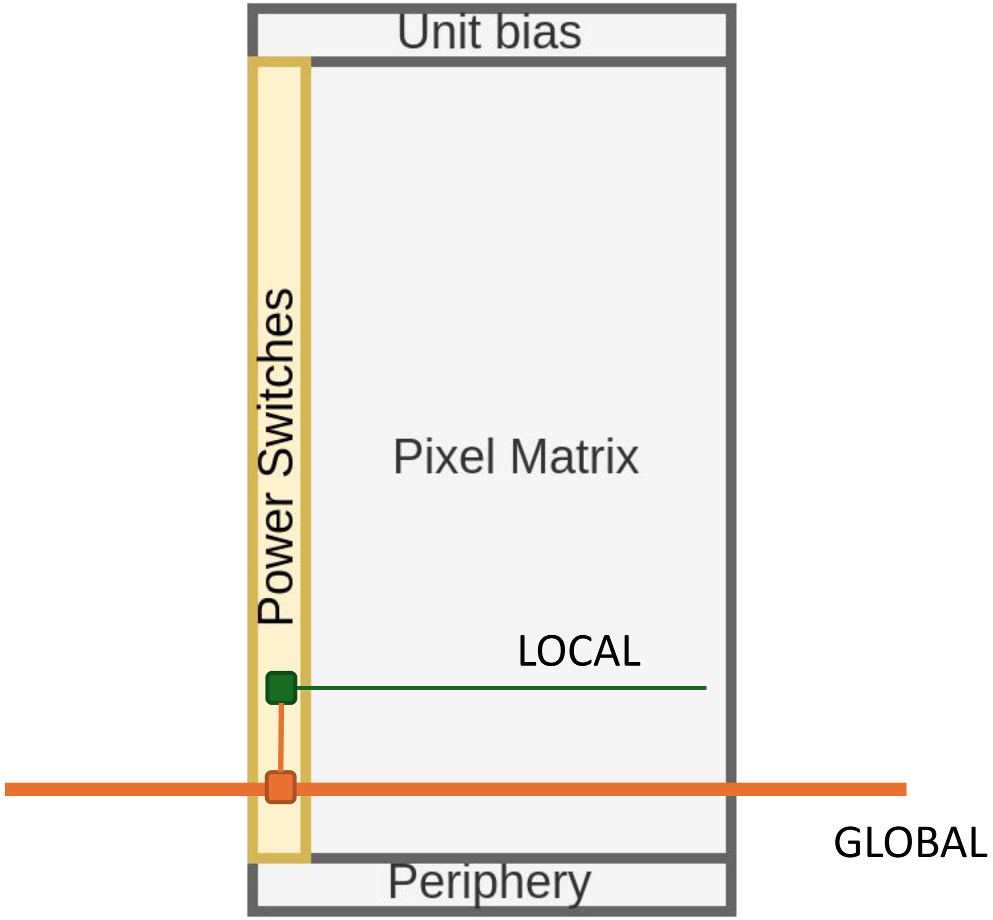
4.5 mm

21.666 mm

1.5 mm

Tile = independent sensor unit



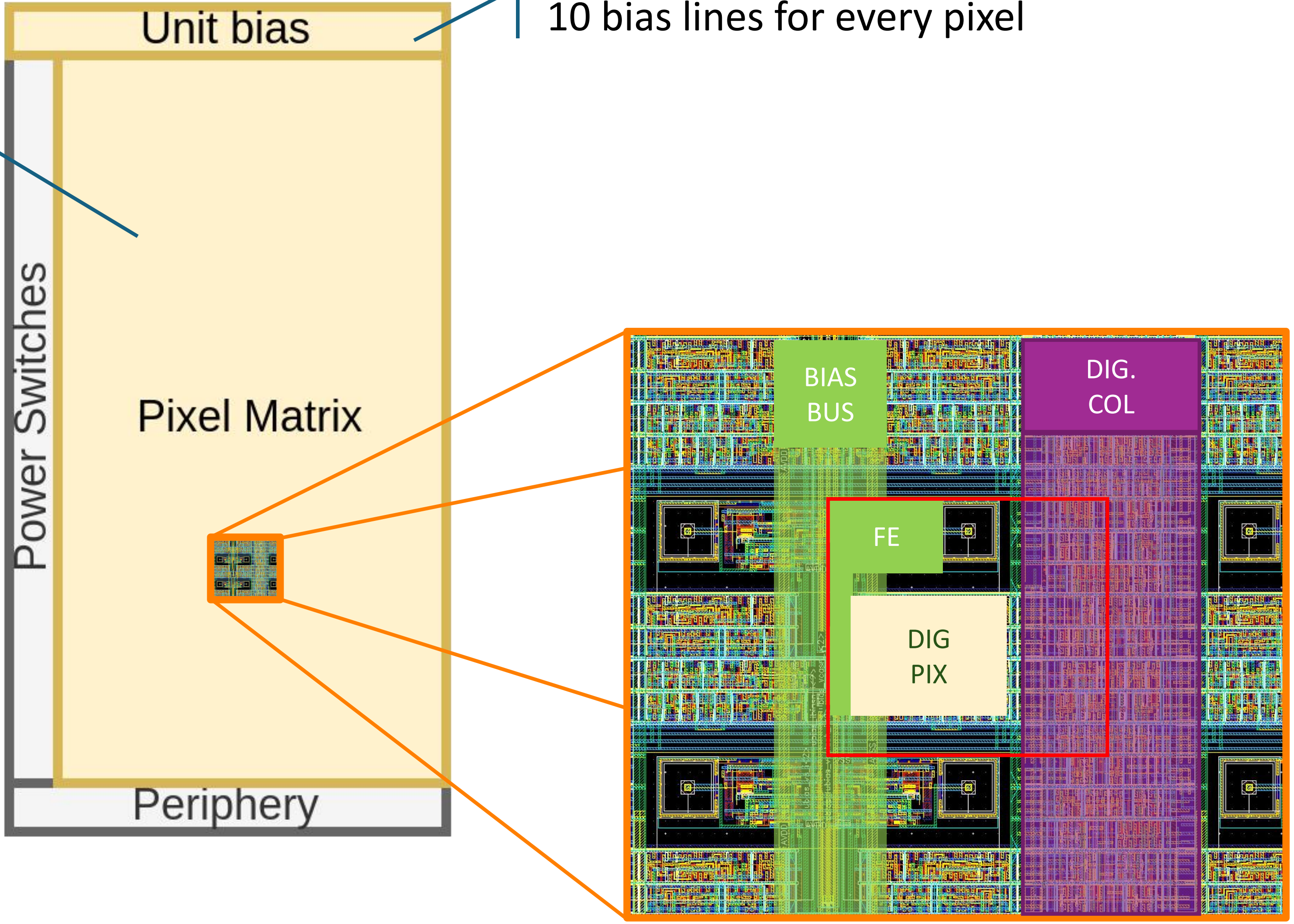


power switches allow to connect the tile to the global power domain

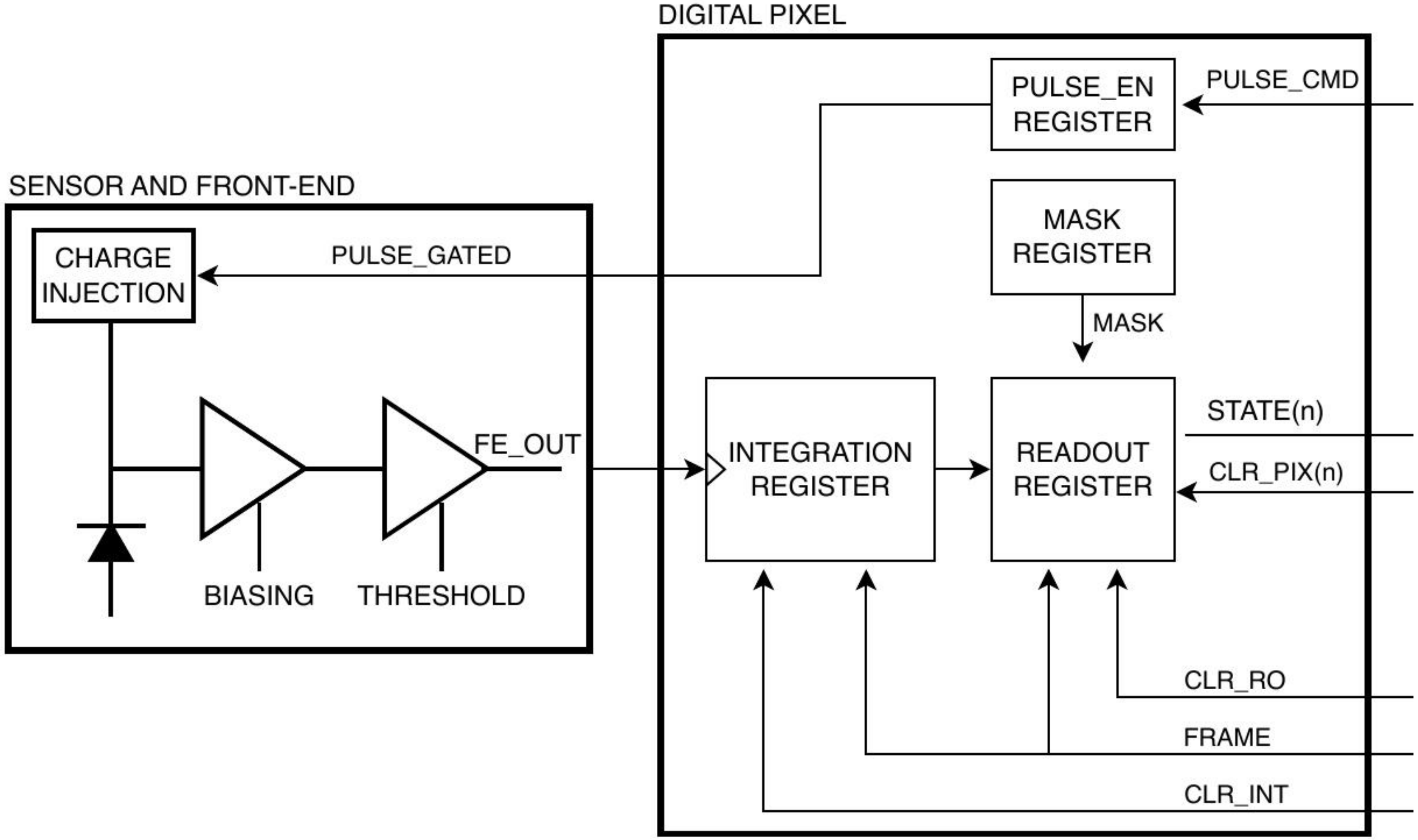
* see Szymon Bugiel's talk on how to reliably distribute power in the MOSAIX chip

6 DACs
10 bias lines for every pixel

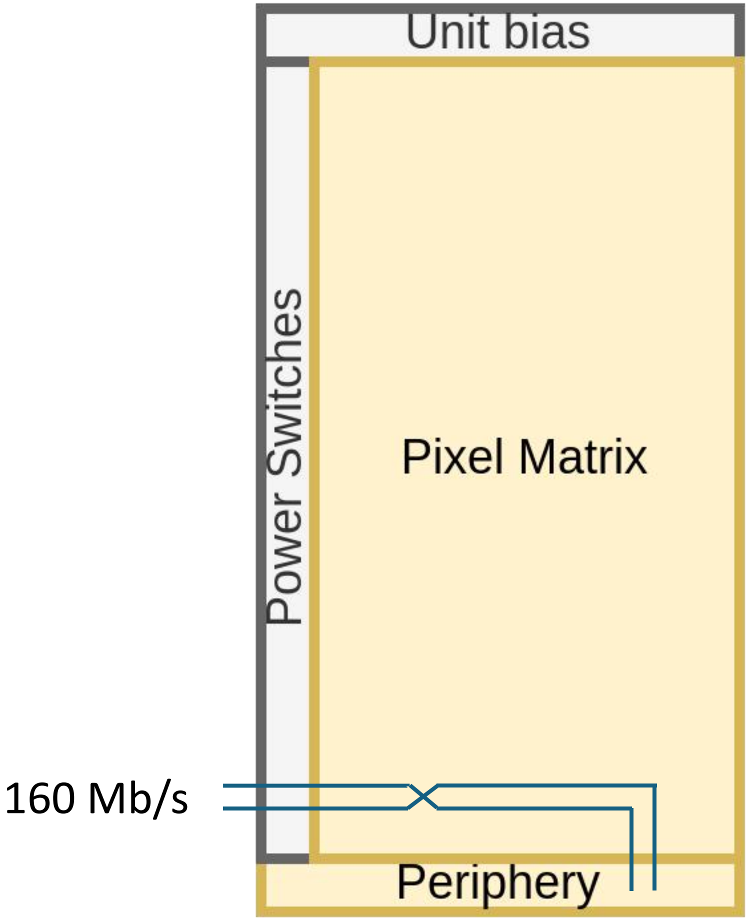
444 rows, 156 columns
double column readout
69.2k pixels / tile

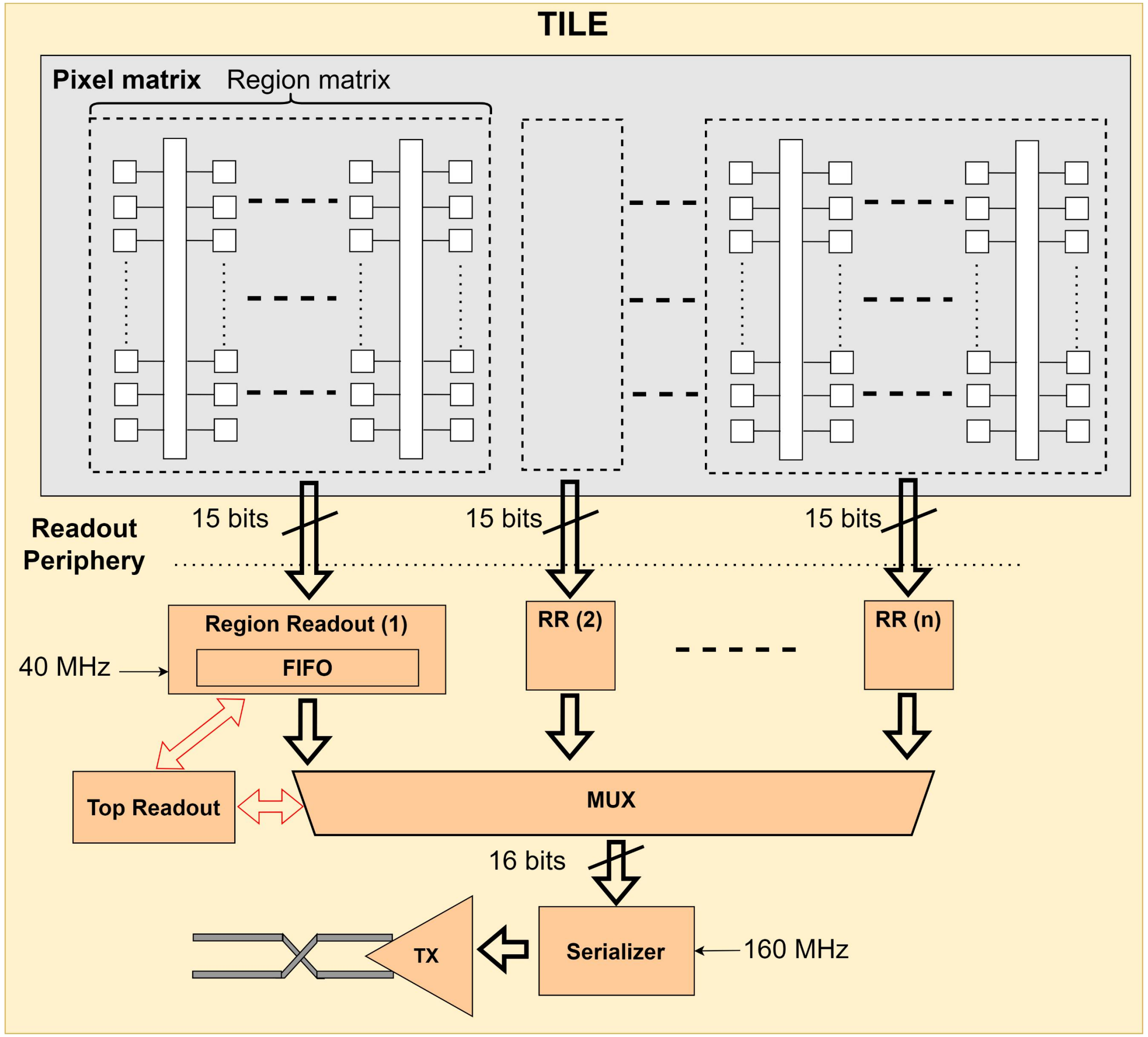


20.8 µm (r-phi) by 22.8 µm (z-axis)

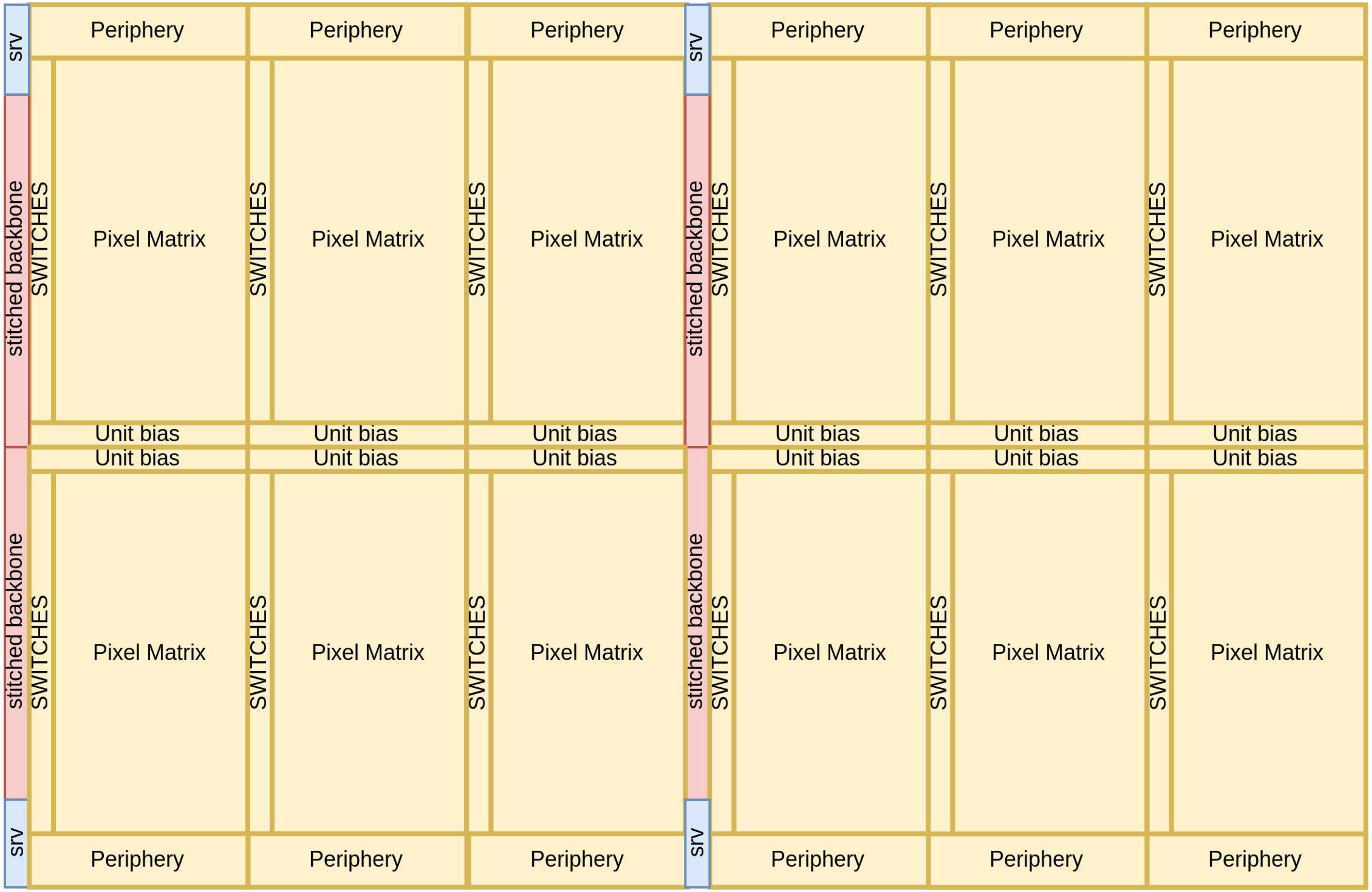


* see Simone Emiliani’s presentation on how non-idealities in testing circuitry affects the sensor performance


Unit bias
Power Switches
Pixel Matrix
160 Mb/s
Periphery


TILE
Pixel matrix
Region matrix
Readout Periphery
15 bits
15 bits
15 bits
Region Readout (1)
FIFO
40 MHz
RR (2)
RR (n)
Top Readout
MUX
16 bits
TX
Serializer
160 MHz

RSU



srv
Periphery
Periphery
Periphery
srv
Periphery
Periphery
Periphery

stitched backbone
SWITCHES
Pixel Matrix
SWITCHES
Pixel Matrix
SWITCHES
Pixel Matrix
stitched backbone
SWITCHES
Pixel Matrix
SWITCHES
Pixel Matrix
SWITCHES
Pixel Matrix

Unit bias
Unit bias
Unit bias
Unit bias
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Unit bias
Unit bias
Unit bias
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srv
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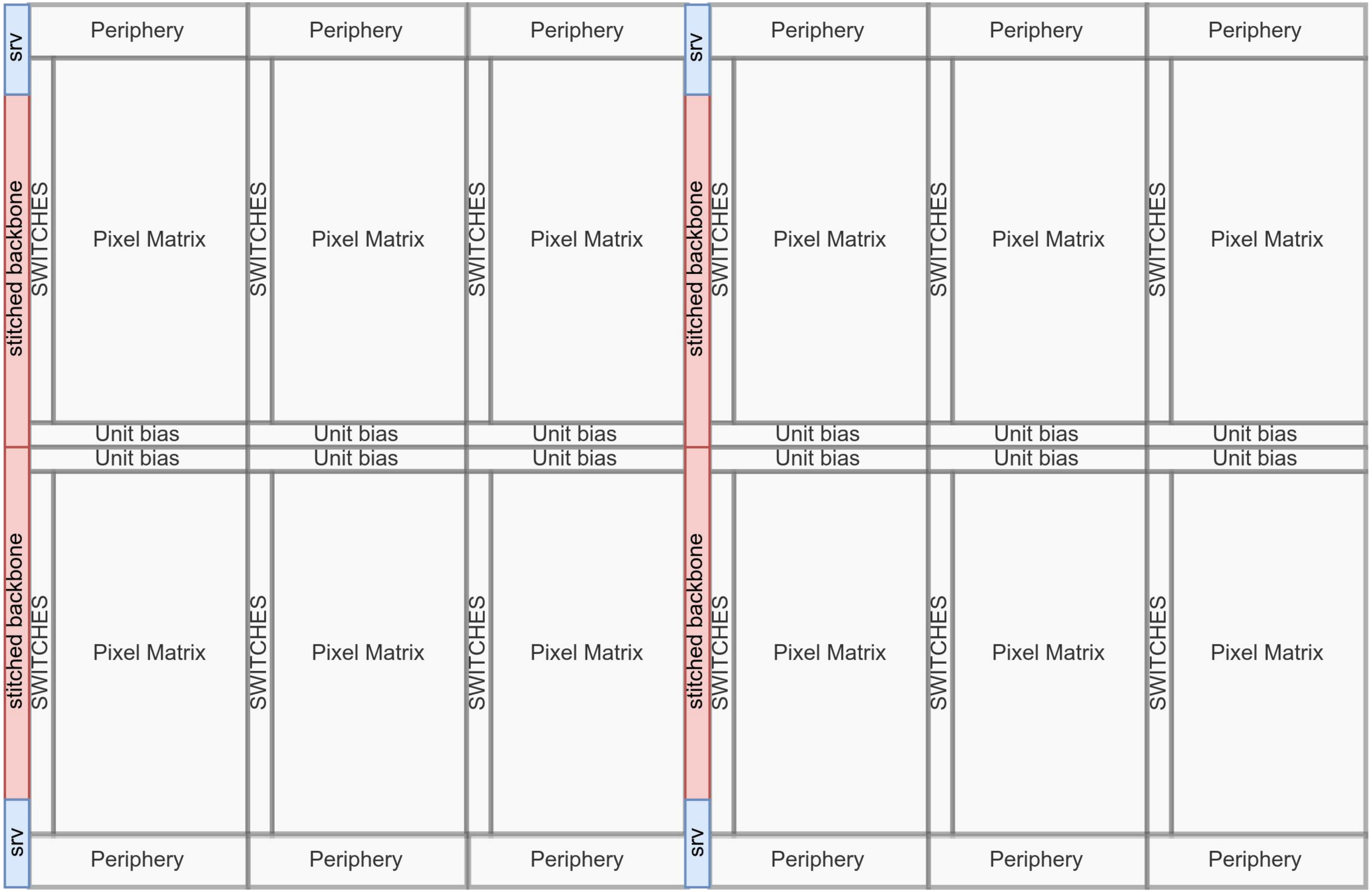

srv Periphery Periphery Periphery srv Periphery Periphery Periphery

stitched backbone SWITCHES Pixel Matrix SWITCHES Pixel Matrix SWITCHES Pixel Matrix stitched backbone SWITCHES Pixel Matrix SWITCHES Pixel Matrix SWITCHES Pixel Matrix

Unit bias Unit bias Unit bias Unit bias Unit bias Unit bias

Unit bias Unit bias Unit bias Unit bias Unit bias Unit bias

stitched backbone SWITCHES Pixel Matrix SWITCHES Pixel Matrix SWITCHES Pixel Matrix stitched backbone SWITCHES Pixel Matrix SWITCHES Pixel Matrix SWITCHES Pixel Matrix

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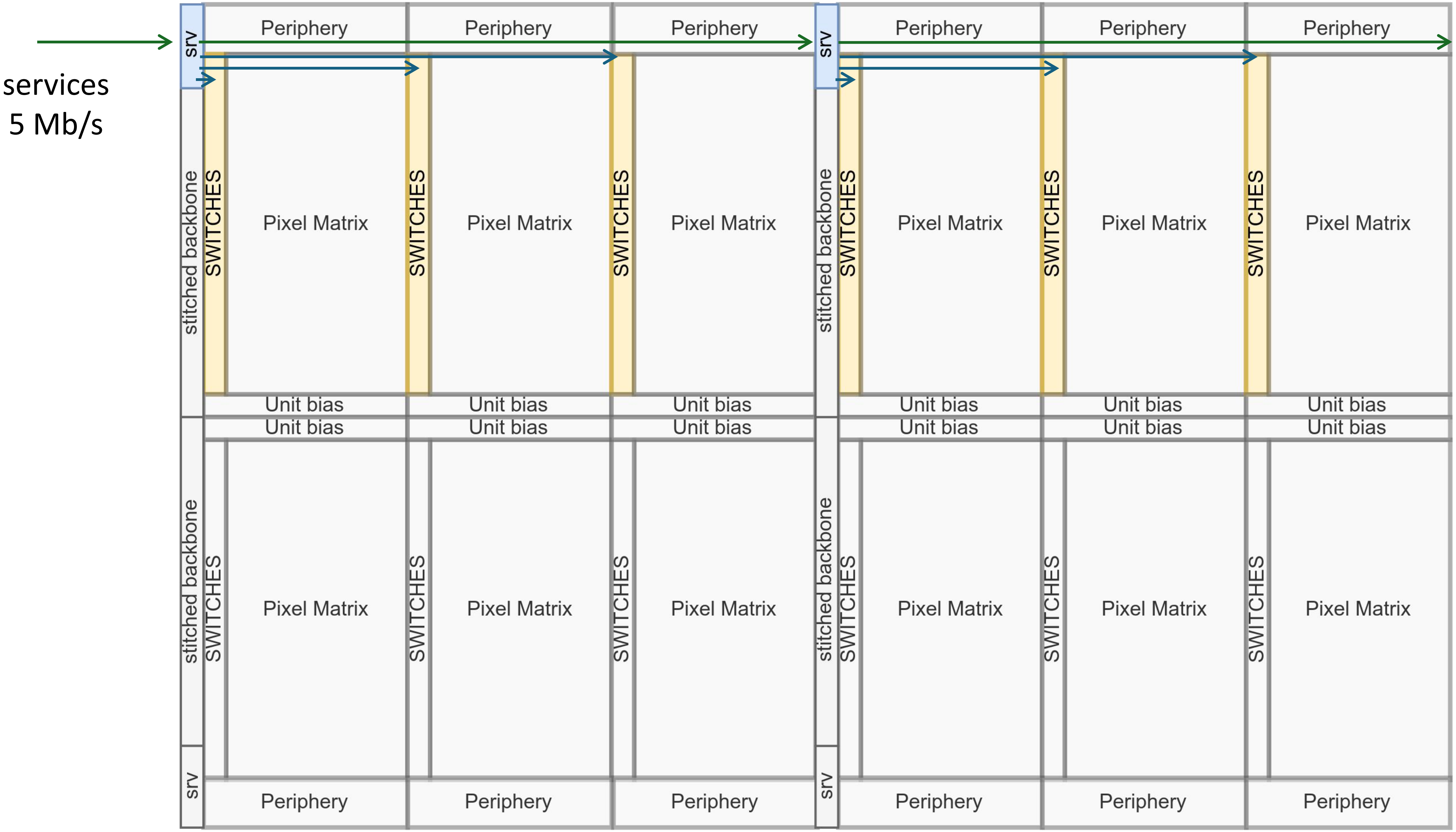


services
5 Mb/s

srv | Periphery | Periphery | Periphery | srv | Periphery | Periphery | Periphery

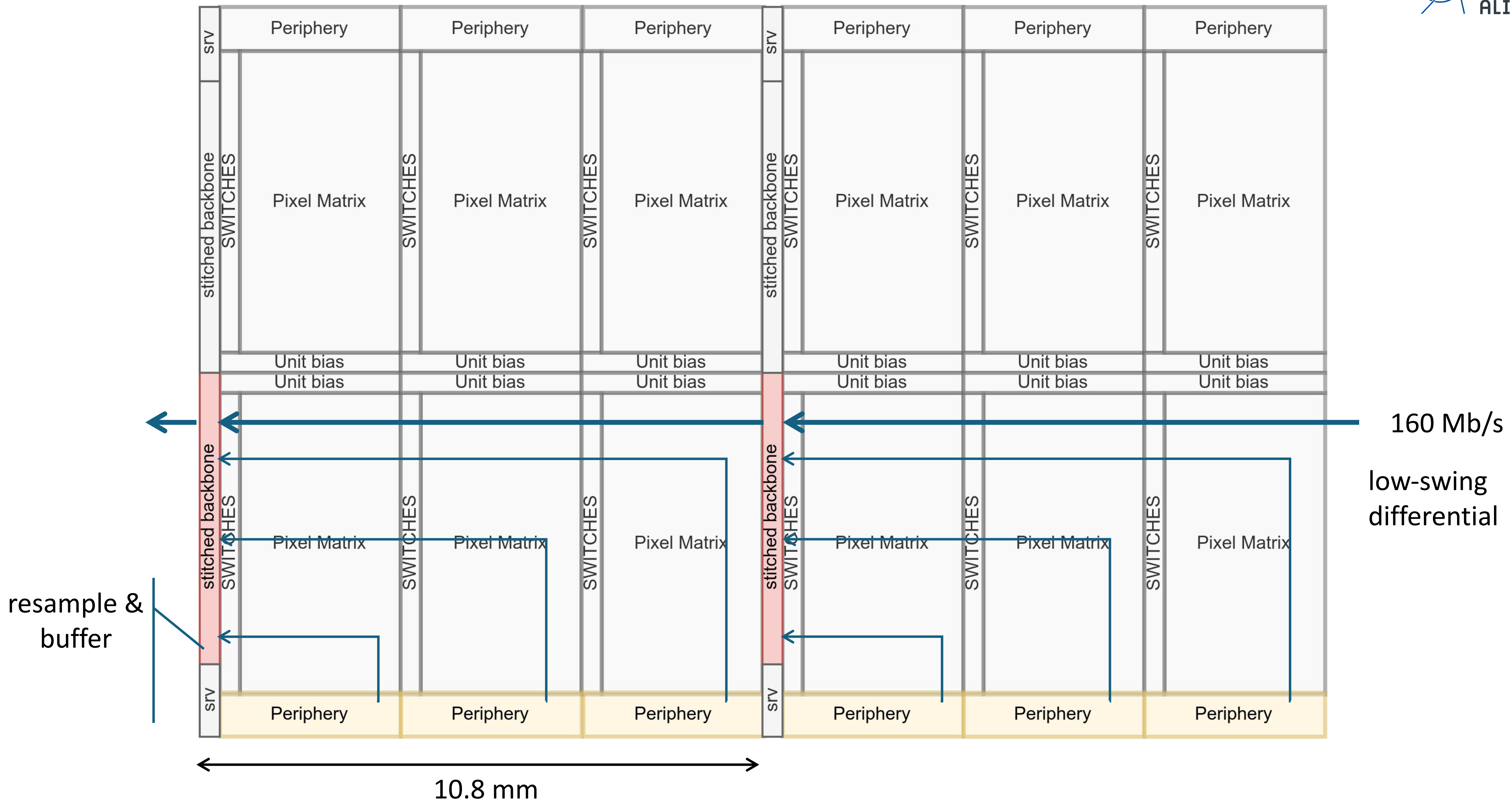
stitched backbone | SWITCHES | Pixel Matrix | SWITCHES | Pixel Matrix | SWITCHES | Pixel Matrix | stitched backbone | SWITCHES | Pixel Matrix | SWITCHES | Pixel Matrix | SWITCHES | Pixel Matrix

Unit bias | Unit bias | Unit bias | Unit bias | Unit bias | Unit bias

Unit bias | Unit bias | Unit bias | Unit bias | Unit bias | Unit bias

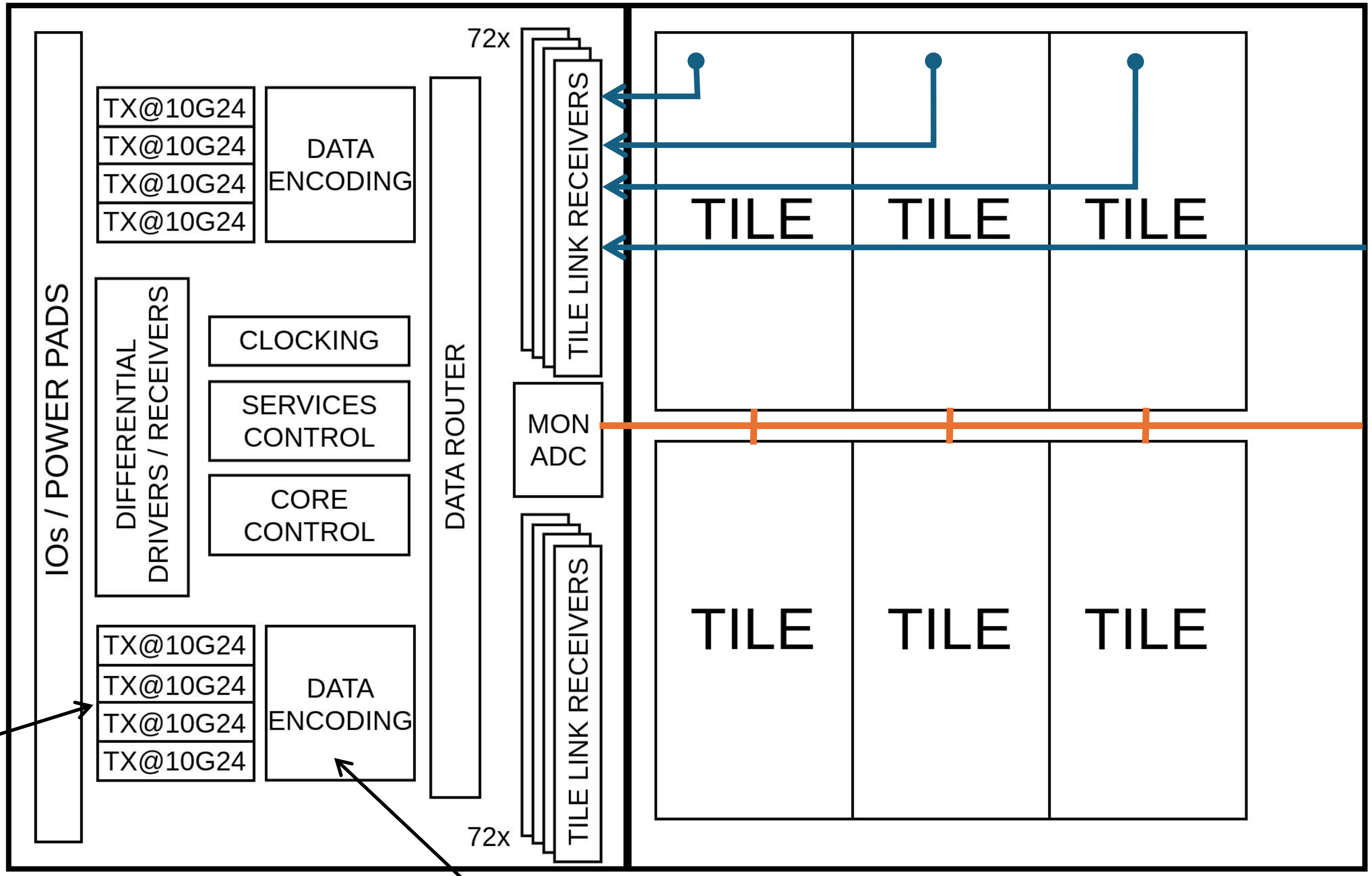
stitched backbone | SWITCHES | Pixel Matrix | SWITCHES | Pixel Matrix | SWITCHES | Pixel Matrix | stitched backbone | SWITCHES | Pixel Matrix | SWITCHES | Pixel Matrix | SWITCHES | Pixel Matrix

srv | Periphery | Periphery | Periphery | srv | Periphery | Periphery | Periphery


srv
stitched backbone
srv
Periphery
SWITCHES
Pixel Matrix
Unit bias
Unit bias
stitched backbone
Periphery
160 Mb/s
low-swing differential
resample & buffer
10.8 mm

LEC: data hub

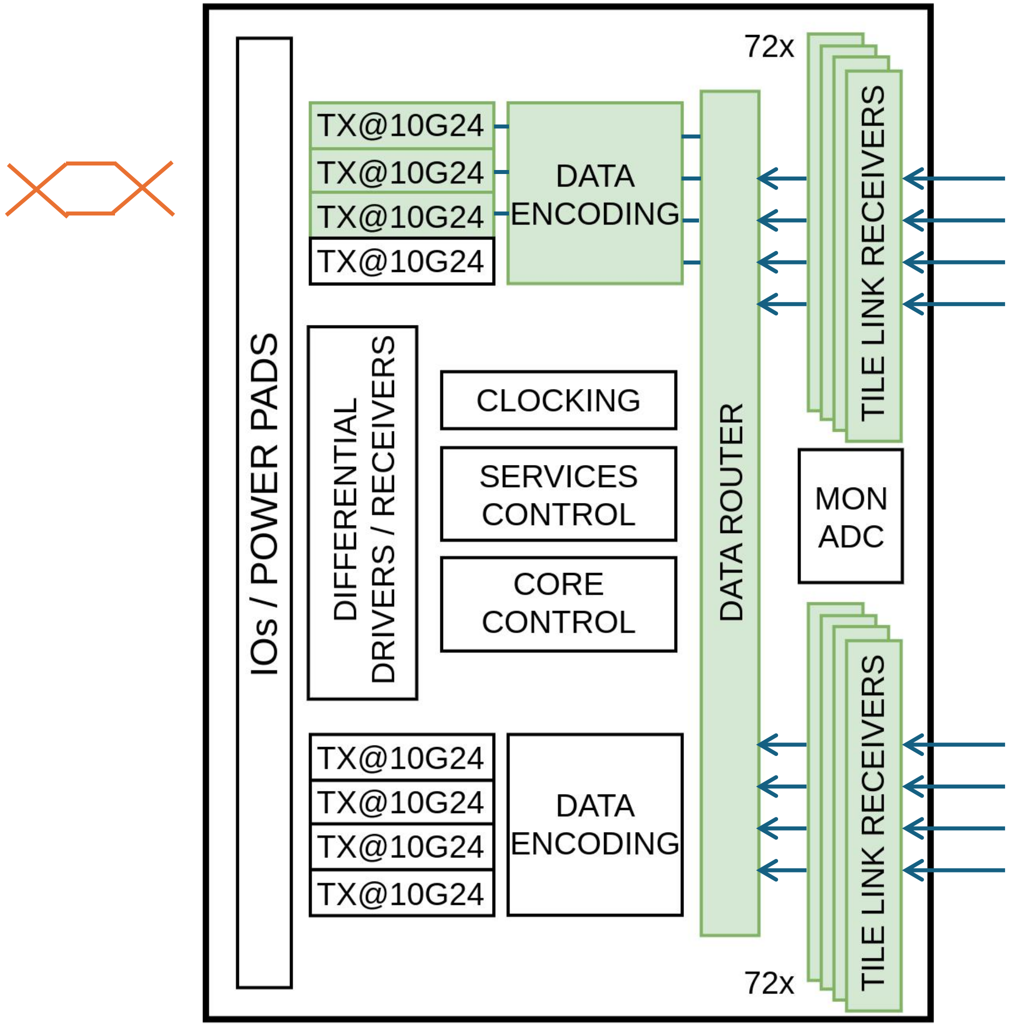
Data path is Versatile Link+ compatible



4 serializers connect to VTRX+

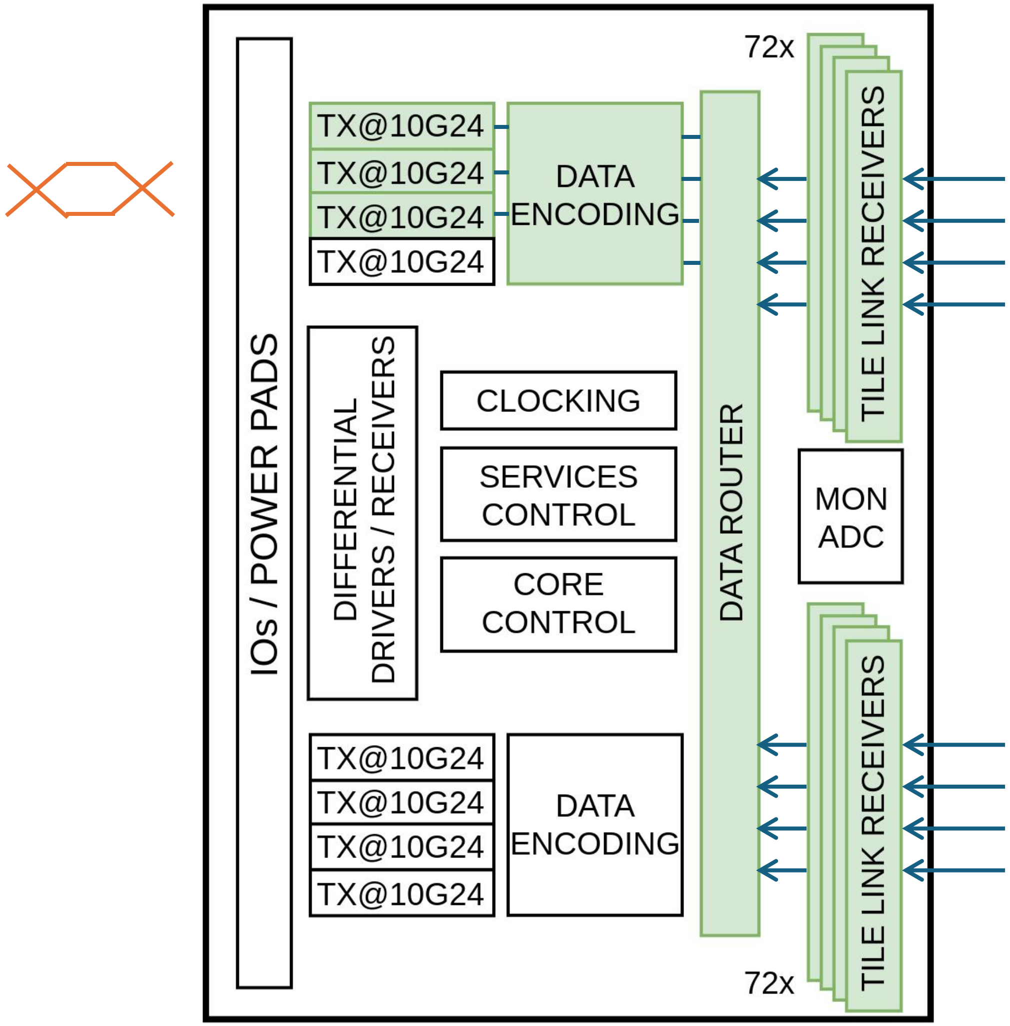
lpGBT frame encoder

[nominal operation]



10.24 Gb/s per serializer
3 serializers in use

[nominal operation]



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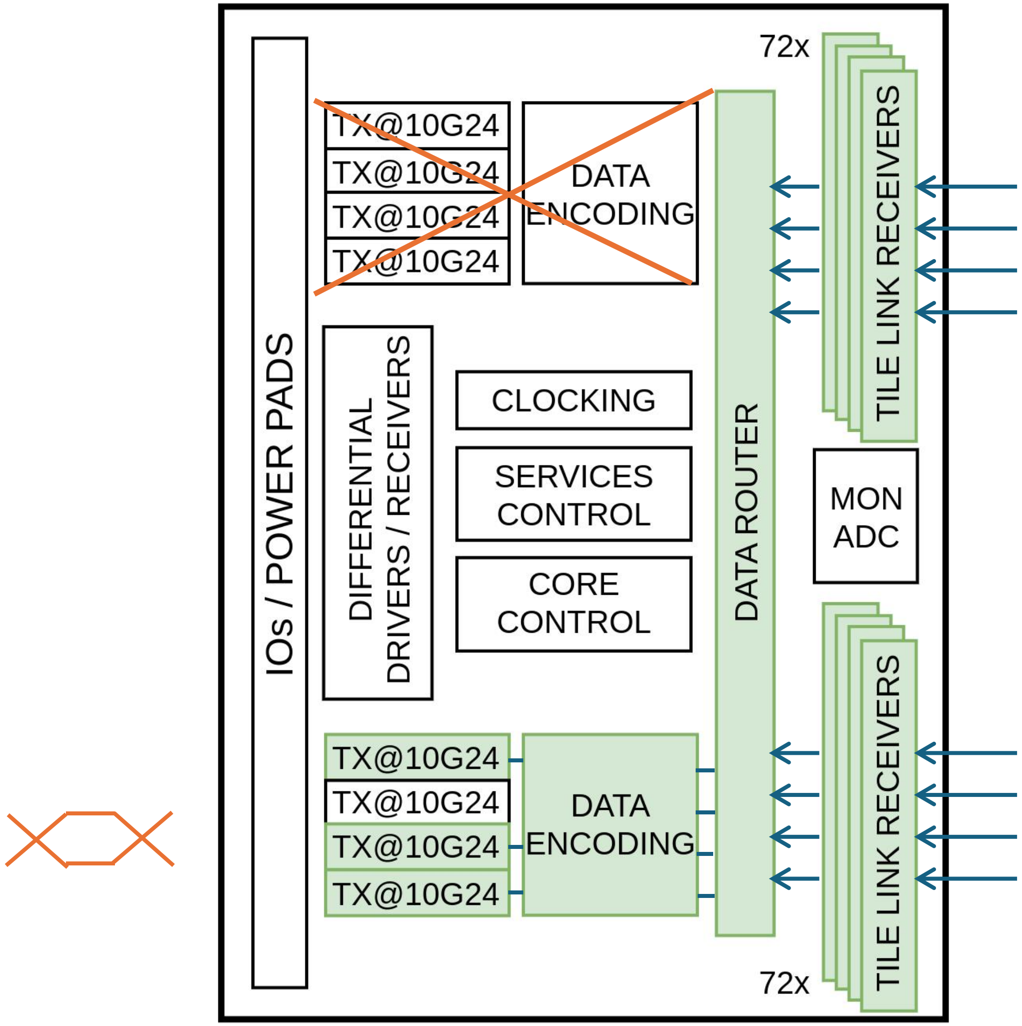
3 serializers in use

[in case of fault]



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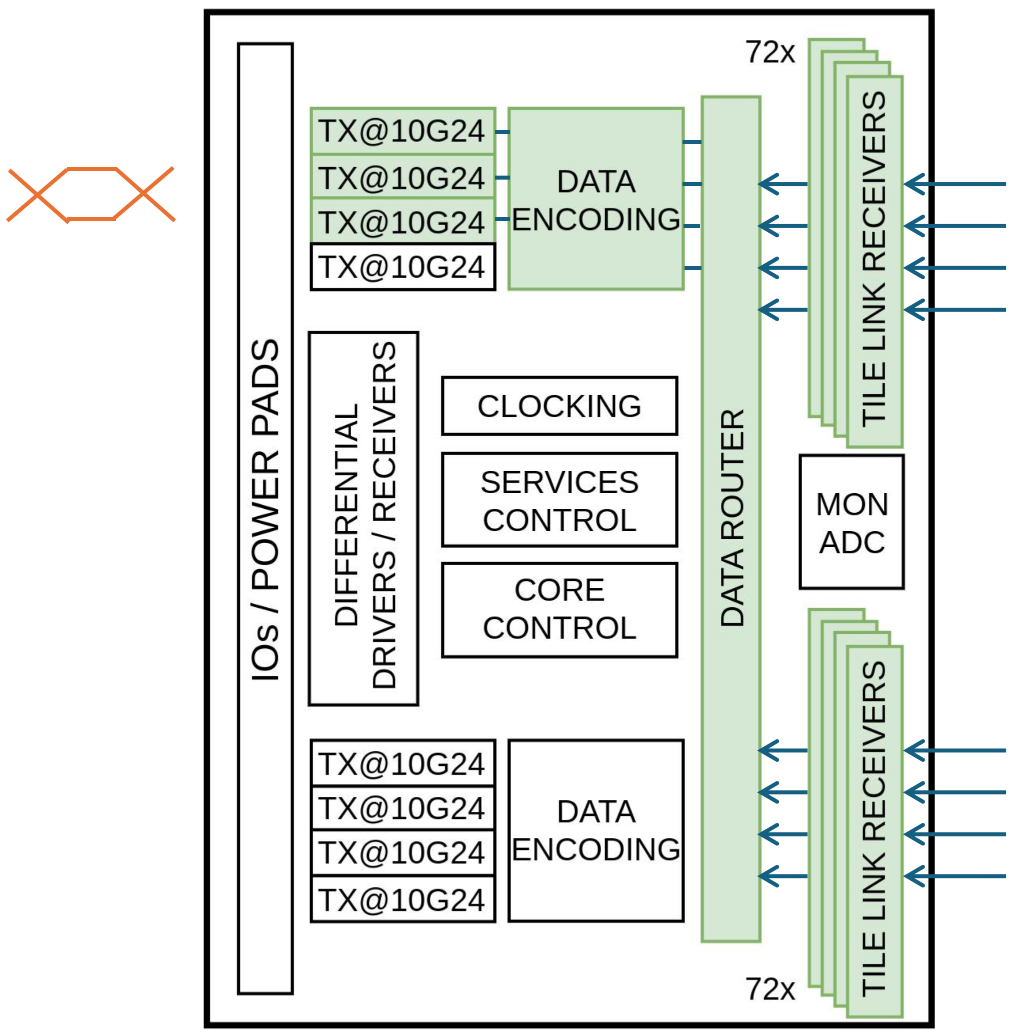

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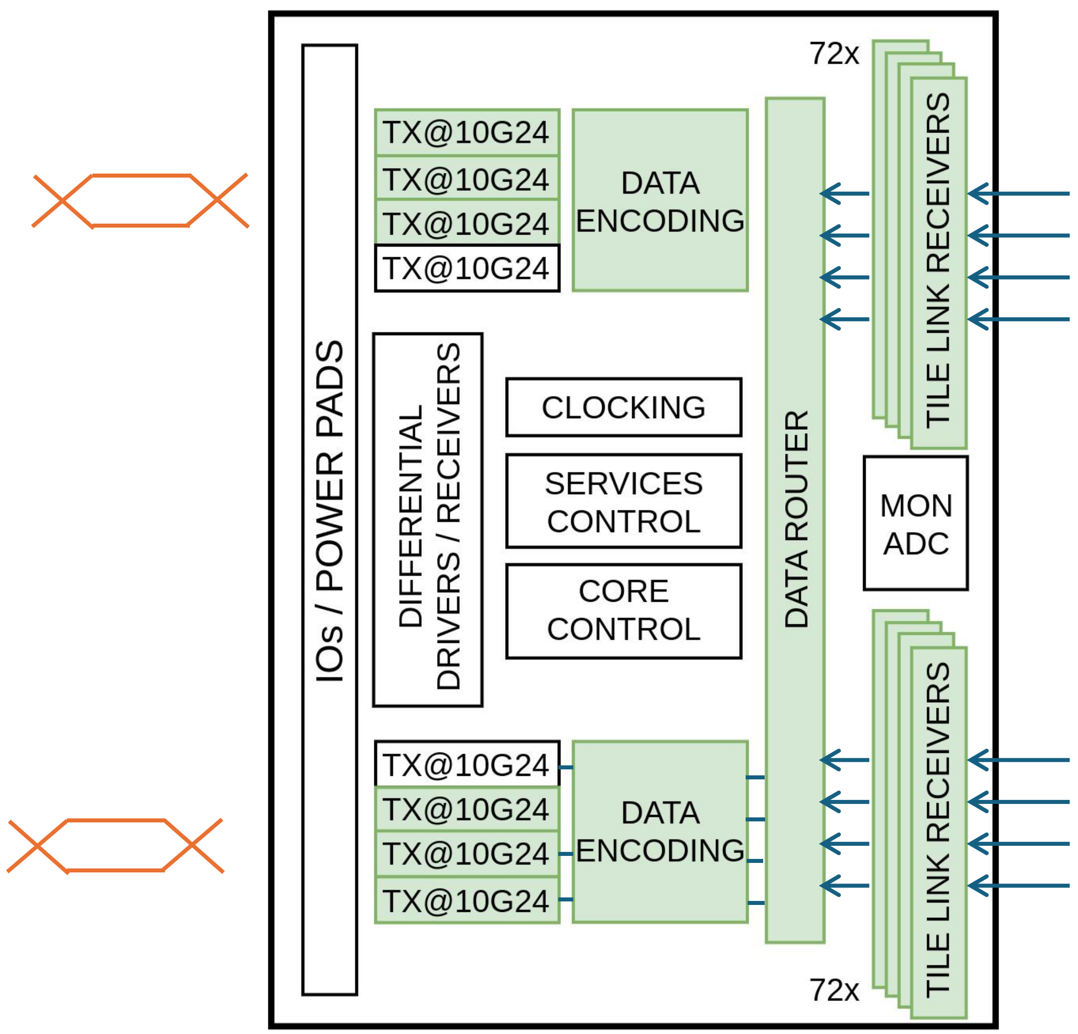


5.12 Gb/s per serializer
6 serializers in use
(bit stretching)

Yield improvement techniques

Yield improvement techniques

Switch off tiles in case of manufacturing defects

SIncreased metal spacing and wire width

Reroute data to different serializers

Increased number of vias

Developed custom standard cell libraries
(low leakage, high yield)

MOSAIX

Summary

MOSAIX

19 mm from the beam pipe

0.07 % X_0 per layer

< 40 mW/cm^2

4.4 MHz/cm^2 hit rate

93% fill factor

26.6 cm x 19 mm

26.6 cm on-chip data transmission

8x 10.24 Gb/s serializers

LpGBT frame encoding

Versatile link+ compatible

Summary

custom layout rules for yield

custom std cells for yield

TPSCo65nm imaging with stitching

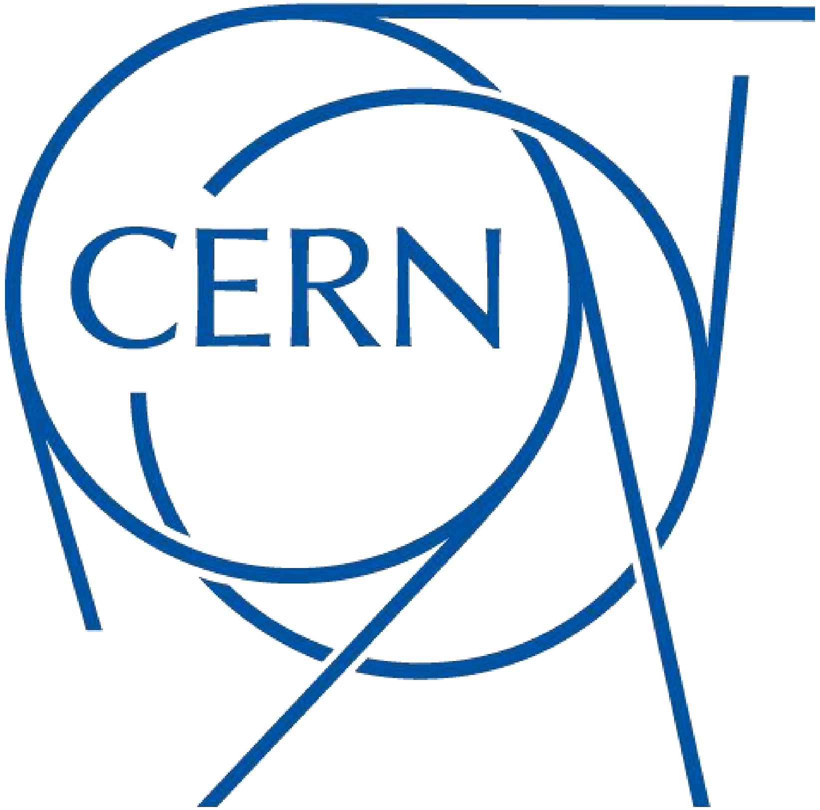
9.97 million pixels per segment

0.7% sensor area granularity

20.8 x 22.8 μm^2 pixel size

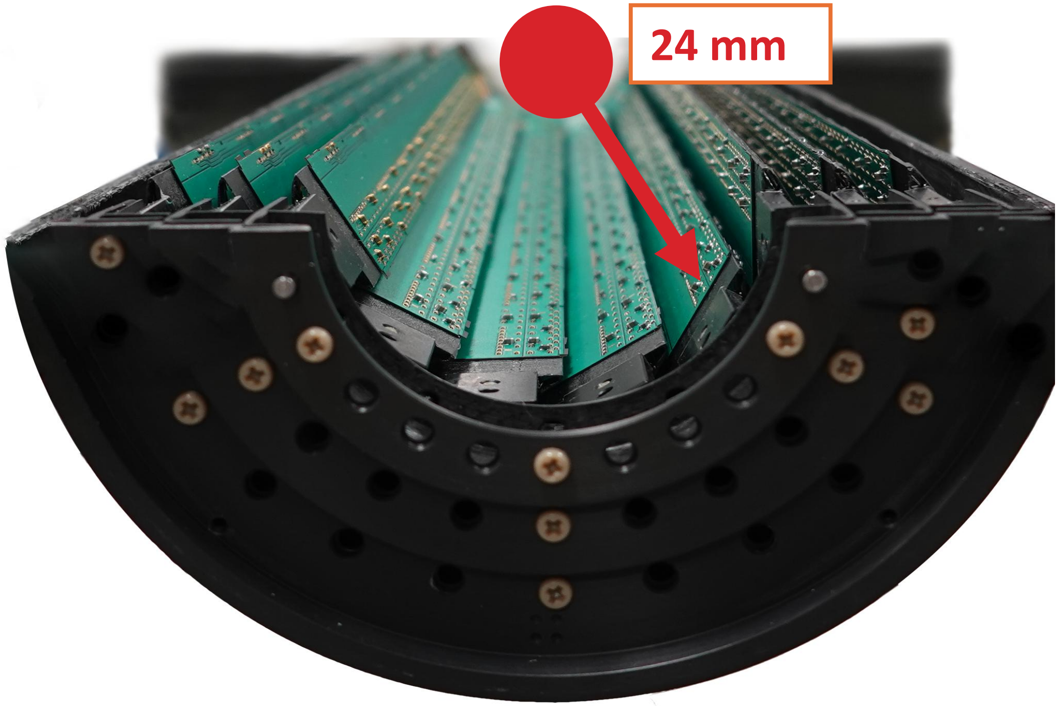
MOSAIX entering last design stage

Unprecedented in the HEP community!


CERN


ALICE

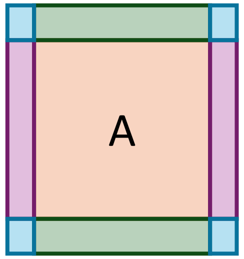
What can we do better?



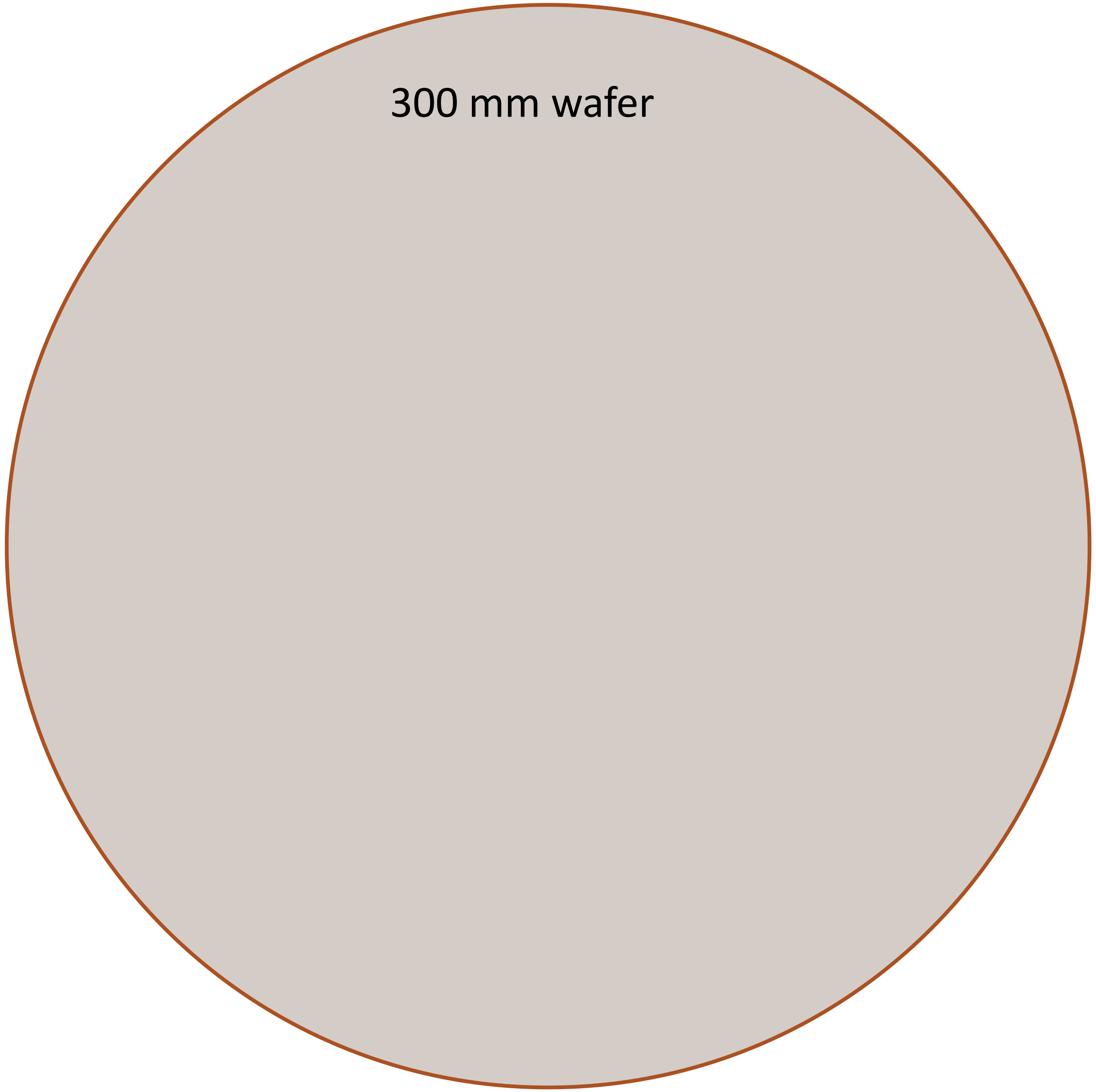
24 mm from the beam pipe
0.35 % X_0 per layer

How to design a wafer scale bent pixel detector?

Max reticle size



A = sensitive area



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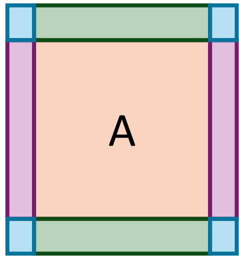
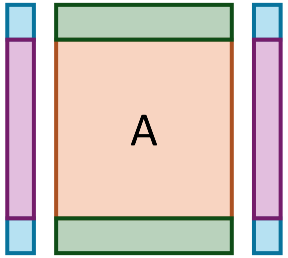


split design



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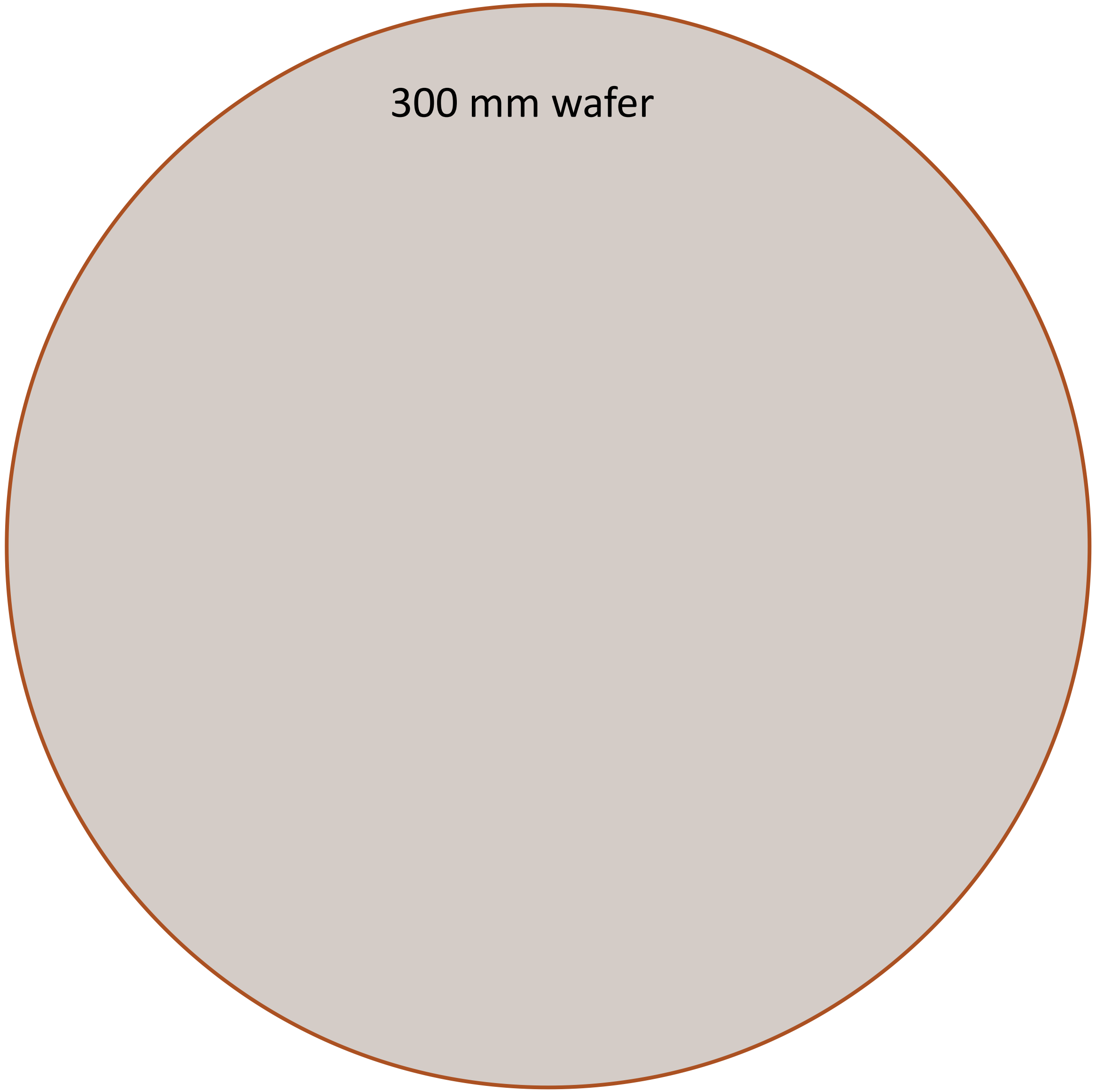

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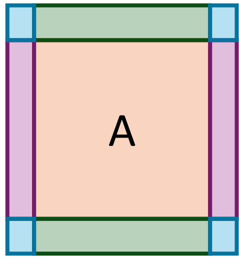

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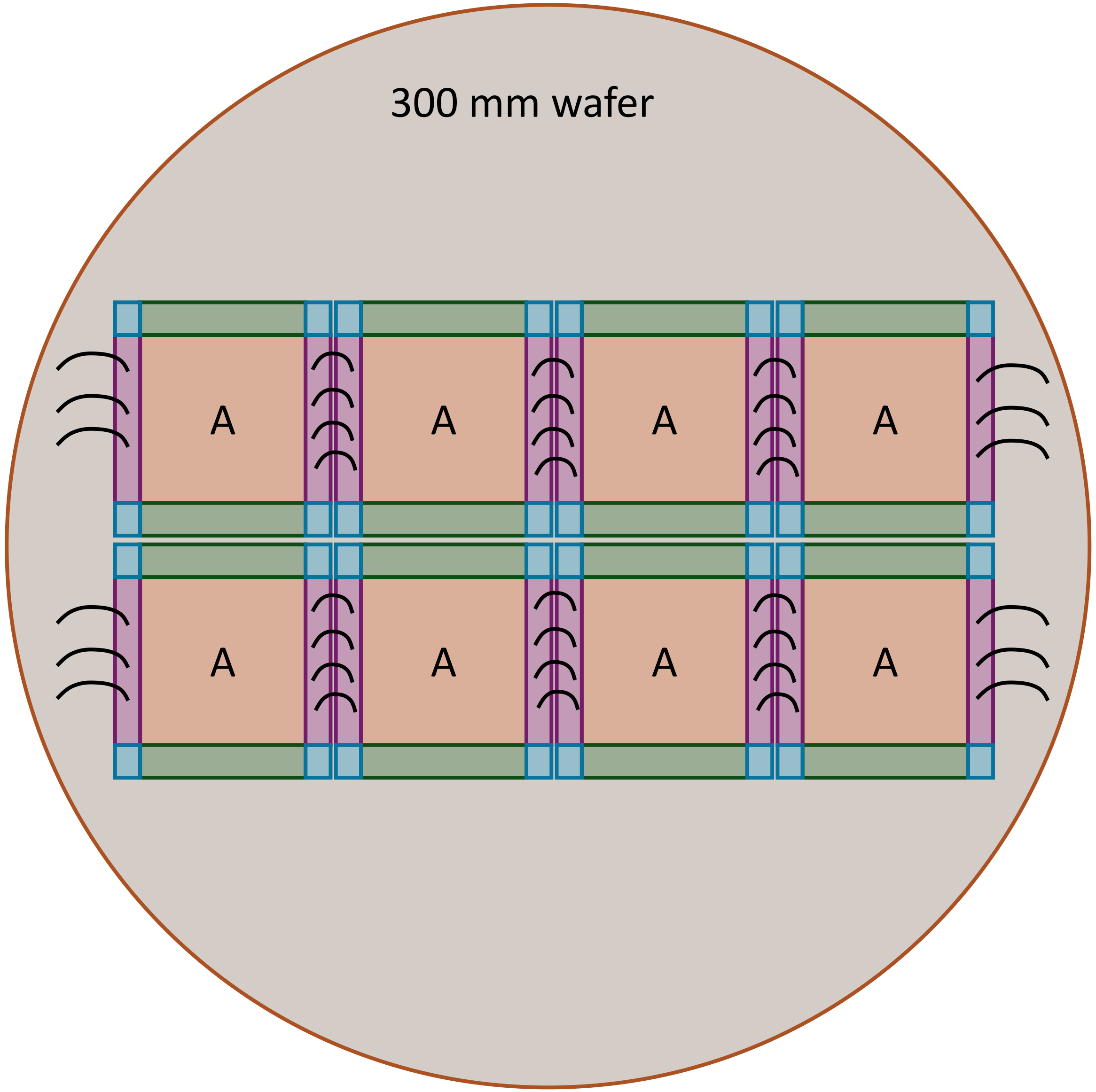

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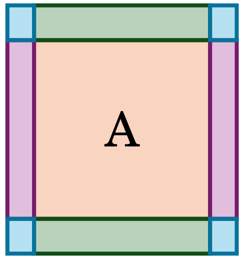

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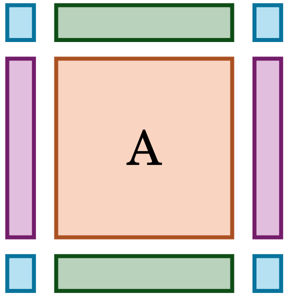
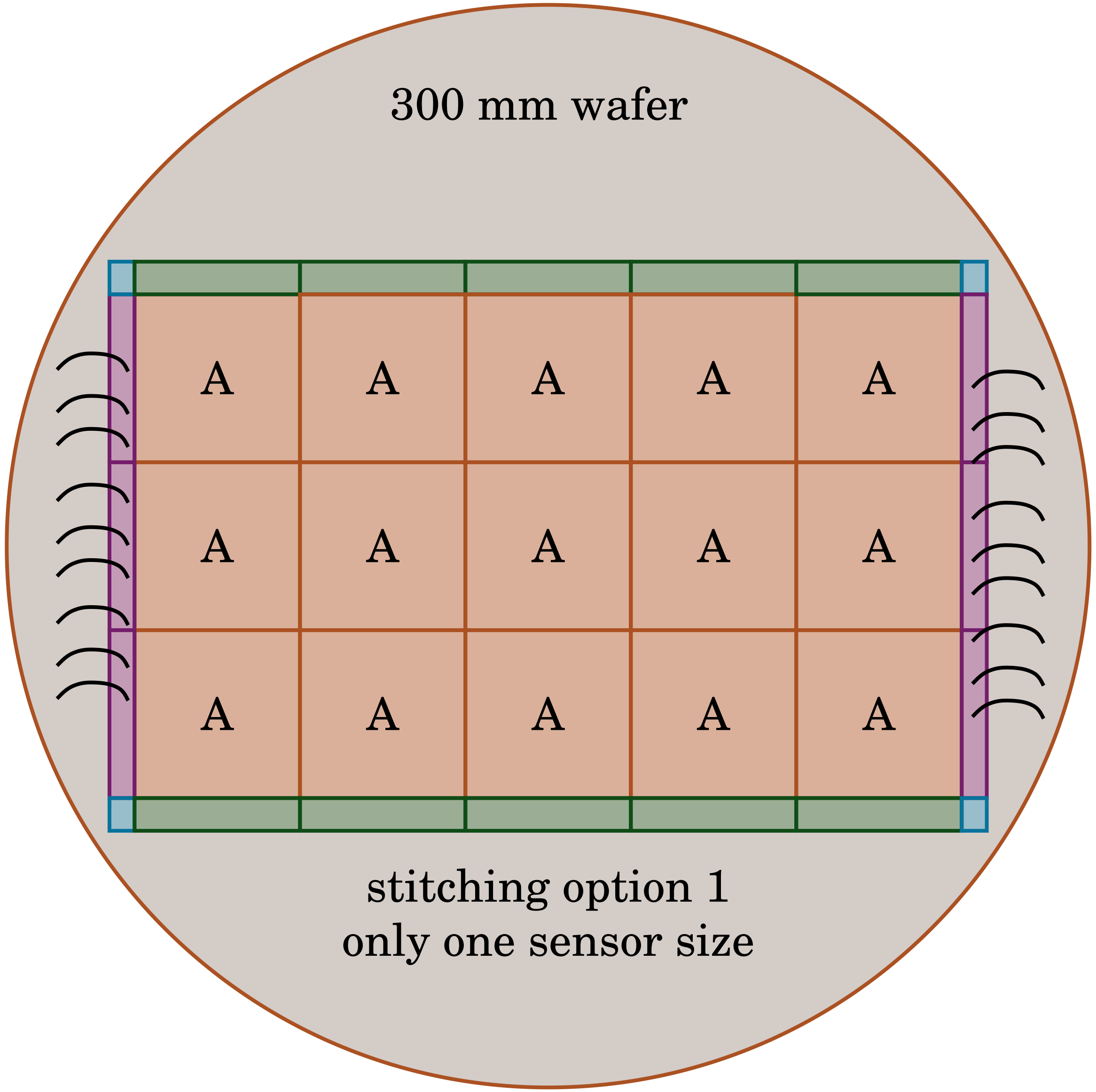
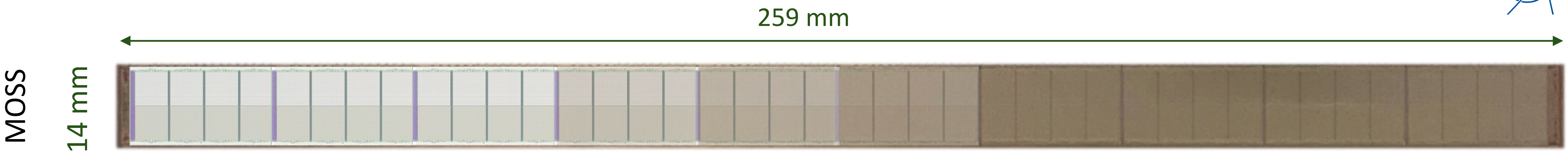



300 mm wafer

stitching option 1
only one sensor size

A = sensitive area



Two different goals

Two different approaches regarding defects

Tile = independent sensor unit

4.4 MHz/cm^2 particle flux

Continuous trigger-less readout

Integration periods of minimum 2 µs

Hits collected in time stamped packets

160 Mb/s low-swing differential data transmission