Contribution ID: **120** Type: **Oral**

Development of the MOSAIX chip for the ALICE ITS3 upgrade

Wednesday 2 October 2024 09:00 (20 minutes)

Following the ALICE ITS3 detector development line of wafer-scale monolithic stitched pixel detector prototypes in the TPSCo. 65nm CMOS imaging technology, the MOSAIX chip is the prototype of the final full-size and full-functionality ITS3 sensor.
MOSAIX has a die size of 26.6x1.96 cm2 with >94% of active area. It has 144 sensor tiles which can be powered individually to compensate for manufacturing defects. Each tile has 69.2k pixels with 22.8x20.8µm2 pixel size.
This contribution highlights the lessons learnt from the predecessors MOSS and MOST chips, summarizing the architectural decisions of the MOSAIX implementation and focusing on the yield enhancement techniques.

Summary (500 words)

The ALICE collaboration develops a novel and considerably improved vertexing detector, the ITS3, to replace the three innermost layers of the Inner Tracker System during the LHC Long Shutdown 3 at CERN.
This upgrade aims to achieve two primary objectives: reduce the material budget per layer to \mbox{0.07 \%X_0} and position the first layer closer to the interaction point at \mbox{19 mm}.
Each layer is composed of segments of a wafer-scale monolithic pixel sensor chip measuring \mbox{26.6 x 1.96 cm^2} with an active area of \mbox{$\geq$ 94 \%}.

Given the size of the wafer-scale sensor it cannot be expected to be produced free of manufacturing defects.
In order to study the yield of such devices the MOSS (Monolithic Stitched Sensor) and MOST (Monolithic Stitched Sensor with Timing) prototypes were submitted as proofs of concept using the TPSCo. 65nm CMOS imaging process with stitching technology.
Both chips employ a granular power domain scheme which allows to switch off sections of the chip in case of manufacturing defects which would otherwise render the chip inoperable.
The MOSS employs a coarse power modularity but implements conservative design rules and the MOST has a fine power modularity but uses minimum spacing design rules.

The MOSAIX chip is the second generation of the stitched sensor development and is the full-size, full-functionality prototype of the final ITS3 sensor ASIC. Following the lessons learned from its predecessors, each MOSAIX contains 144 identical tiles in the sensitive region which can be independently powered, controlled, and read out, providing a granular control of 0.7 \% of the chip's sensitive region.
Each tile features a pixel matrix array of 444 x 156 pixels with a pixel size of \mbox{22.8 x 20.8 µm^2}.
The chip's substrate can be reversed biased enhancing the sensor performance by decreasing the input capacitance which effectively increases the signal over noise ratio.
The analog front-end biasing is self-contained within each sensor tile.
The pixel matrix is read out via a double-column priority encoder with zero suppression, and the pixel hit data is transmitted over 26 cm on-chip at 160 Mb/s to a data aggregator positioned on the chip's left endcap.
To comply with the power budget of 40 mW/cm^{2}, custom standard cells were designed to both increase the yield and decrease the leakage.
The digital periphery is entirely triplicated for yield improvement and robustness against Single-Event-Effects.
The sensor tile is powered via on-chip switches and a monitoring ADC on the left endcap allows for short circuit detection during power ramp-up by monitoring the power supply of each tile.
Two slow control paths are implemented, separating the functions of chip control and power management.

Configurable data routing options provide redundancy both on- and off-chip with serializer line rates of 10.24 Gb/s or 5.12 Gb/s for off-chip data transmission.

This contribution highlights the lessons learned from the predecessors MOSS and MOST chips, summarizing the architectural decisions of the MOSAIX implementation and focusing on the adopted yield enhancement techniques.

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Session Classification: ASIC

Track Classification: ASIC