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RD50-MPW4: A thin backside-biased High Voltage CMOS pixel chip for high radiation tolerance

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The RD50-MPW prototypes are High Voltage CMOS pixel chips in the 150 nm technology from LFoundry S.r.l. aimed at developing monolithic silicon sensors with excellent radiation tolerance, fast timing resolution and high granularity for tracking applications in future challenging experiments in physics. RD50-MPW4, the latest prototype within this programme, implements significant improvements for a high breakdown voltage (> 400 V), and therefore an excellent radiation tolerance, through a multiple ring structure around the chip edge and substrate backside-biasing to high voltage. This contribution will present the laboratory evaluation of RD50-MPW4 samples irradiated with neutrons to 10^{16} $\mathrm{n_{eq}/cm^2}$ high fluence.

Summary (500 words)

The breakdown performance of silicon sensors, which constitutes the upper limit of the operating voltage and therefore constrains the radiation tolerance, can be significantly improved with advanced ring structures around the sensor edge. The charge collection efficiency can be enhanced, also after irradiation to high fluence, with substrate backside-biasing. RD50-MPW4 is a monolithic High Voltage CMOS pixel chip developed to achieve high radiation tolerance through a multiple ring structure around the chip edge and substrate backside-biasing to high voltage. The chip was fabricated in the 150 nm technology node from LFoundry S.r.l. on a p-type substrate with a nominal 3 kΩ·cm high resistivity, and thinned to 280 µm. For comparison studies all the fabricated samples can be biased through substrate contacts on the topside chip edge to high voltage. A subset of the samples was processed after fabrication to enable substrate backside-biasing to high voltage. The post-processing uses a p-plus beamline implantation with boron, metallisation and Rapid Thermal Annealing method. Non-processed and backside processed samples have been irradiated with neutrons up to 10^{16} $\mathrm{n_{eq}/cm^2}$ high fluence. Preliminary current-to-voltage measurements show a > 400 V breakdown voltage before irradiation, and a close to 800 V breakdown voltage after irradiation.

RD50-MPW4 is composed of a 64 rows × 64 columns matrix of 62 µm x 62 µm pixels with both analogue front-end and digital logic embedded inside the large charge collection electrode, and a digital periphery that implements the I2C protocol for slow control configuration and one 640 Mbits/s LVDS serial link for hit data transmission. Each pixel essentially contains sensor diode, Charge Sensitive Amplifier, comparator with 4-bit trimming to compensate small threshold voltage variations, masking electronics, edge detector, priority logic, and two 8-bit dynamic RAMs plus one 8-bit ROM to store the hit data inside the collection electrode. The hit data consists of an 8-bit leading edge time-stamp and an 8-bit trailing edge time-stamp, which give the Time-over-Threshold, and an 8-bit pixel address. The time-stamp clock is provided by an on-chip common 40 MHz time-stamp generator. The chip uses the triggerless column-drain readout architecture. The pixels are implemented following a double column scheme. There is one End-Of-Column per double pixel column, which receives the hit data from pixels with higher addresses first and stores it in a 24-bit FIFO with capacity for 16 hits. The readout of the 32 End-Of-Columns is controlled by a token handler, which connects each individual End-Of-Column one after the other with a 32-bit buffer register to temporarily store the hit data together with an 8-bit End-Of-Column address. The 32-bit data is then pushed from the buffer register into a 32-bit transmission FIFO with capacity for 64 hits, and the token is given to the following End-Of-Column. The data is framed and encoded before is finally read out with the 640 Mbits/s LVDS serial link.

This contribution will review the design of RD50-MPW4 and present the laboratory evaluation of irradiated samples, with topside and backside biasing, to further study the radiation tolerance of this technology.

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