HKROC: an integrated readout chip designed to facilitate the readout of a large number of photomultiplier tubes for the next generation of neutrino experiments

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Organization for Micro-Electronics desiGn and Applications

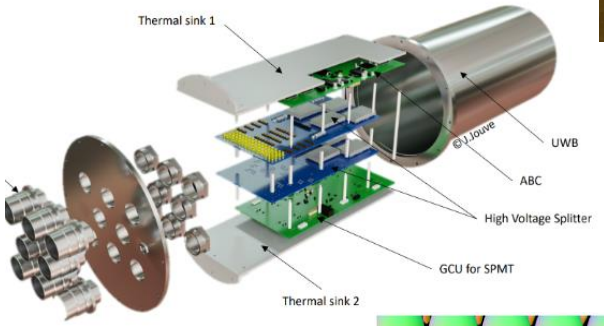
A read-out for multi-ton neutrinos experiments

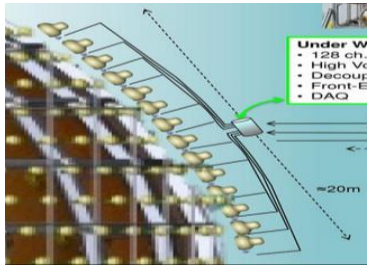
The **HKROC ASIC** was originally designed to read out Photomultiplier Tubes (**PMTs**) for the **Hyper-Kamiokande** experiment.

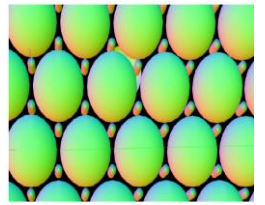
As next-generation neutrino experiments continue to expand in scale, with an increasing number of PMTs,

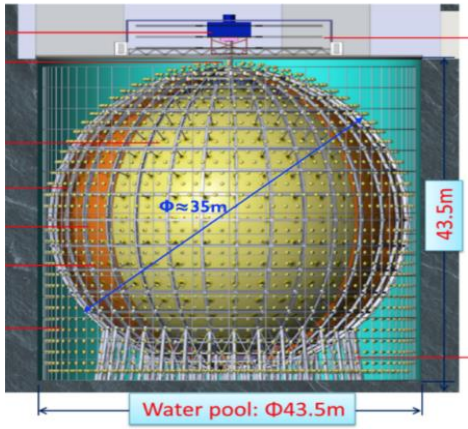
there is a growing need for **fully integrated electronic systems**.

- Multichannel
- Auto-trigger acquisition mode
- High speed
- Low noise
- Large dynamic range
- Precise charge and time measurements









Omega has extensive experience in **ASIC design for neutrino physics**,

having developed several ASICs in recent years:

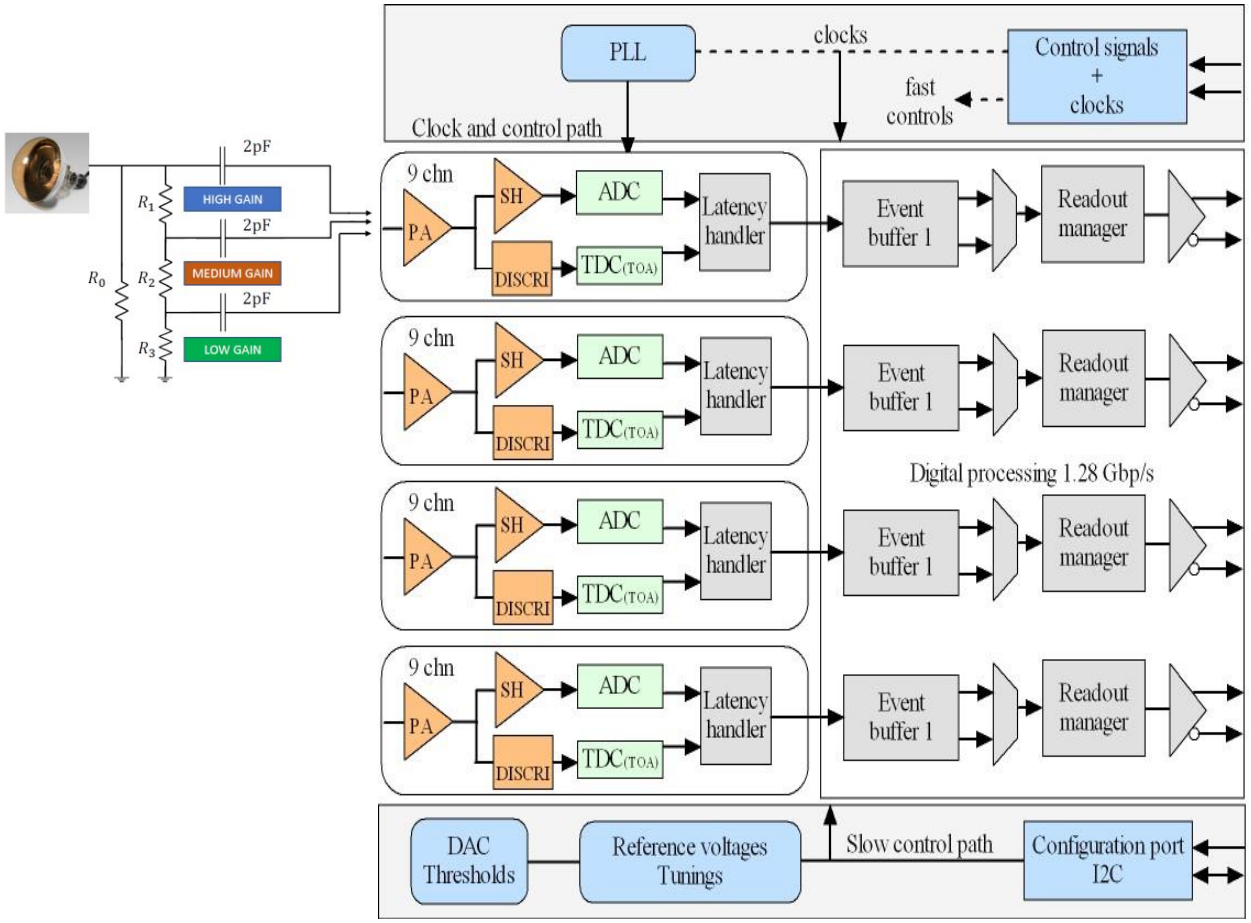
PARIROC 2007	BiCMOS SiGe 350 nm	**First ASIC** that was a veritable **SoC** in auto-trigger mode
CATIROC 2015	BiCMOS SiGe 350 nm	Based on the PARISROC ASIC, which will be installed in the **SPMT system of the JUNO detector** (China)
HKROC 2020	CMOS 130 nm	**Based on the ASIC HGCROC** for the CMS High Granularity Calorimeter

From physics to electronics specifications

1 p.e. = 2 pC

Physics constraint	Impact on electronics requirement
Detect synchronous & asynchronous events (accelerator/atmospheric/solar/supernova neutrinos, p decay)	**Self triggering** for each channel
No event loss (e.g. crucial for SN neutrino)	**High hit rate** (e.g. 1 MHz)
Low energy events detection (e.g. SN or solar neutrino)	**Low threshold** triggering (e.g. <= **1/6 p.e.)**
Charge reconstruction from low to high energy physics	**Large dynamic charge** range (**1 − 1300 p.e.**) photoelectrons
Excellent charge reconstruction	**High linearity (~ 1%)** and **resolution (~ 1%)** - 0.1 p.e. for < 10 p.e. - < 1% for >10 p.e.
Electronics time resolution < PMT time resolution (1.3 ns)	Timing resolution (e.g. < 0.3 ns) **300 ps** for **1 p.e.** **200 ps** for **> 6 p.e.**
Low power consumption	50 mW/ PMT channel

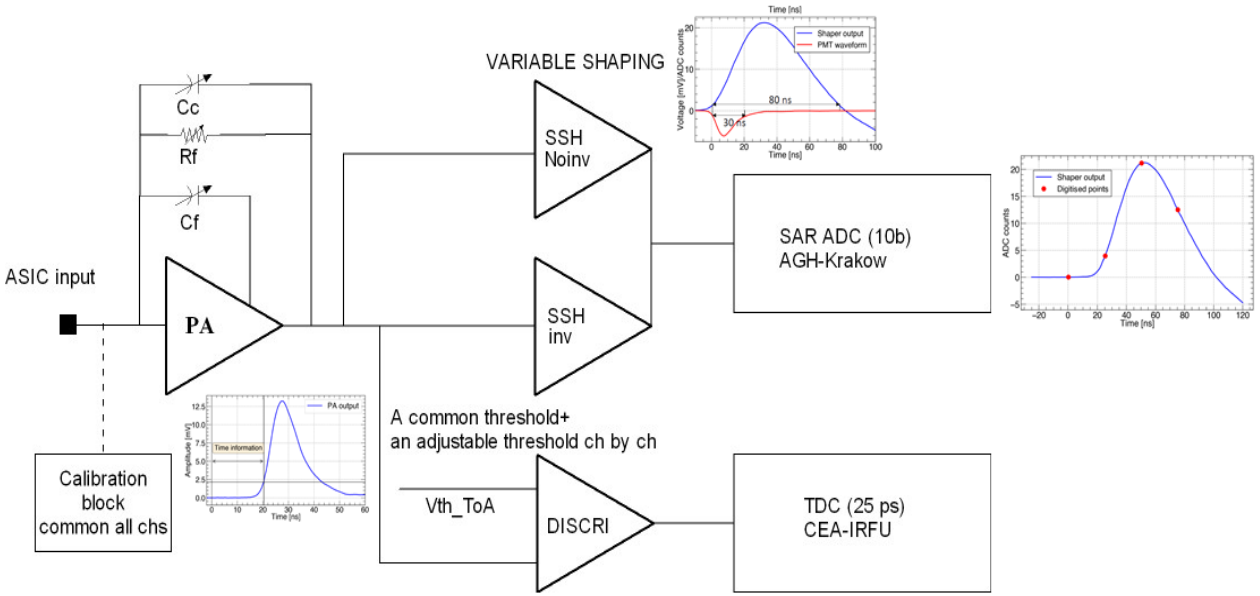
HKROC architecture



- ASIC developed in **130 nm CMOS** technology (1.2 Volts)
- **36** input channels → **12** PMT channels
- **Charge** and **time** measurements:

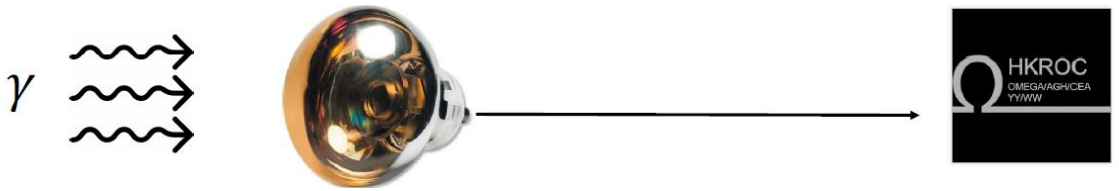
  Slow path: shaper+10b SAR-ADC @ **40MHz**,

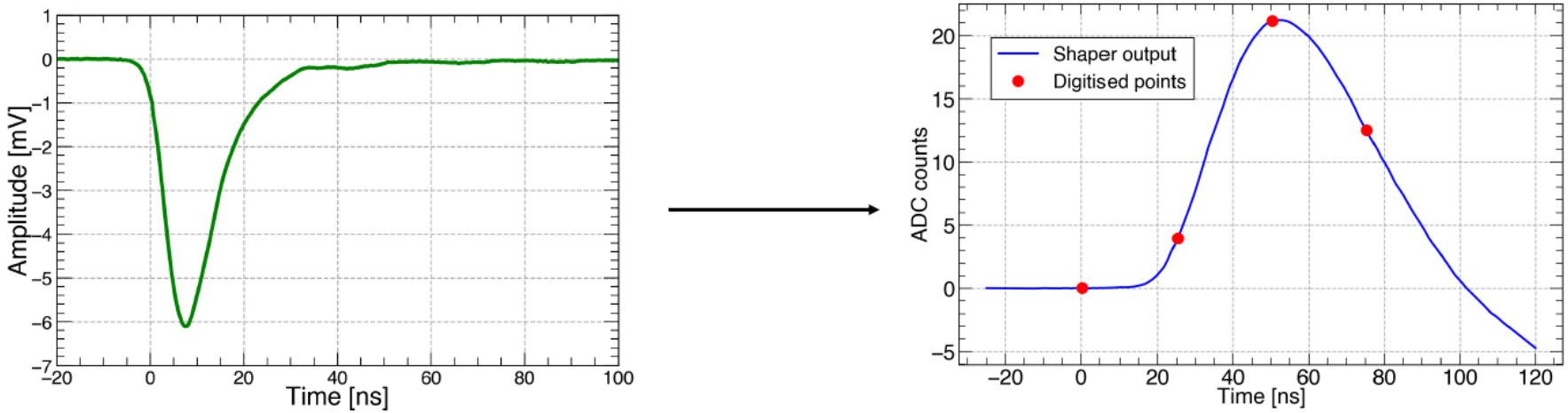
  Fast path: discriminator + 10b TDC (LSB= 25 ps)
- 4 readout high-speed links (1.28 Gbps) → 1 read-out → 3 PMTs
- **I2C** protocol to load ASIC parameters
- 320 MHz fast commands
- Power consumption 10 mW / channel



HKROC waveform digitizer

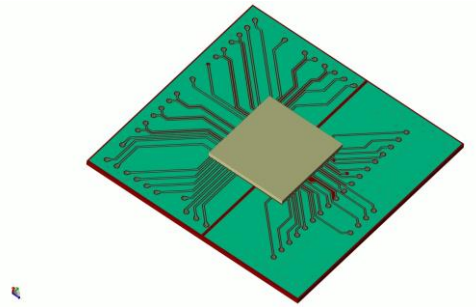
- **The shaper signal digitized** at 40 MHz by a **10 bits SAR** (Successive Approximation) **ADC (***AGH-Krakow group)(***DOI** 10.1088/1748-0221/18/11/P11013)
- **For each trigger:** a **coarse time-stamp** (24 bits) common for all channels (at 40 MHz) and a **fine timestamp** for each channel using a 10 bits TDC (LSB=25ps) (*CEA group) (**DOI**: 10.1109/TNS.2023.3335657*)
- **The ASIC is a Waveform digitizer**: when one trigger happens (ToA≠0) **N sampling points** separated by 25ns **are captured and saved in the internal memory . N is variable by slow control** (from 1 to 7)

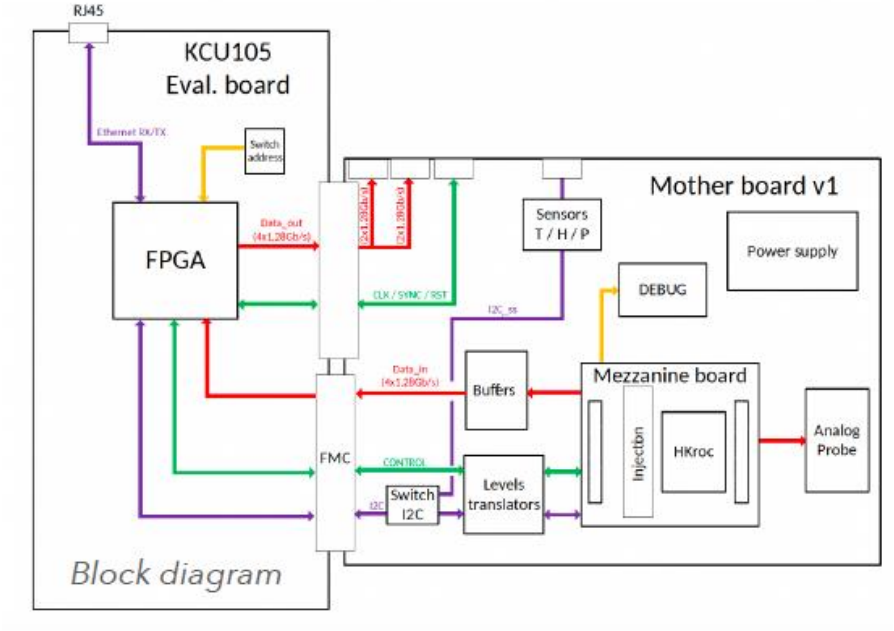




HKROC measurements

- **HKROC0**, produced in **2020** (**to see TWEPP 2022**), showed good performance that fitted well with the Hyper-K requirements, except for an extra crosstalk that affected the charge measurements.
- **HKROC1B**, produced in **2022**, was designed to reduce the crosstalk observed in HKROC0. It demonstrated good overall performance, with a significant reduction in crosstalk (see next slides).
- **HKROC1C** was produced in **2023** and received a few months ago. It is currently under test
  - ✓ Diffuse crosstalk is being tested
  - ✓ Global test are ongoing



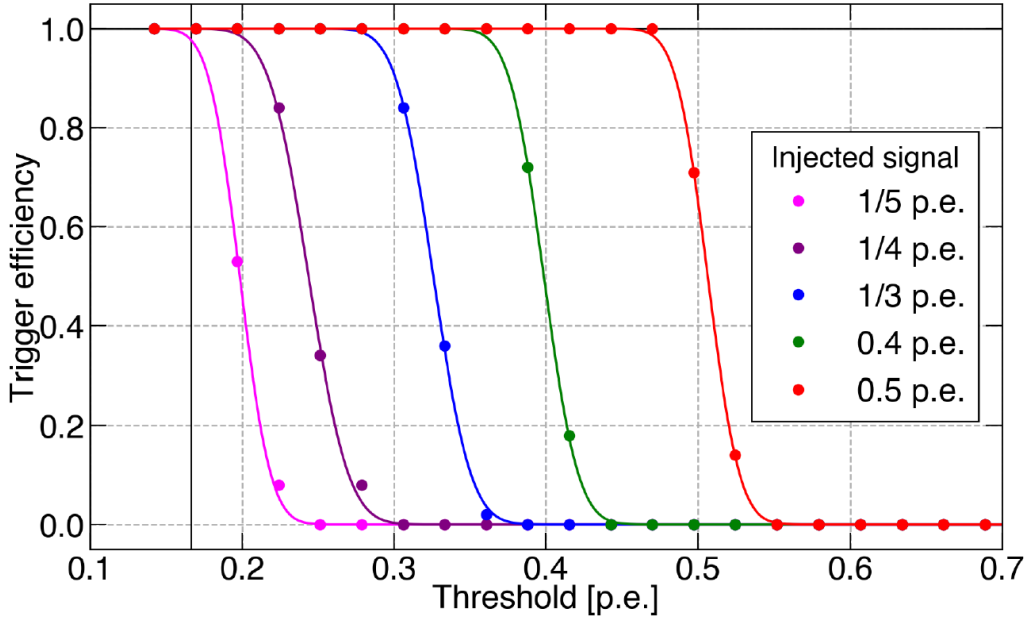


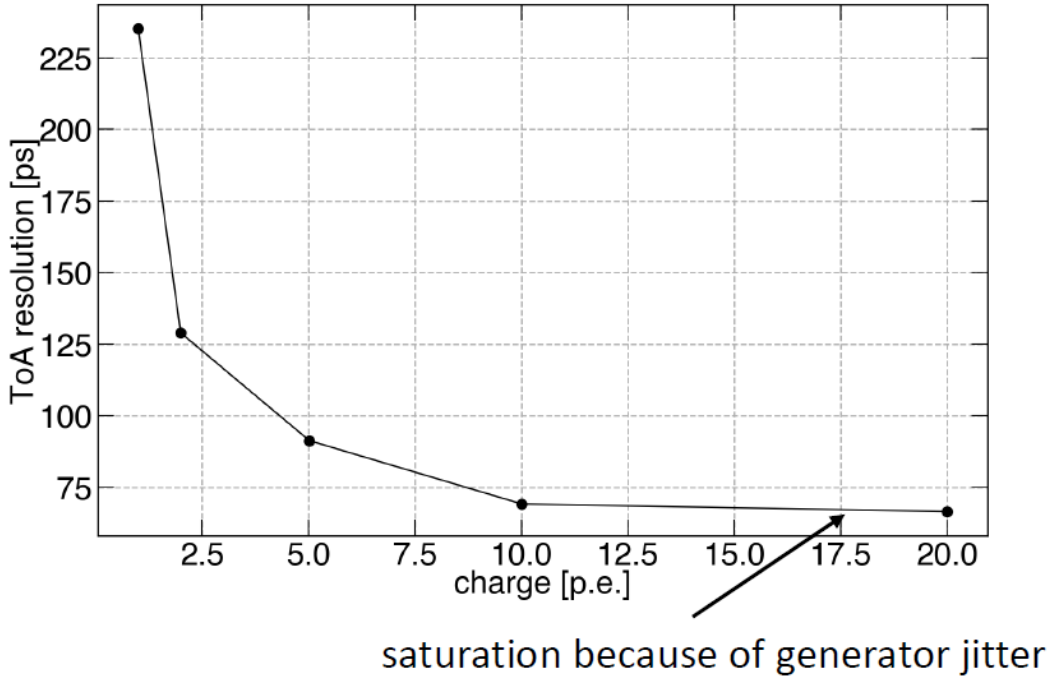
First board with mezzanine

Digitizer V1

HKROC1B general performances

The second version of the ASIC (**HKROC1B**) is completely tested and it showed good overall performance, similar to the first version (HKROC0)





Trigger threshold = 1/6 p.e. > 90% efficiency for signal as low as 1/5 p.e.

Noise amplitude < 1/22 p.e.

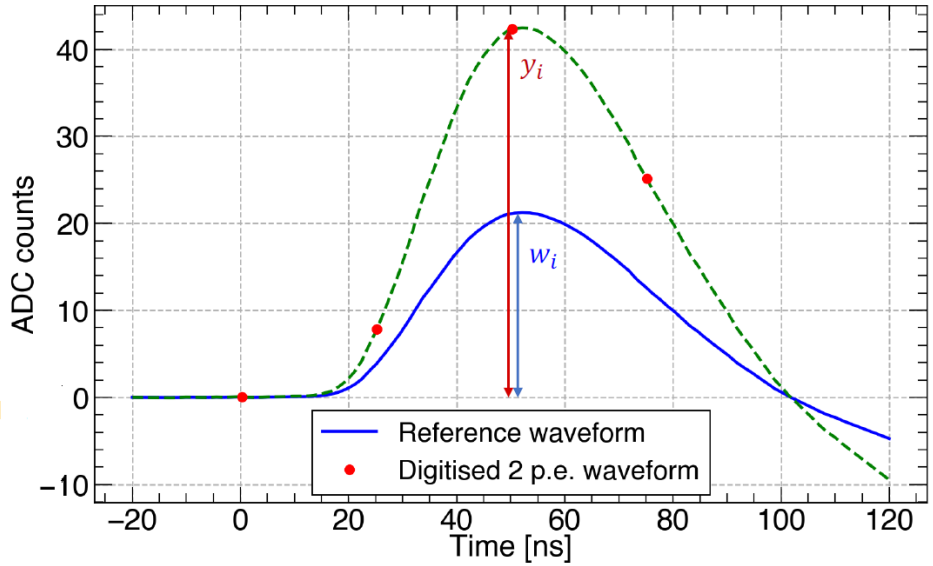
TDC characterization with 1/6 p.e. threshold

TDC resolution:

225 ps std @ **1 p.e**

60 ps std @ >**10 p.e** (intrinsic resolution 25 ps)

Charge reconstruction

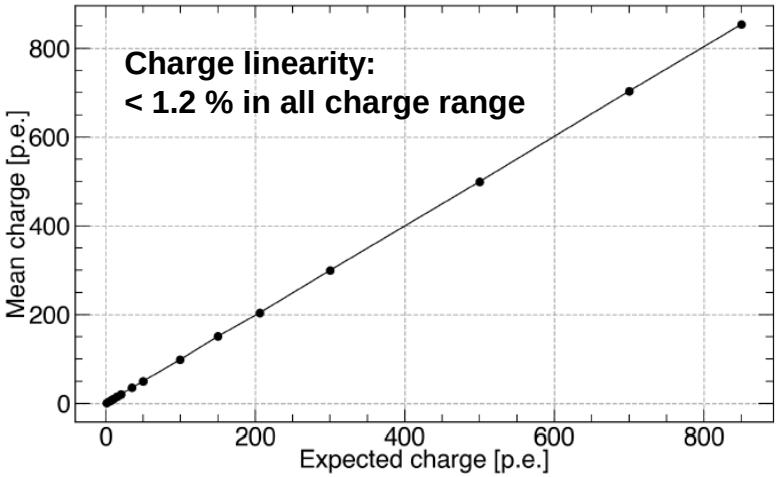


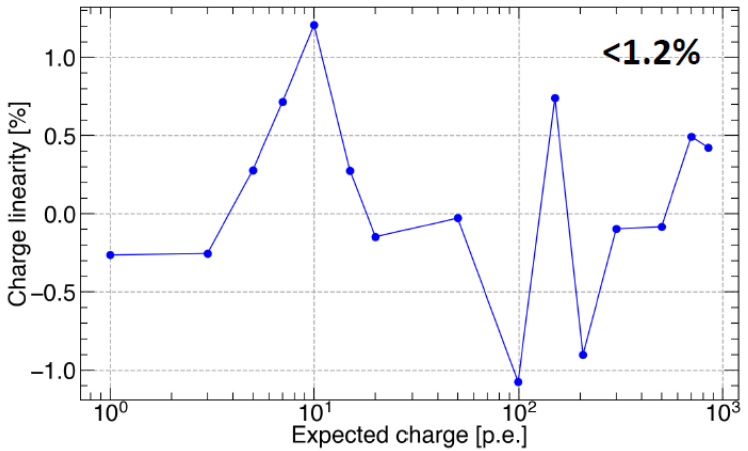
The digitized charge must be reconstructed offline in the FPGA.

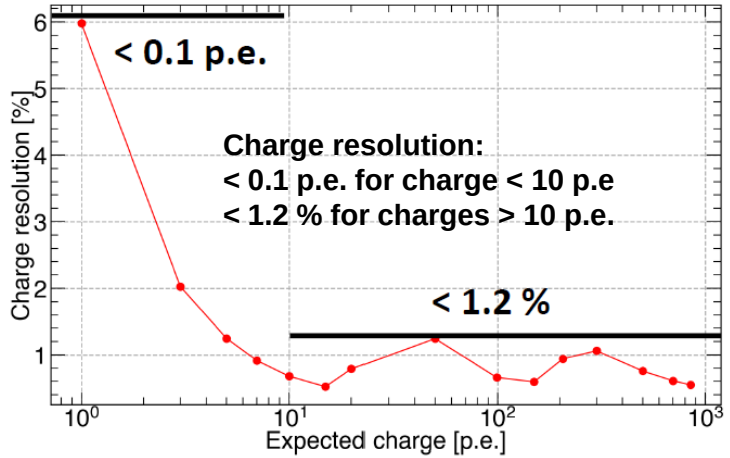
The charge reconstruction method consists of two steps:

- Build a **reference waveform** to calibrate each channel:
  - ➞ High gain channel : 1. p.e.
  - ➞ Medium gain channel : 20 p.e.
  - ➞ Low gain channel : 200 p.e. 2.
- Given a **digitized waveform**, find the associated charge :

$$\chi^2(\alpha)=\sum_1^N\left(\frac{yi-\alpha wi}{\sigma i}\right)^2 \qquad \frac{d\chi^2}{d\alpha}=0 \iff \alpha=\frac{\sum_1^N \frac{yiwi}{\sigma i^2}}{\sum_1^N \frac{wi^2}{\sigma i^2}} \Longrightarrow q=\alpha q_{ref}$$





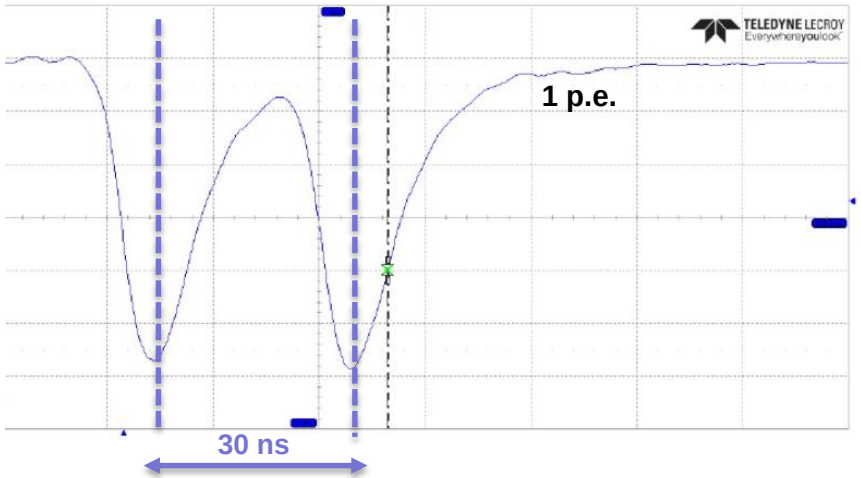


Pile-up et dead time

- The HKROC saturation naturally appears when the chip internal memory is full.

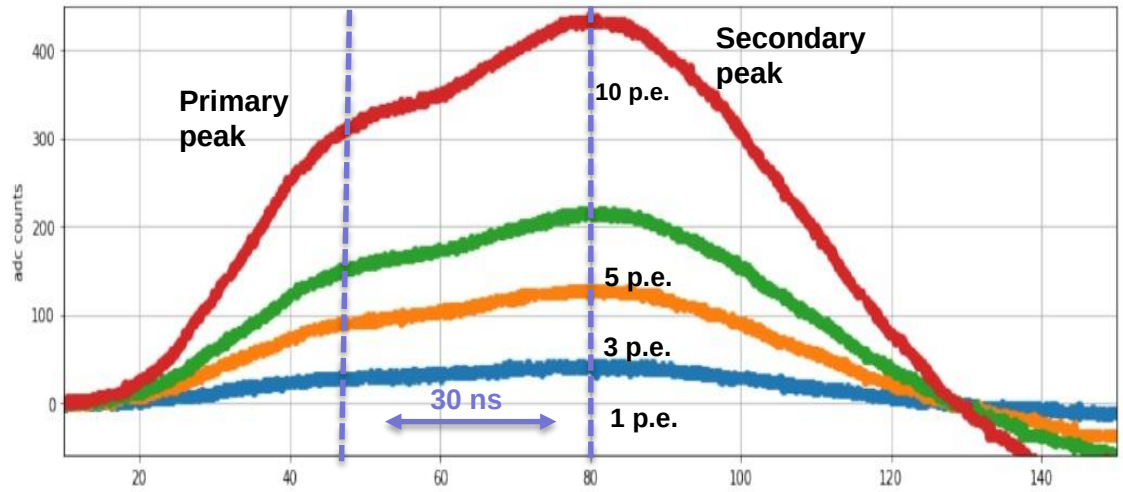
  The chip has one independent memory for each read-out link at 1.28 Gb/s
- **ASIC hit rate**: ~**400 kHz/PMT**, up to **1 MHz/channel**, but we have tested the ASIC with pile-up events at a 30 ns delay time.

The **HKROC feature to be a waveform digitizer** and **the charge reconstruction method** allow the differentiation of **events at extremely high frequencies**



Events with separate timestamps > 30 ns→ **2 trigger times**

Dead time **30 ns**



Accurate charge reconstruction of pile-up:

➞ Charge linearity ~ **1%**

➞ Charge resolution:

< **0.1 p.e.** for charges **< 5 p.e.**

< 0.17 p.e. @ 10 p.e.

HKROC crosstalk – Diffuse crosstalk

Two crosstalk observed already in the first prototype HKROC0:

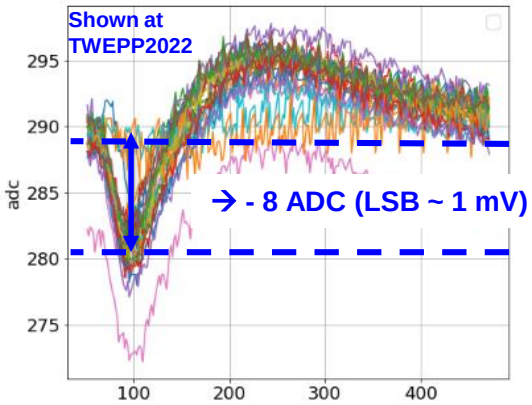
- One defined "**Diffuse crosstalk**" → A negative crosstalk observed in all the channels
- The second one defined "**Close crosstalk**" → A positive signal was observed in the close channels

The Diffuse Crosstalk **ADC for 1 p.e. signal is 22 ADC**

HKROC0

850 p.e. injected in one channel

→ signal observed in all channels



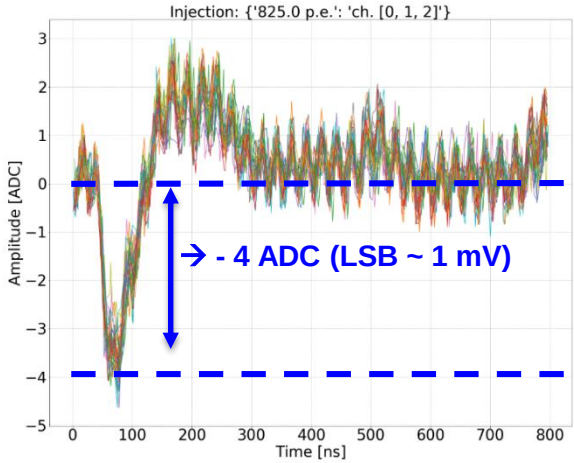
Reproduced in simulations

Three main sources of crosstalk:

- The **PA bias**,
- The **shaper references**
- The **input calibration block**

HKROC1B

850 p.e. injected in one channel

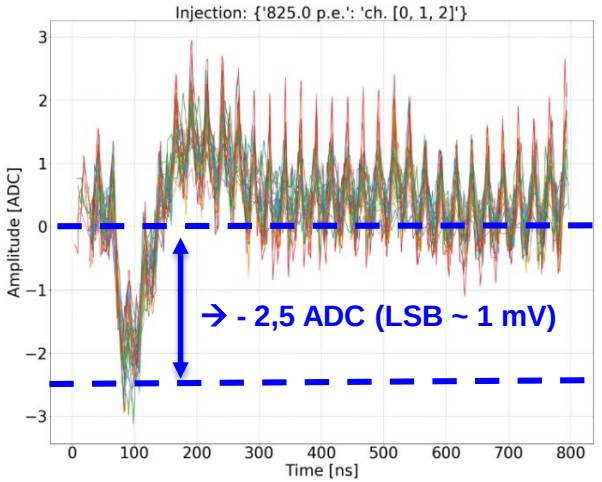


Schematic corrections

- The **more sensitive points** of the PA bias and shaper references, were **put on pins** in order to add **decoupling capacitances** on the board.
- A **new input calibration block** structure was implemented

HKROC1C

850 p.e. injected in one channel



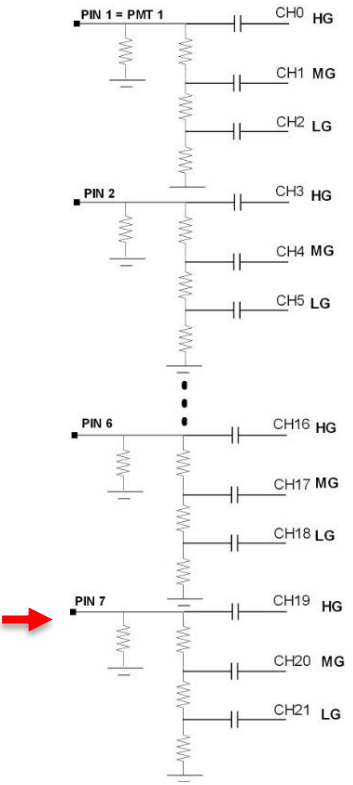
Schematic corrections

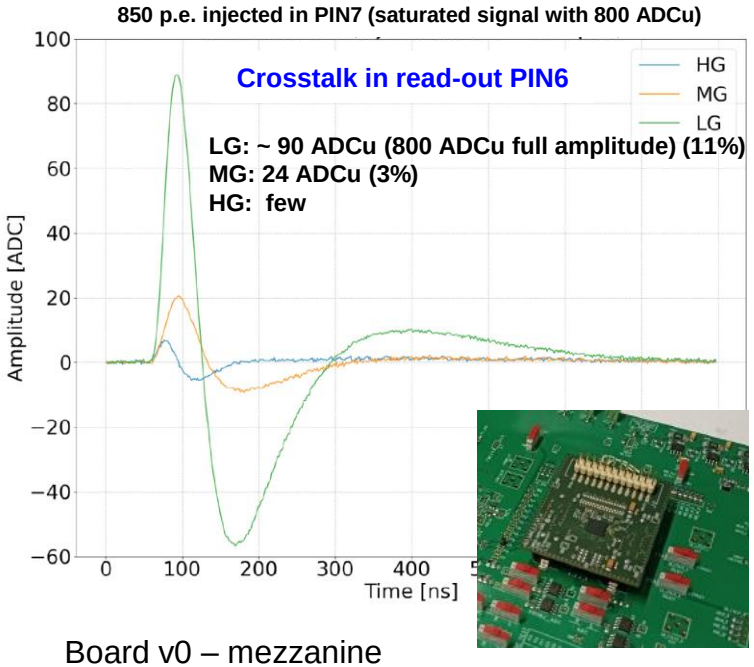
- The **bias of the PA input stage** (vbi_pa) was put **on a pin** in order to add decoupling capacitances on the board.

Close crosstalk

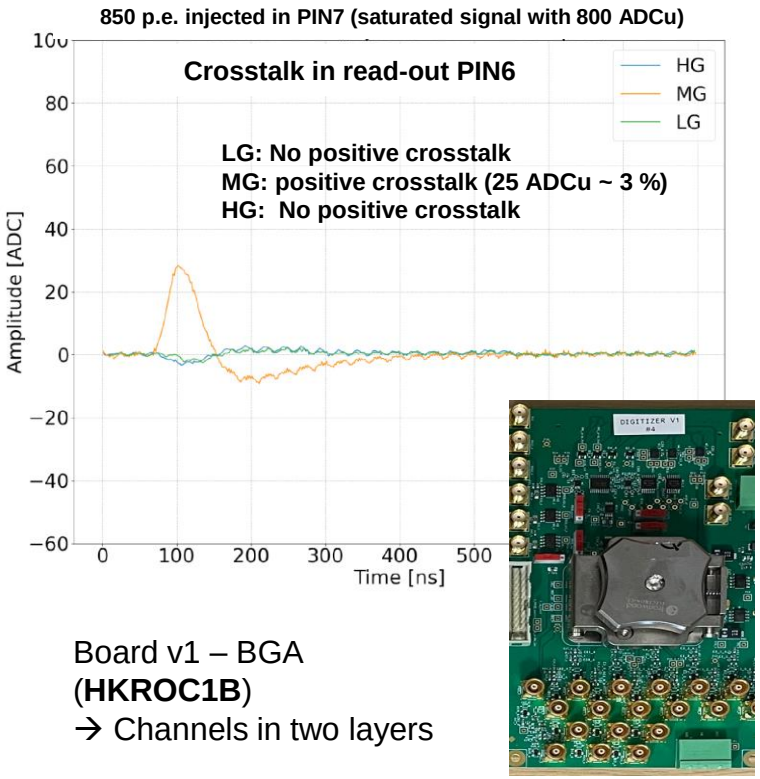
A large signal of 850 p.e. is injected into one pin (PIN7), affecting three ASIC channels, and an additional positive signal is observed only on the adjacent PIN6. This crosstalk was not reproduced in simulations, suggesting that it originates externally to the ASIC (in the BGA substrate and test board).

- A **BGA substrate** was designed with **additional layers** to separate the input into EVEN and ODD channels
- A **new board** for BGA packaging was also designed with **two layers**, dedicated to EVEN and ODD channels.

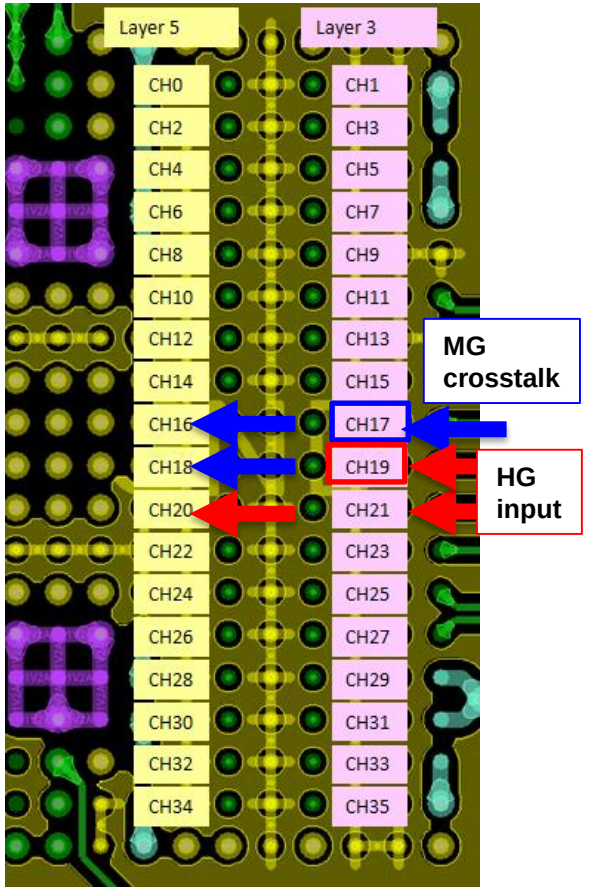




Board v0 – mezzanine (**HKROC1B**)
→ Channels in one layer



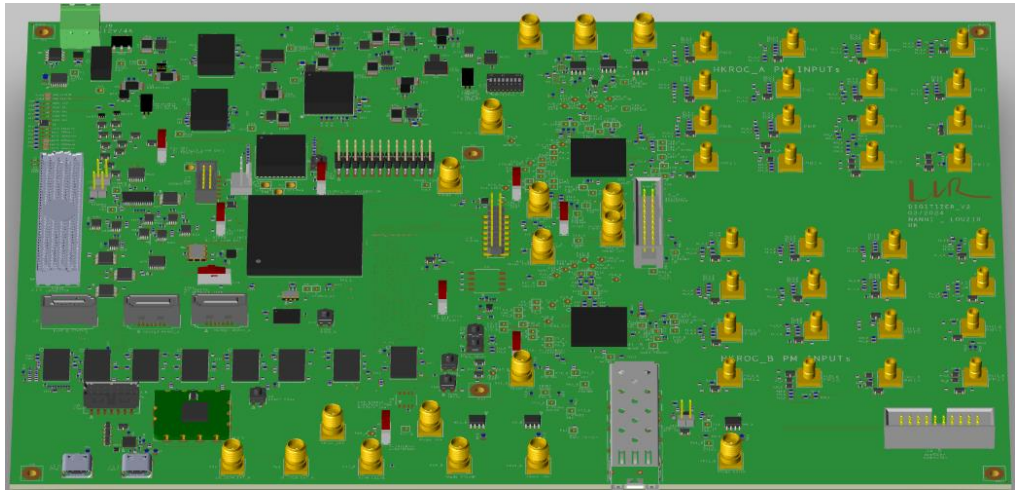
Board v1 – BGA (**HKROC1B**)
→ Channels in two layers



Conclusions and prospects

- The **HKROC1B**, designed to reduce crosstalk, has demonstrated good overall performance, fitting the requirements of neutrino experiments. **It has reduced 'diffuse crosstalk' by a factor of 2.**
- The **HKROC1C**, further optimized to reduce 'diffuse crosstalk,' has shown a reduction by a **factor of 1.6** compared to **HKROC1B** and **3.2** compared to **HKROC0**. **Crosstalk is now at the noise level, with only 2 mV remaining.**
- The **new test board**, designed to separate the channels into two layers, has completely **eliminated 'close crosstalk'** in the **HG** and **LG** channels and significantly **reduced** it in the **MG** channel.
- An **HKROC-based acquisition board** (21 x 29 cm) is currently in production. It includes two HKROCs and an FPGA for DAQ and charge reconstruction. This board is specifically designed **to further minimize 'close crosstalk**' and will be tested by the end of this year

Although it was designed for the Hyper-Kamiokande experiment,
it will not be used for this detector.
However, its **unique performance and flexibility** could make it useful for various experiments



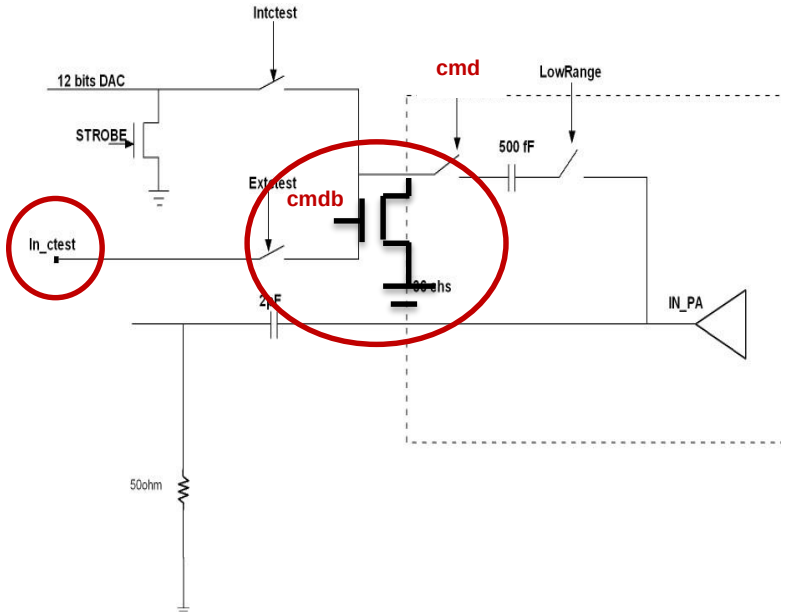
- Backup

Diffuse crosstalk

For **HKROC1C** (2022 version):

The "diffuse crosstalk" was observed in measurements, verified through simulations, and understood.

Three main sources of crosstalk were identified:



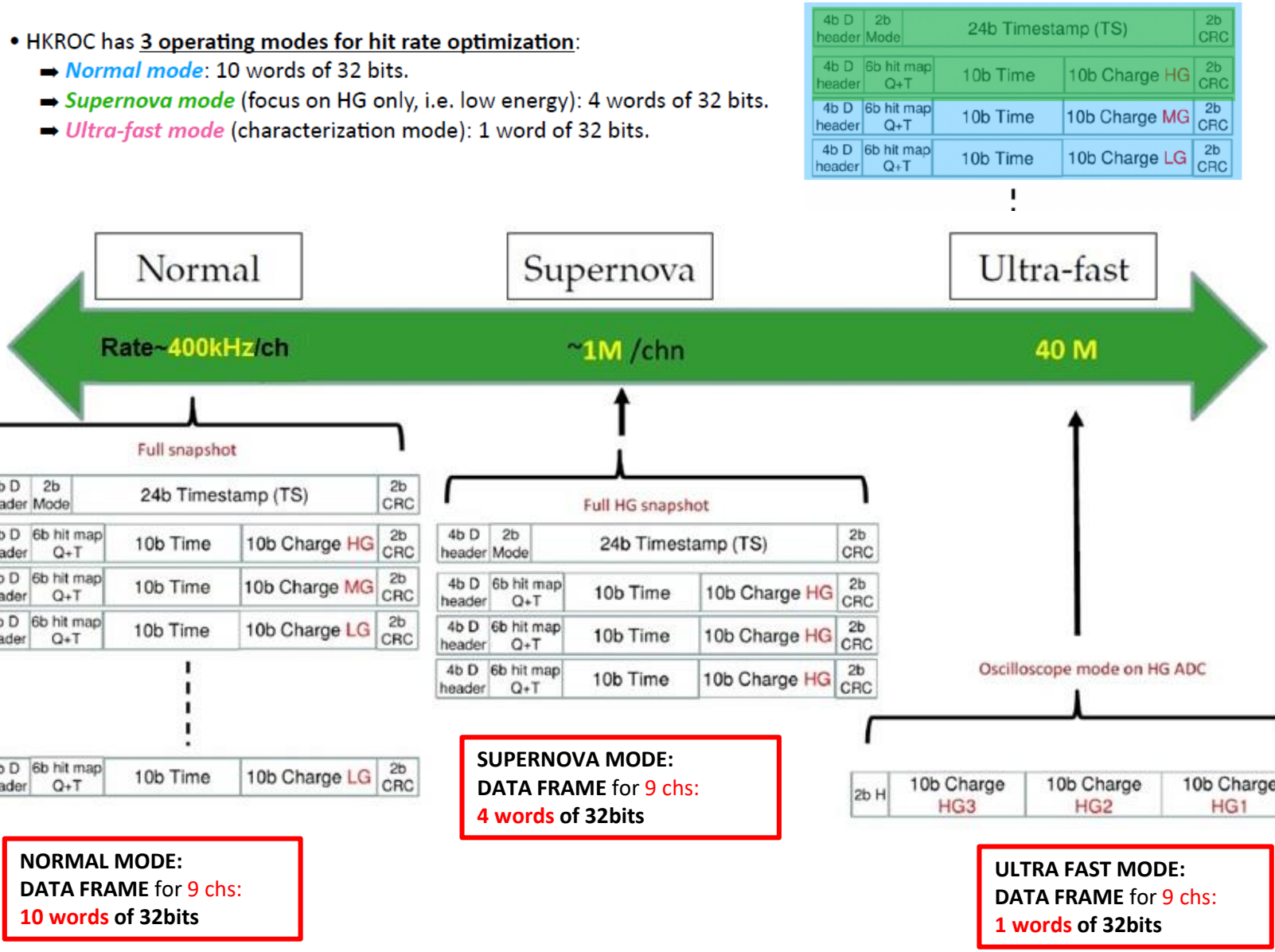
- PA bias → Cdecoupling + pins
- Shaper references → Cdecoupling + pins
- Ctest → New input calibration block structure

For **HKROC1C** (2023 version):

An additional PA bias was better decoupled in the layout and on the external board.

HKROC operating modes

- HKROC has **3 operating modes for hit rate optimization**:
  - ➡ *Normal mode*: 10 words of 32 bits.
  - ➡ *Supernova mode* (focus on HG only, i.e. low energy): 4 words of 32 bits.
  - ➡ *Ultra-fast mode* (characterization mode): 1 word of 32 bits.



NORMAL MODE:
DATA FRAME for 9 chs:
10 words of 32bits

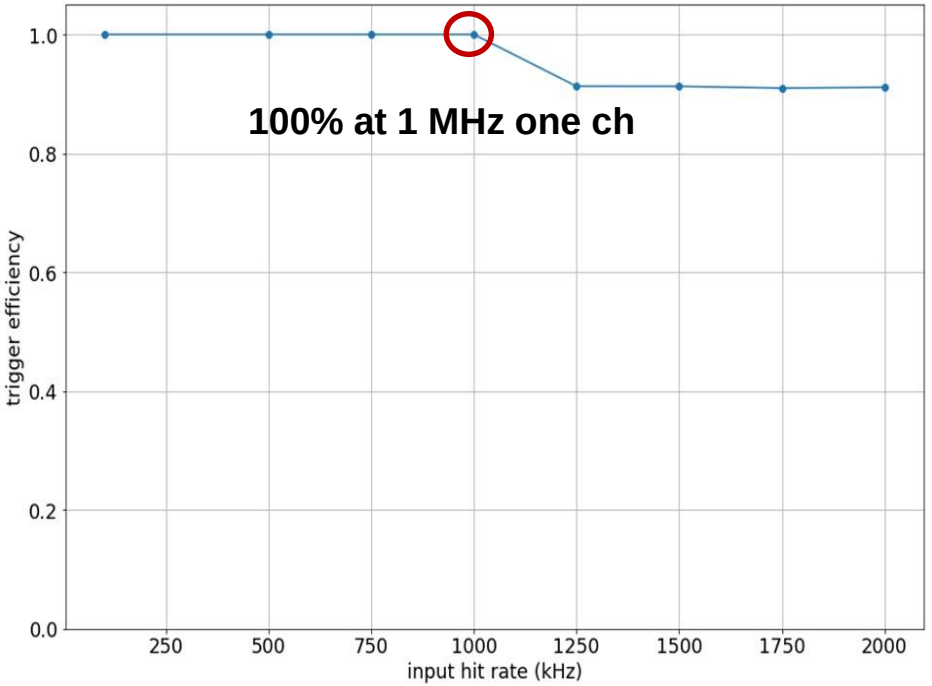
SUPERNOVA MODE:
DATA FRAME for 9 chs:
4 words of 32bits

ULTRA FAST MODE:
DATA FRAME for 9 chs:
1 words of 32bits

HKROC Trigger rate measurements

FAST hit rate (~ 1MHz) required for close Supernova signals (~ 1 p.e.)

Normal mode:

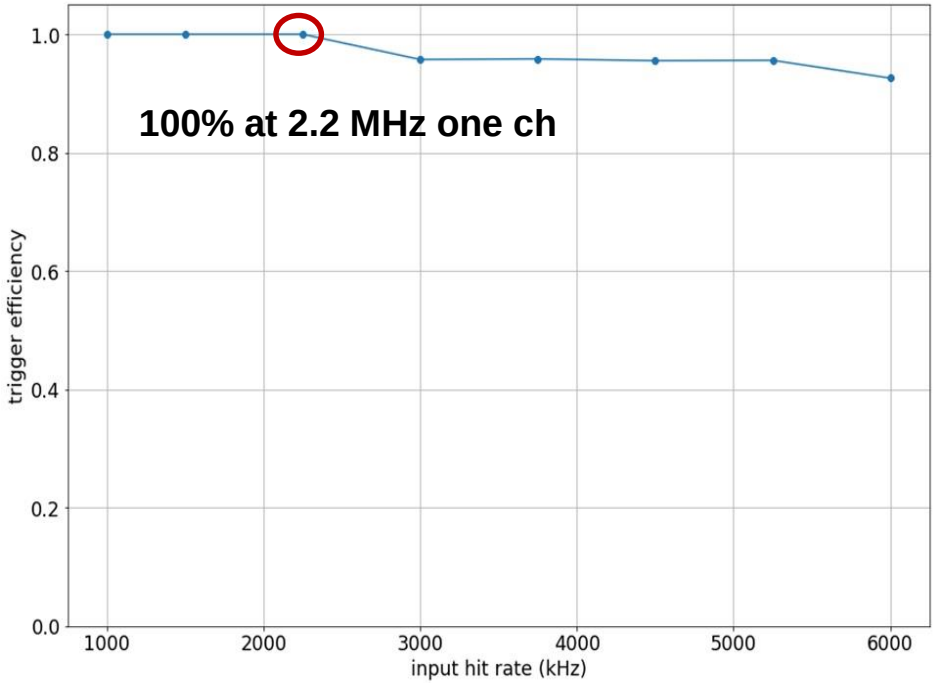


1 PMT channel →

3 HKROC channels tested in Normal Mode:

100% Trigger efficiency up to **415 kHz 3 chs**

Super Nova mode

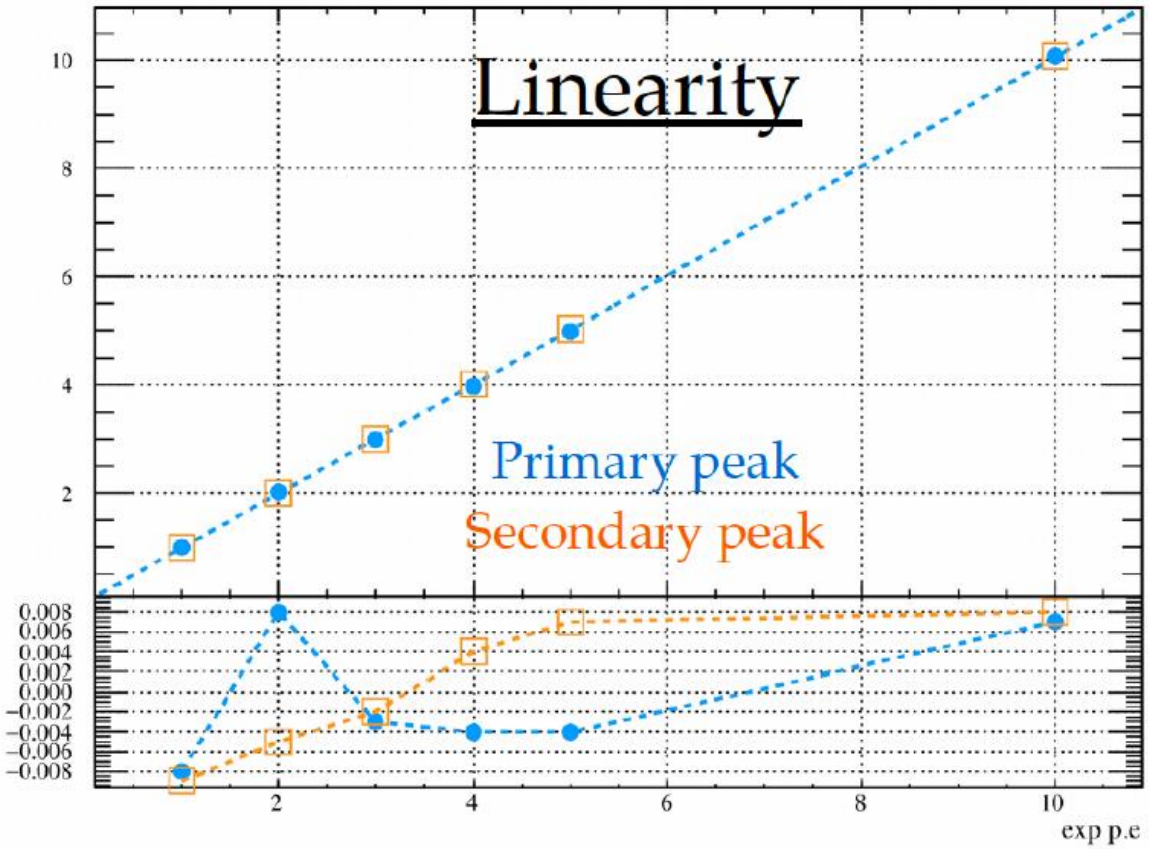


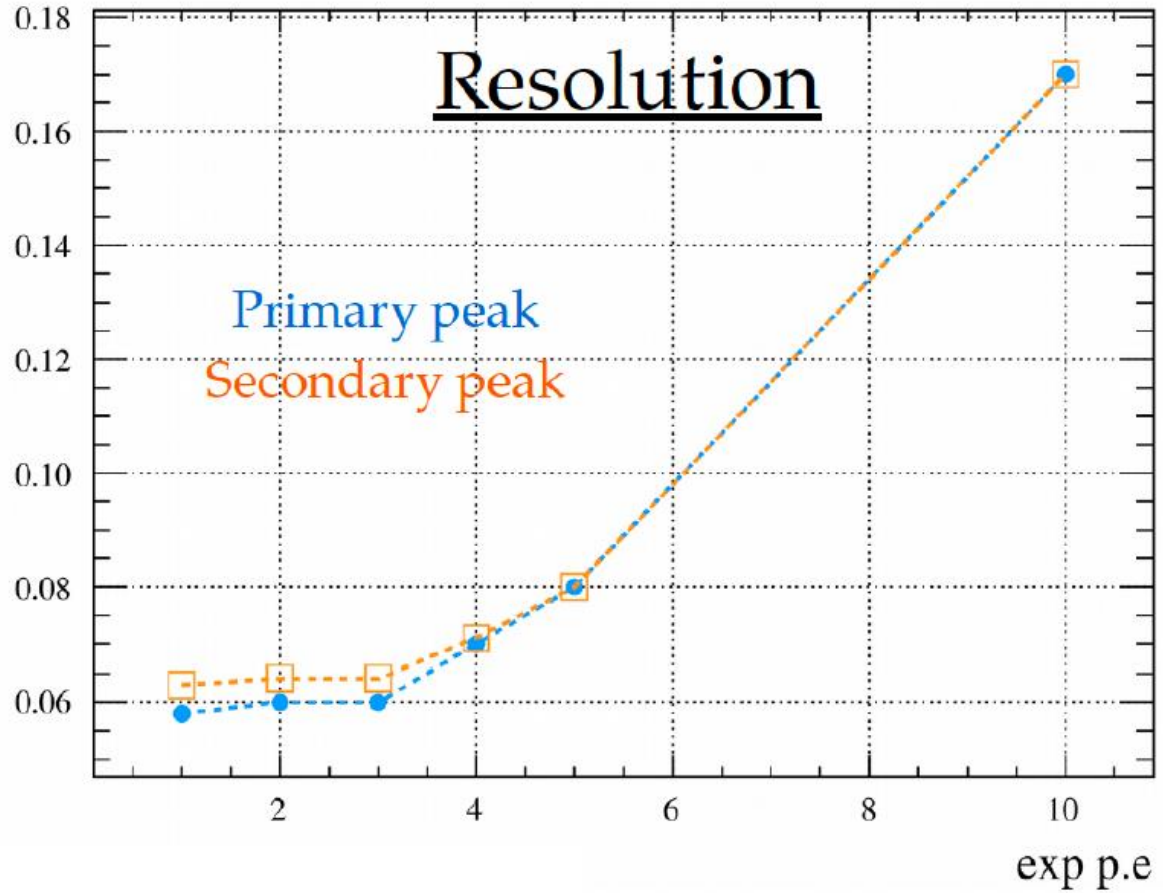
1 PMT channel →

3 HKROC channels tested in SuperNova Mode:

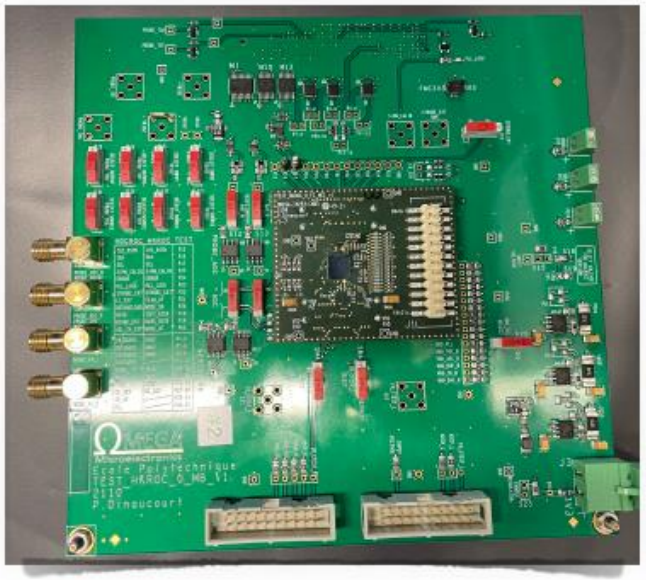
100% Trigger efficiency up to **950 kHz 3 chs**

The HKROC saturation naturally appears when the chip internal memory is full. The chip has one independent memory for each read-out link at 1.28 Gb/s, which gather 3 PMTs.

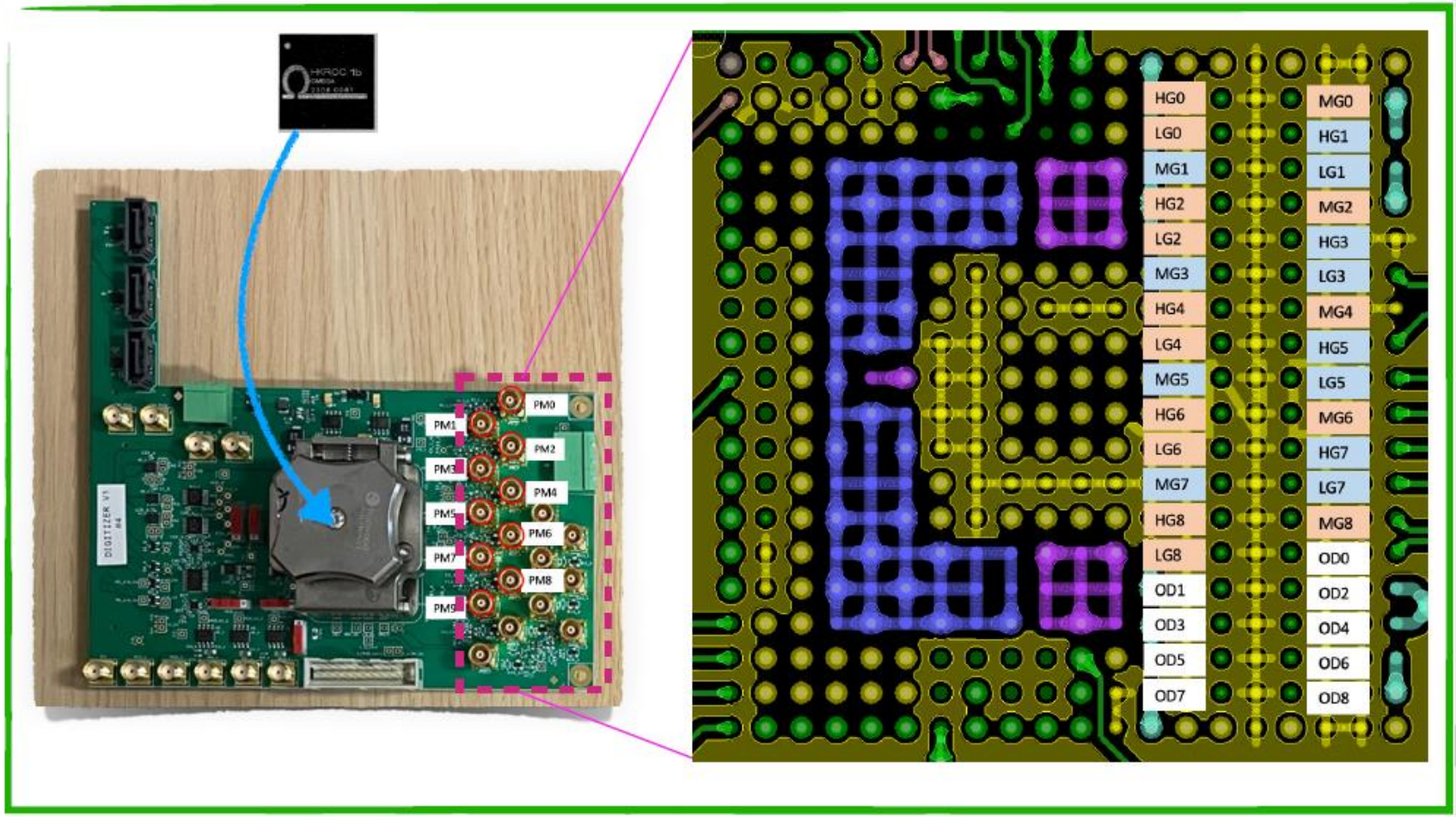

Linearity
Primary peak
Secondary peak
exp p.e


Resolution
Primary peak
Secondary peak
rms p.e
exp p.e

From single-layer to multi-layer front-end board

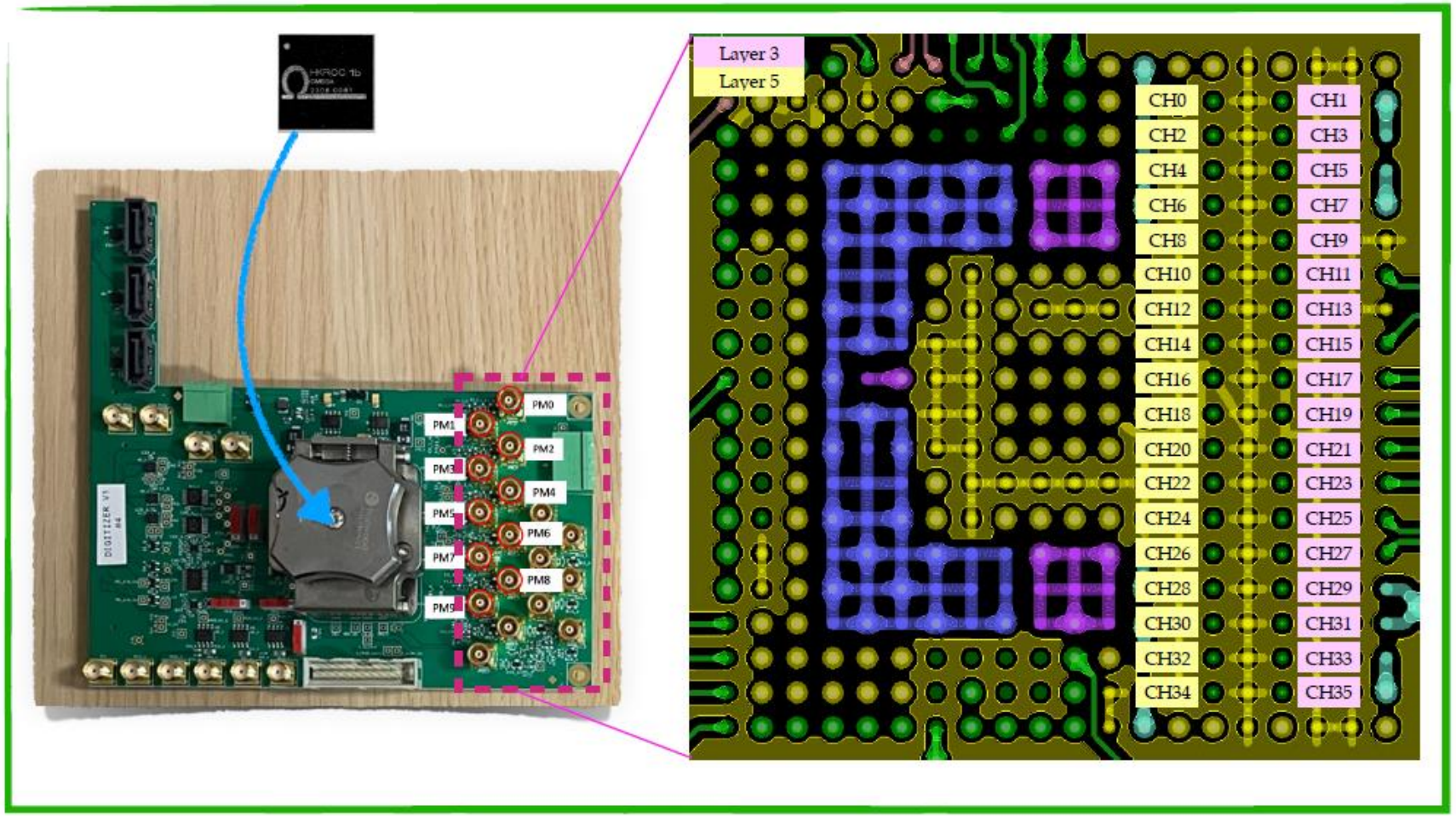


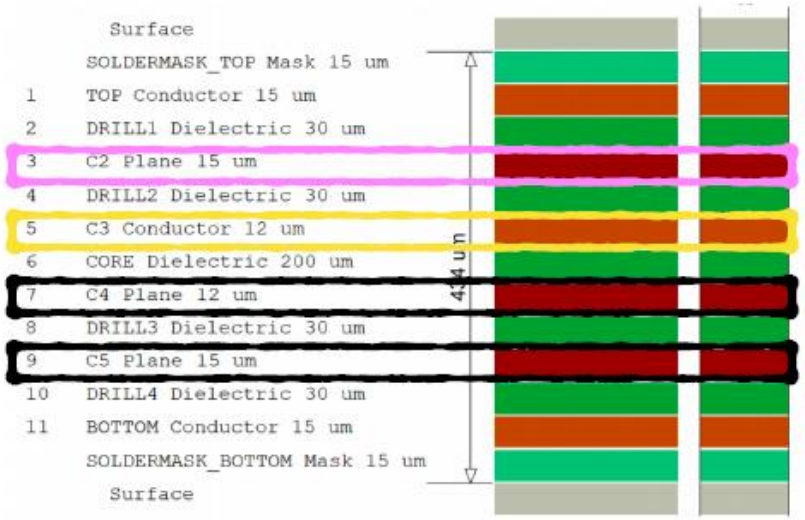
Mezzanine daughter board on mother board



BGA on mother board

From single-layer to multi-layer front-end board





BGA on mother board