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HKROC: an integrated readout chip designed to facilitate the readout of a large number of photomultiplier tubes for the next generation of neutrino experiments

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The HKROC is designed to read out the Photo Multiplier Tubes (PMTs) for next-generation neutrino experiments, which involve multi-ton detector with thousands of PMTs. It measures and digitizes the charge (up to 2500 pC) and Time-of-Arrival (ToA) (25 ps), transmitting this data to the back-end electronics. A second prototype of the HKROC, submitted in CMOS 130 nm node by summer 2022, aimed to improve performance in both noise and cross-talk, has undergone our complete testing procedure. In this presentation, we will show the results and performance of this improved ASIC

Summary (500 words)

Ongoing multi-ton neutrinos experiments, including projects like JUNO, HyperKamiokande, involve the integration of thousands of photomultiplier tubes (PMTs) during their design and construction phases. These experiments are increasingly expanding in size so this brought to a growing need for versatile integrated systems characterized by fast response, precise charge and time determination, and efficient data transmission. The HKROC, developed in this content, is a complex System on Chip (SoC) with analog and digital processing. It embeds 36 independent channels working in a trigger-less fashion.

To cope with the neutrinos experiment large dynamic range, each PMT is connected to three channels of the ASIC. The dynamic range is split in three parts corresponding to different channel gain configurations (High, Medium or Low gain). Thus, from a system point of view, one HKROC can be connected to 12 PMTs.

HKROC is designed with a trigger-less mechanism in order to detect the random physics events and it is based on an internal trigger generated comparing the input signal with a threshold level tunable channel by channel. Each channel of the chip is made of a low-noise input preamplifier followed by two paths: a fast path with a discriminator connected to 10-bit Time-to-Digital Converter (TDC from CEA IRFU group) for time measurement with 25 ps accuracy; a slow path with shapers connected to a 10-bit 40 MHz successive approximation Analog-to-Digital Converter (SAR ADC from AGH Krakow) for charge measurement.

The TDC is only activated when the input signal is higher than a defined threshold. When triggered, it opens an acquisition window where all input signals are digitized, stored and automatically read out. The TOA is directly given by the TDC. For the charge, the shaper output is continuously sampled by the ADC at 40 MHz. Only during the acquisition window, the digitized samples are stored inside a memory (with a maximum of 32 samples).

The latest iteration of the ASIC, submitted by the end of 2023, included schematic modifications aimed at mitigating crosstalk issues across channels. Crosstalk had previously limited ASIC performance, affecting the detection of minimum input signals and linearity. This updated ASIC version is expected to significantly improve performance in terms of crosstalk, thereby leading to overall improvements. The presentation will cover the ASIC architecture, performance improvements, and the measurements with a PMT

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