



ECON-T and ECON-D: Endcap Concentrator ASICs for the CMS HGCAL

Jim Hoff on behalf of the ECON team and the CMS collaboration

Topical Workshop on Electronics for Particle Physics

01 October 2024

In partnership with:



ECON Team



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Duje Coko



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Fermilab Team: Jim Hoff, Alpana Shenai, Chinar Syal, Neha Kharwadkar and Cristian Gingu (missing: Jim Hirschauer, Danny Noonan, Xiaoran Wang, Davide Braga and Paul Rubinov)



Special Thanks and Acknowledgement

- The lpGBT team
 - eRX: Di Guo (SMU), Datao Gong (SMU), Jingbo Ye (SMU), Paulo Moreira (CERN)
 - ePortRxGroup (phaseAligner, ePortRx): Dongxu Yang (SMU), Szymon Kulis (CERN), Datao Gong (SMU), Jingbo Ye (SMU), Paulo Moreira (CERN)
 - ljCDR (LJCDR and ser640Mto10G24): Jeffrey Prinzie (KUL), Paul Jozef Leroux (KUL), Rui De Oliveira Francisco (CERN), Pedro Leitao (CERN), Szymon Kulis (CERN), Paulo Moreira (CERN)
 - eTX: Paul Jozef Leroux (KUL), Bram Feas (KUL), Paulo Moreira (CERN)
- The hls4ml team (ECON-T Autoencoder)
- Special thanks to the following for their critical input to ECON design :
 - Frederick Dulucq, Mowafak El Berni (HGCROC digital behavior)
 - Alesandro Caratelli (I2C interface IP)
 - Matt Noy (HGCAL Fast Command Receiver IP)

Introduction – High-Level View

The CMS HGICAL is a 47-layer sampling calorimeter that features fine readout segmentation, and which replaces the existing endcap calorimeter detectors for the High Luminosity phase of the LHC (HL-LHC).

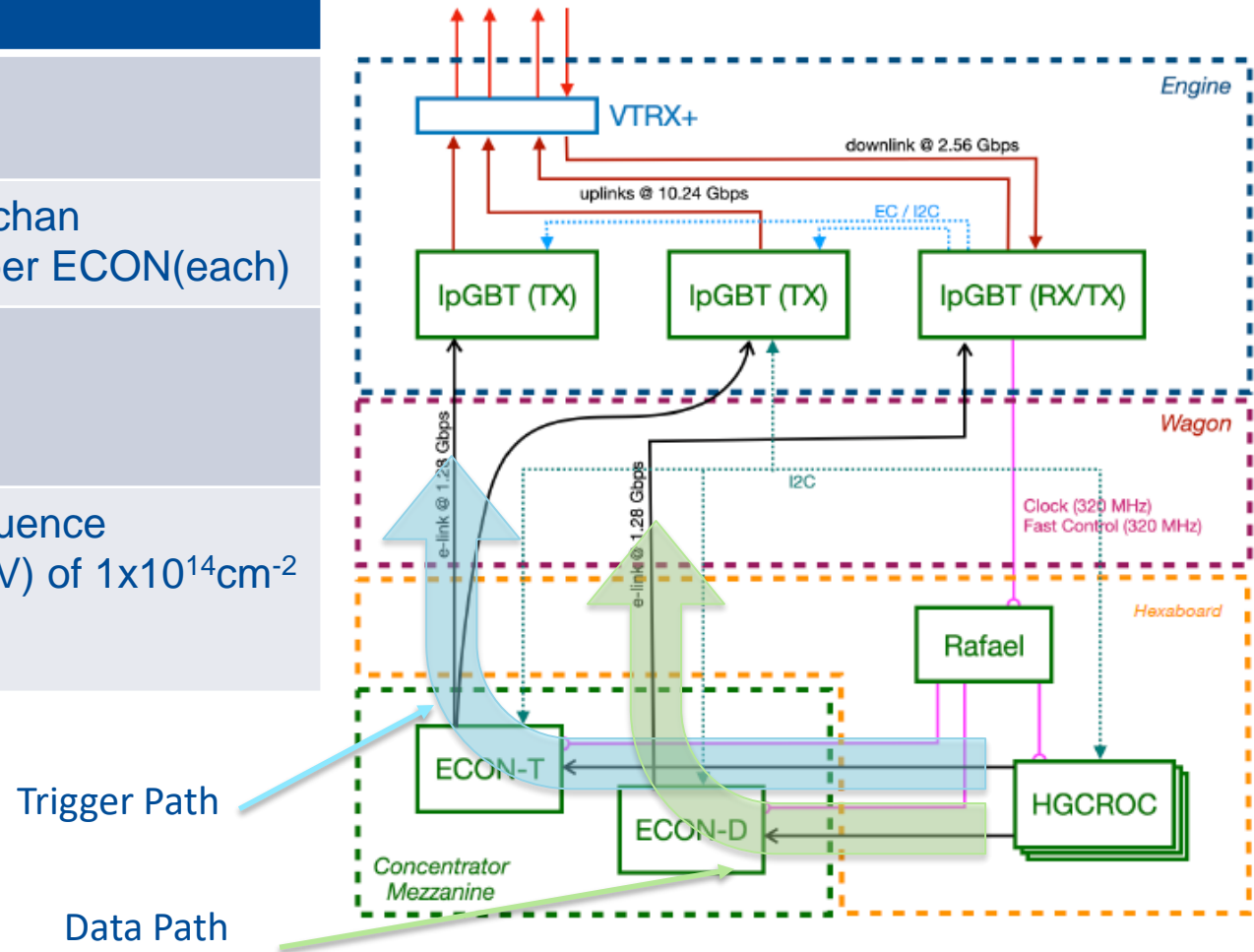
6 million channels	600 m² of silicon	0.5-1.0 cm² sensor pads	Digitized by HGCROC ASICs
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More than 5 Pb/s of raw digital data must be processed and compressed/selected along two independent data paths.

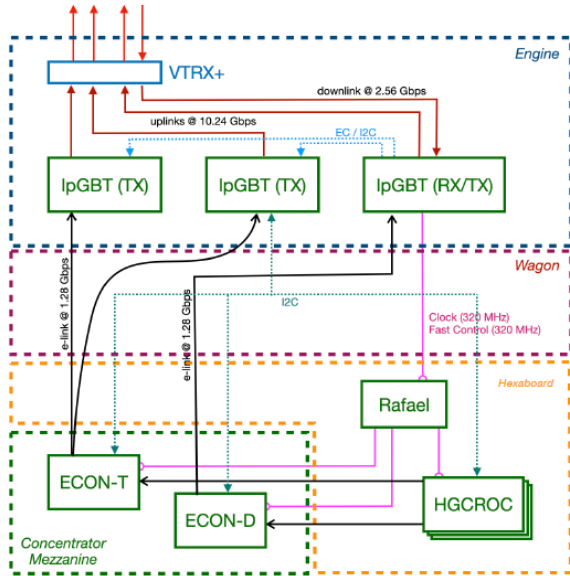
	Trigger Path	Data Path
	ECON-T	ECON-D
Content	Limited Data for L1 Trigger	Full Data Frame for Data Acquisition
Rate	40MHz Bunch Crossing Rate	750kHz L1 Accept Rate

Introduction – High-Level View (cont'd)

Parameter	Specification
ECON-T Latency	$\leq 0.4\mu\text{s}$
Power Consumption	$\leq 2.5\text{mW}/\text{chan}$ 500mW per ECON(each)
Total Ionization Dose	220 Mrad
SEE tolerance	Hadron fluence ($E > 20\text{MeV}$) of $1 \times 10^{14}\text{cm}^{-2}$



Specifications and the Chip Architecture



Consequently, by **design** both chips:

- Use CERN IpGBT IP
 - Receive a user programmable number of 1.28GHz serial input streams from HGCROC front end chips (1-12 IpGBT eRX links for each chip).
 - Produce a user programmable number of 1.28GHz serial output streams to be sent to IpGBT chips for transmission off-detector (1-6 IpGBT eTX links for ECON-D and 1-13 for ECON-T).
 - PLL modified by Xiaoran Wang for 9-layer metal process
- Other external IP
 - I2C Secondary
 - Fast Command
- Common, ECON-specific IP
 - word/frame alignment of input data streams
 - Output data serializers
 - Clocks and resets (based strongly on IpGBT IP)

By **specification** both chips:

- Receive 320MHz system clock
- Receive a common fast command stream
- Beam synchronous clock is recovered from the fast command stream
- Require programmability via slow control
- Transmit a serialized data frame to the IpGBTs for off-detector transmission.

Other Project-wide decisions

- **SEU tolerance**

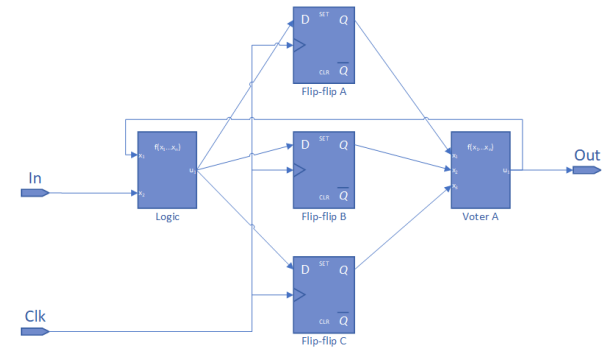
1. Tolerance by Design
2. Graceful Failure
3. Full TMR

- **Minimize differences**
to

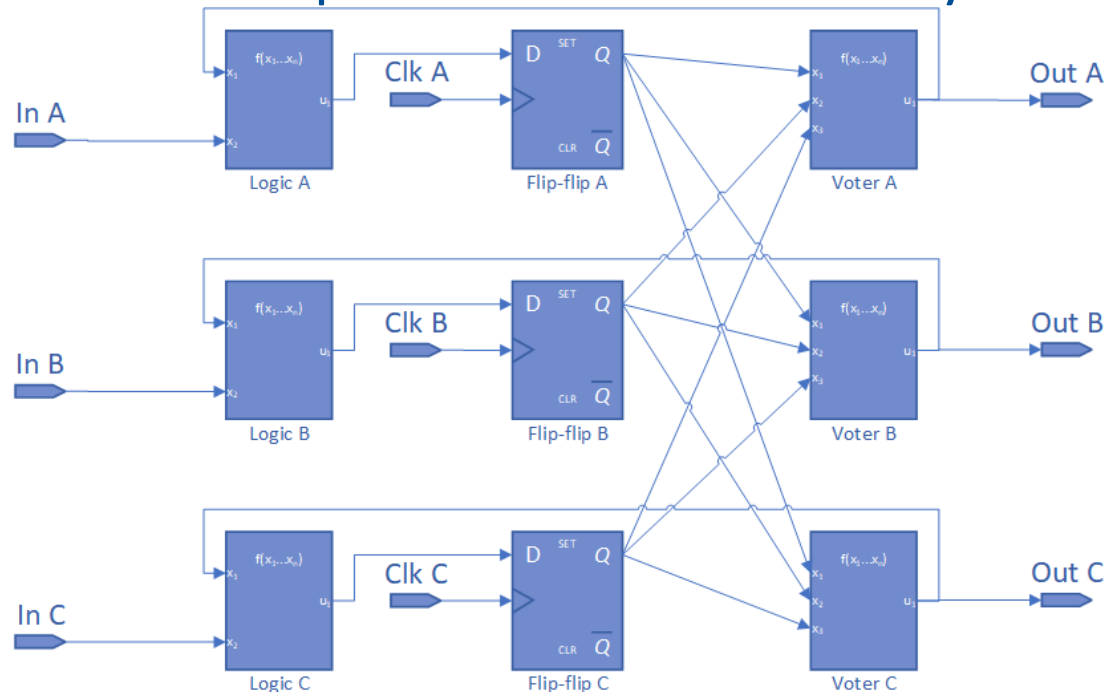
- **Maximize design reuse**

1. Impacts not only RTL, but also PNR and Verification.
2. Schedule submissions; feedback gleaned from one submission could be applied to the next.
3. Was not practical to make ECON-T and ECON-D the same chip with different mode settings

Simple Triple Modular Redundancy

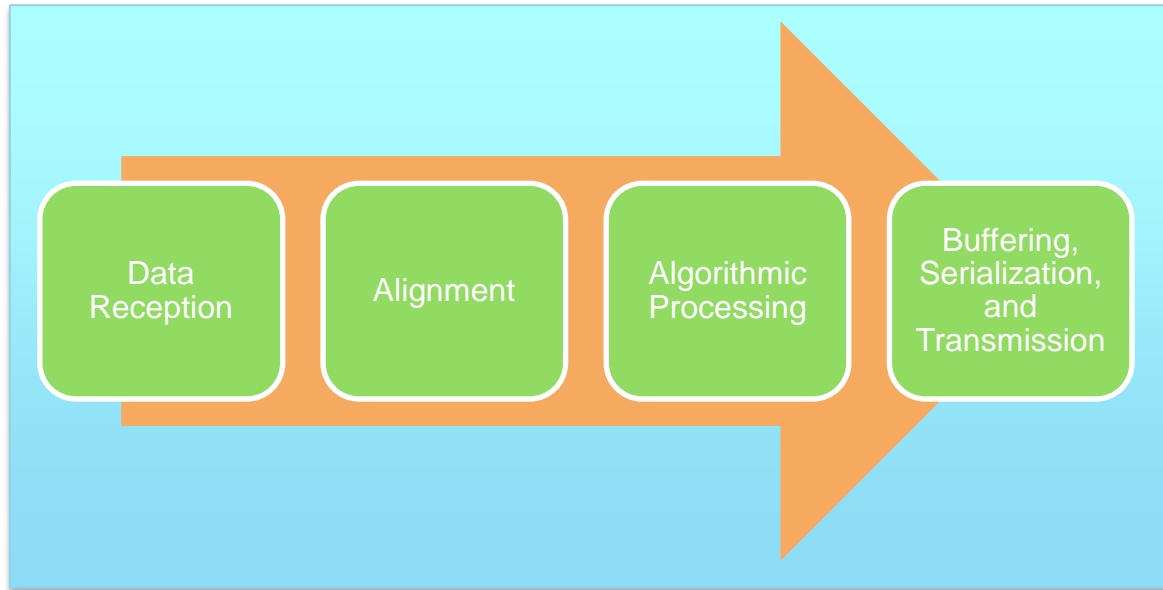


Full Triple Modular Redundancy



Chosen Architectures

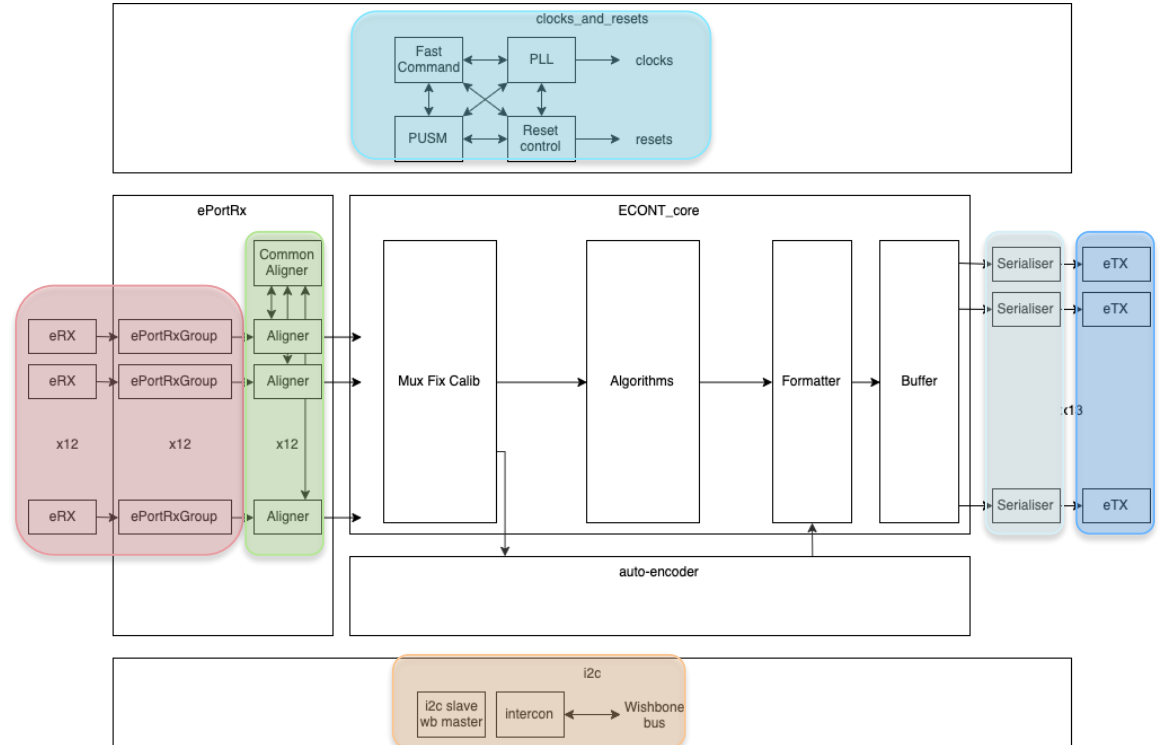
The resultant chip-wide data-flow architecture for both chips is:



- **ECON-T vs ECON-D uniqueness is confined to Algorithmic processing.**
- **That data frame processing is **RADICALLY** different between ECON-T and ECON-D.**
 - It was deemed impractical to make a single chip to serve both paths

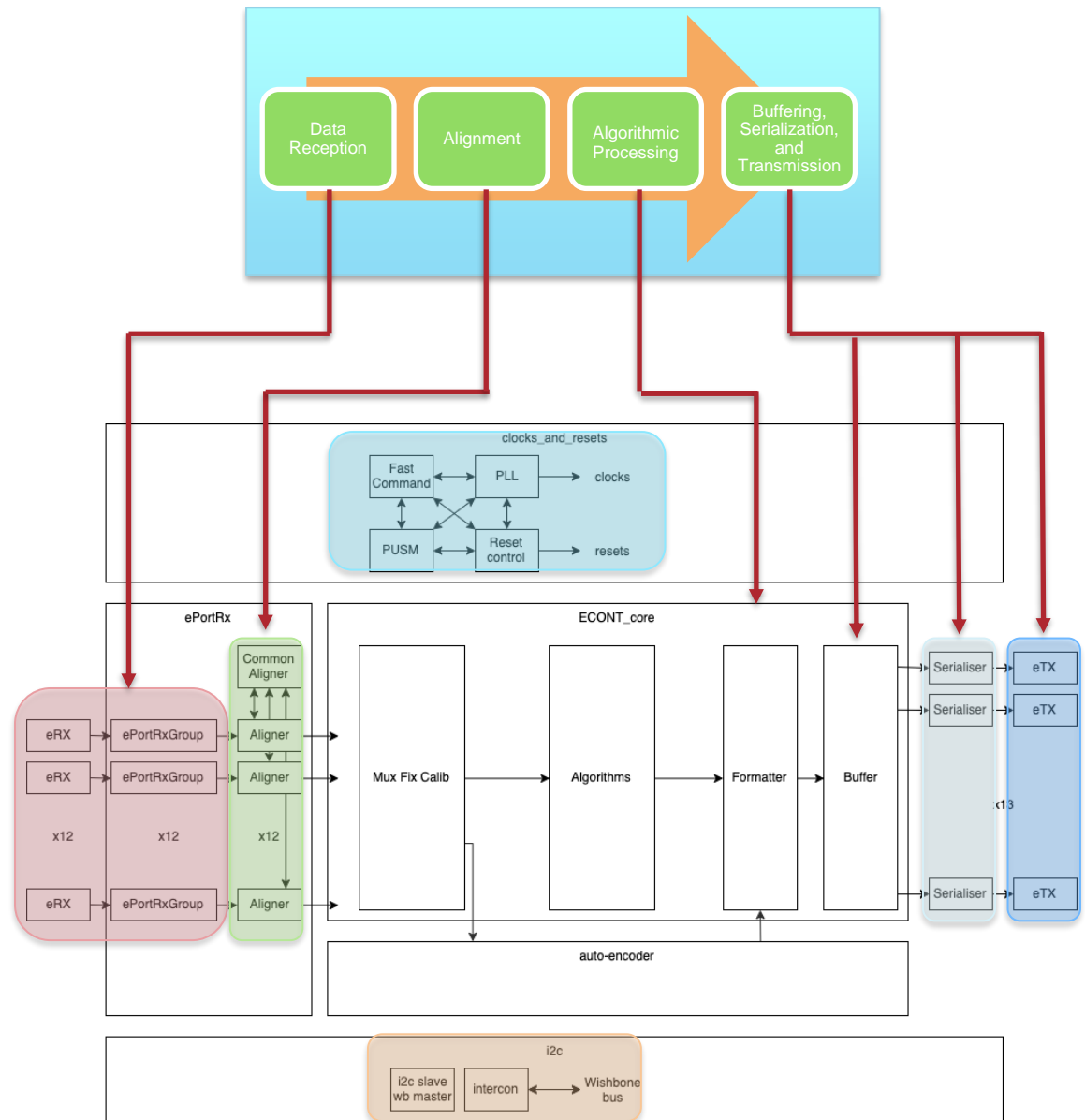
ECON-T

- The highlighted sections are IP held in common between ECON-D and ECON-T.
- Input Frame: 1 32-bit word per active HGCROC per 40MHz event clock. Each new word is a new, independent event.
- Idle words only during reset and alignment phases.



ECON-T

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- Input Frame: 1 32-bit word per active HGCROC per 40MHz event clock. Each new word is a new, independent event.
- Idle words only during reset and alignment phases.



ECON-T

I. Mux-Fix-Calib

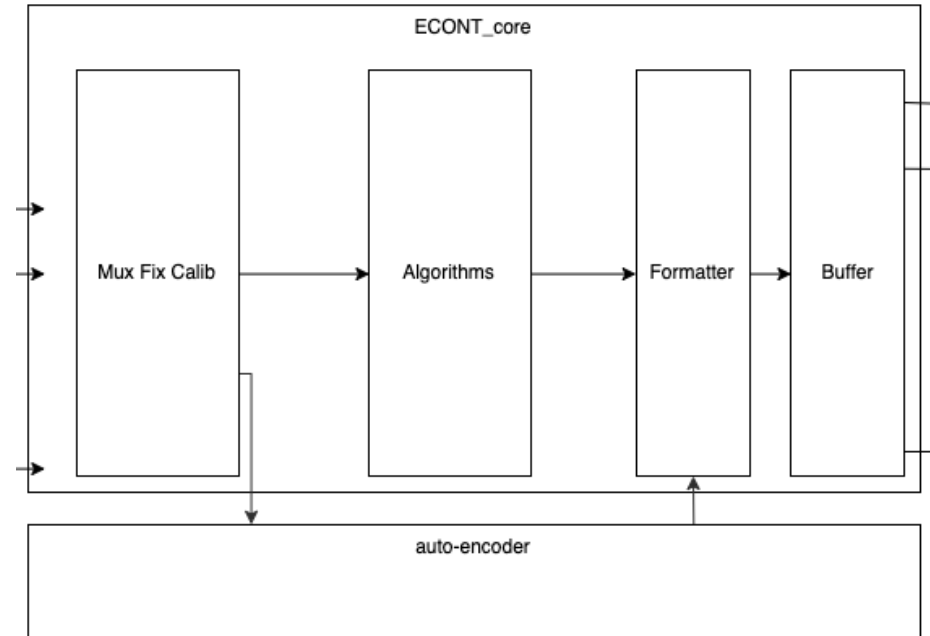
- I. A switch box for logically shuffling HGCROC inputs;
- II. A floating-point to fixed-point converter
- III. Calibration multiplication by a user-defined constant

II. Algorithms

- I. Threshold Sum (TS)
- II. Super Trigger Cell (STC)
- III. Best Choice (BC)
- IV. Repeater (R)
- V. Auto-encoder (AE) – ML-based compression algorithm

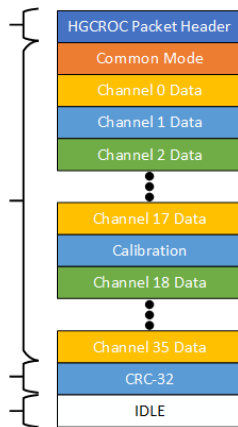
III. Formatter-Buffer

- I. Formatter acts as a demultiplexer selecting algorithm outputs
- II. STC, BC, R and AE are all fixed length algorithms. Buffer management is a simple distribution of data to serializers and outputs
- III. TS is a variable length algorithm. Output buffer provides a well-defined maximum readout latency, and this number is programmable

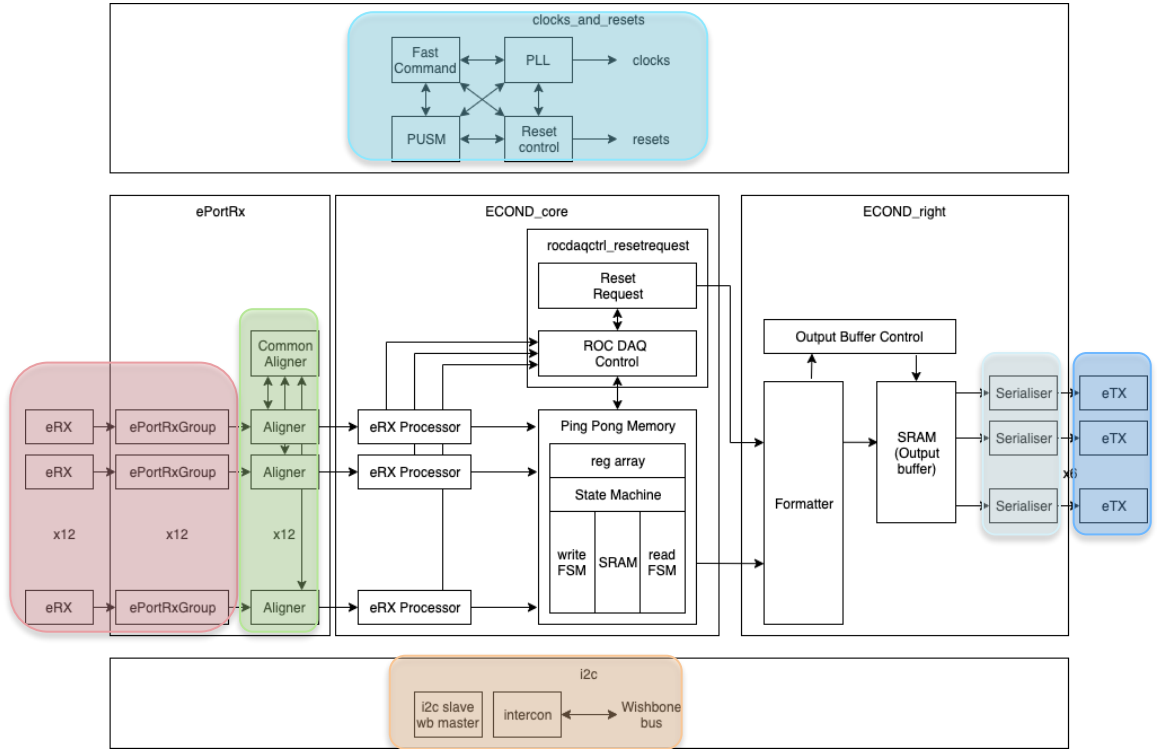


ECON-D

- The highlighted sections are IP held in common between ECON-D and ECON-T.
- Each active HGCROC outputs either an Idle Word or a packet component every 40MHz.
- Idle Words are functionally and bit-to-bit identical to those used by ECON-T
- Packets:

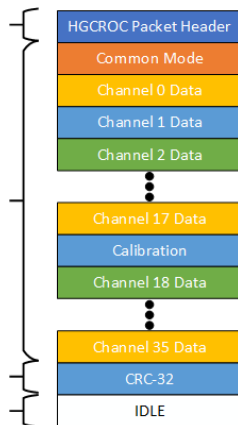


System Enforced
Coincidence

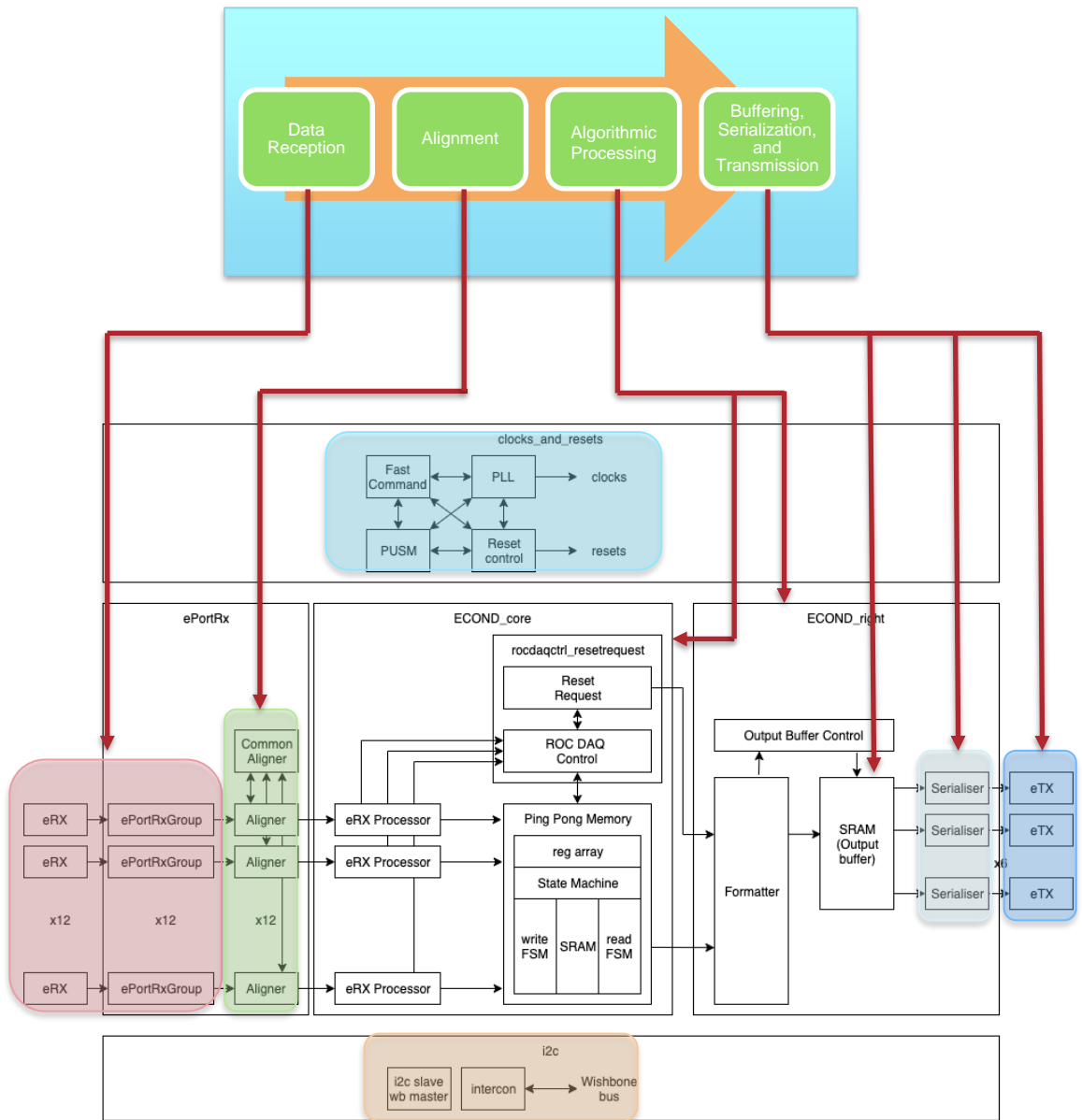


ECON-D

- The highlighted sections are IP held in common between ECON-D and ECON-T.
- Each active HGCROC outputs either an Idle Word or the same packet component every 40MHz.
- Idle Words are functionally and bit-to-bit identical to those used by ECON-T
- Packets:

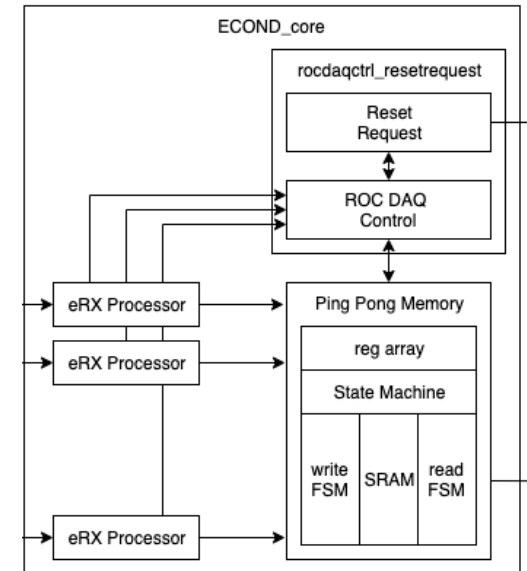


System Enforced
Coincidence



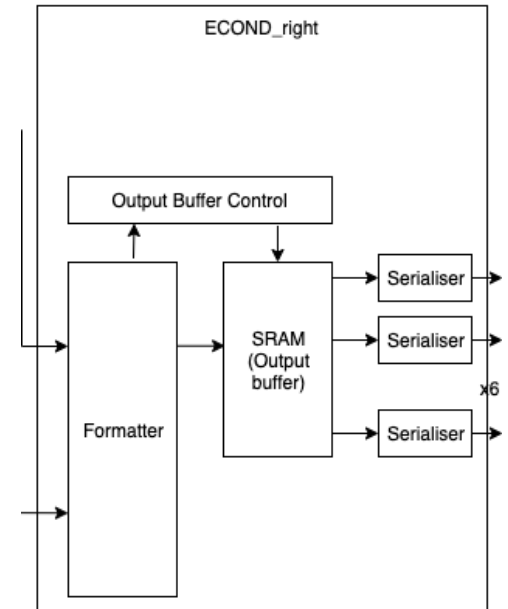
ECON-D Core – HGCROC Packet Capture

- All actions occur on the 40MHz clock in response to HGCROC outputs
- **Purpose:**
 1. Extract all information from HGCROC packets (including errors)
 2. Present this information simultaneously to ECON-D Left
- **ROC DAQ Control:**
 1. Single state machine consequence of system-enforced coincidence
 2. Diagnostics (e.g Header count, Idle count, Invalid state)
 3. Simple Mode vs. Predictive Mode
 4. **Packet Veto** – self-regulation through the elimination of packets depending on certain user-defined conditions.
- **eRX Processors:**
 1. Independent for each component of the HGCROC packet (Header, Common Mode, Channel Data, CRC).
 2. Zero suppression and algorithmic processing handled here.
- **Ping-Pong Memory:**
 1. Enables the information transfer to ECON-D Left.
 2. Enables simultaneous HGCROC packet reception and ECON packet output
 3. Data arrives in time order; read out in channel order
- **Reset Request :**
 1. Extensive, event-based self-monitoring system
 2. Determines if internal conditions suggest a reset is necessary.
 3. Maintains packet-by-packet history of events.



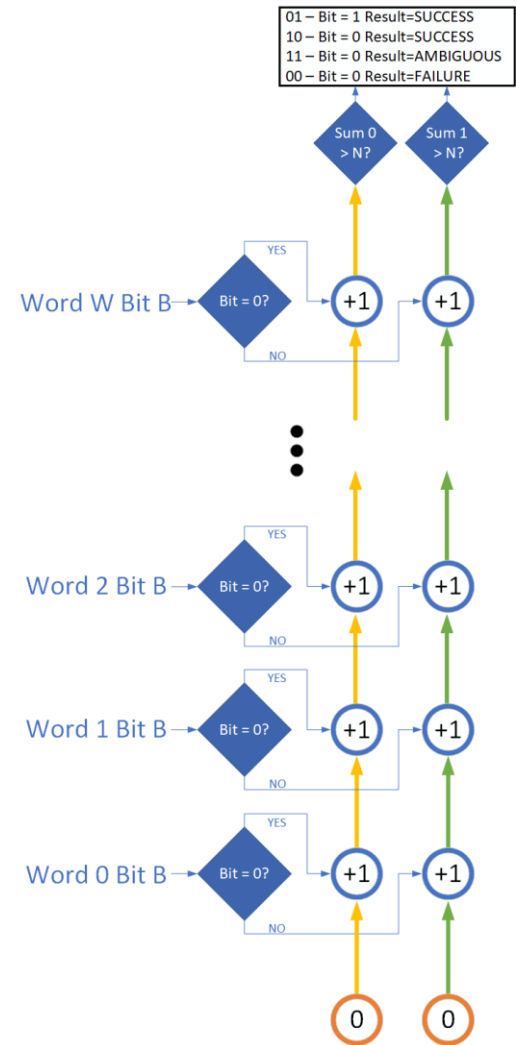
ECON-D Right – Outbound Packet Assembly

- All actions occur on the 40MHz clock in response to ECON's own buffer and output packets.
- **Purpose:**
 1. Assemble outbound event packet
 2. Buffer the event packets
 3. Cycle 32-bit output words to next available serializer
- **Formatter**
 1. Fills out header data as available
 2. Assembles incoming channel data in 384-bit vectors
 3. On Packet Veto or bad ECOND_core state, flushes Ping-pong memory and aborts assembly
- **SRAM Output buffer**
 1. Daisy chains incoming data, simultaneously for all HGCROC channels
 2. On abort resets write pointer. The next event packet will be written as if nothing had happened.

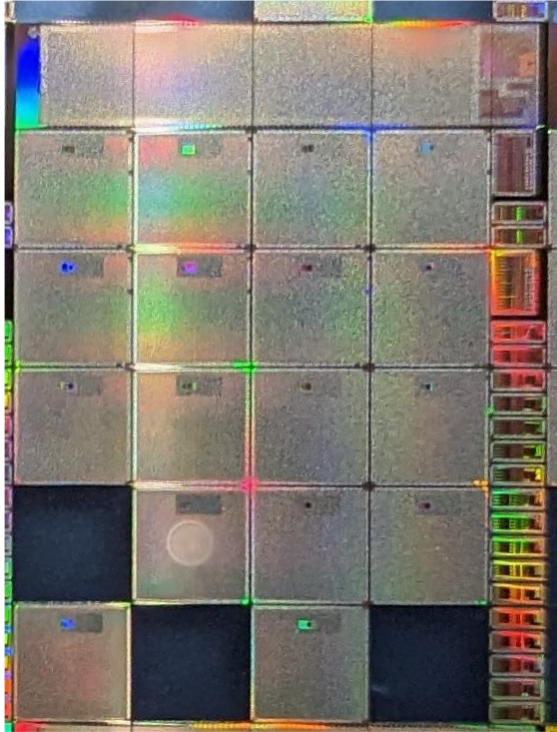


Radiation Tolerance by Design

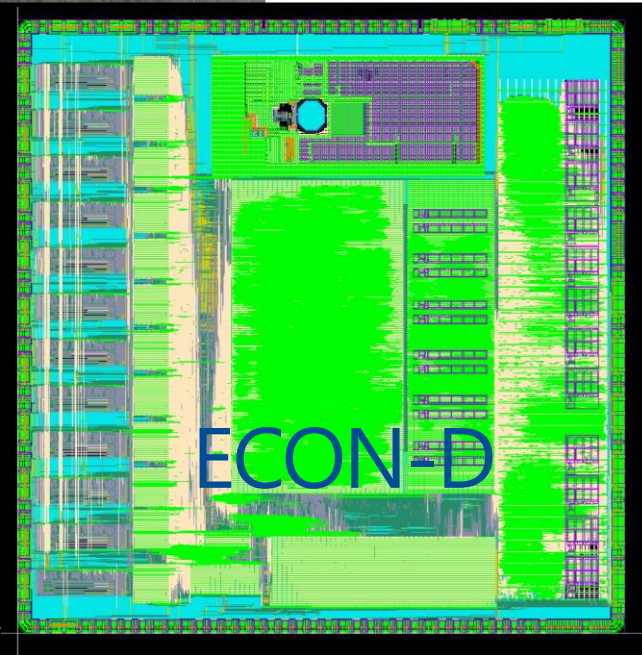
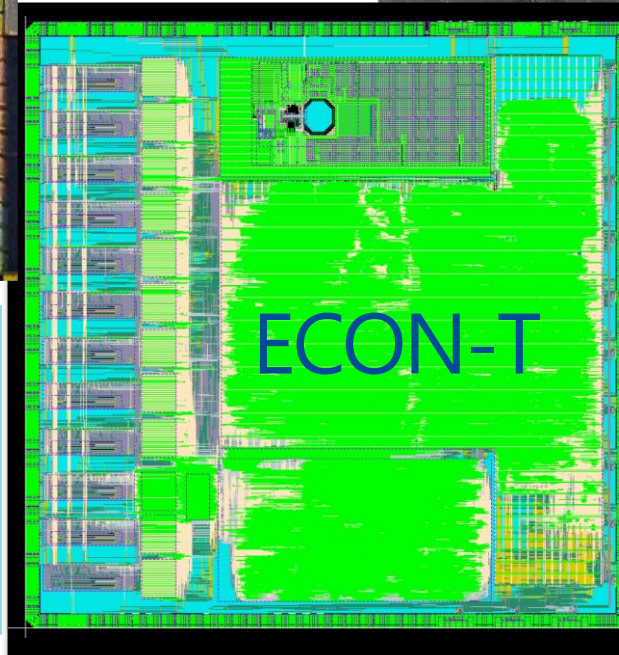
- **Full Triple-Modular-Redundancy everywhere (except external IP)**
- **Exploit implicit redundancy in the system**
 - Packet Header recognition – how many HGCROCs call this a header?
 - Header Field Extraction – Vertical Reconstruction (a form of modular redundancy); recognition of perfect, good, failed and ambiguous reconstructions
 - Reconstructed Header Fields are checked against those of individual channels. Repeated mismatches in a given channel could indicate a link that needs resetting.
- **State Machine “Design Rules”**
 1. All states valid within the phase space of the state machines.
 2. Non-functional states all have a path back to home (i.e. they fail gracefully and recover on their own).
 3. Non-functional states flag errors within the system that can be checked by the back end.
- **Erroneously formed IDLE words are used to check for potentially missed packets.**
- **Reset Requests include repeated failures in reconstruction and matching.**
- **Hamming codes used for critical data in SRAMs**



ECON Production



- Plan :**
- 20-wafer engineering run
 - Dec-2023 6-wafer lot (N61H30.00) - **complete**
 - Jan-2024 8-wafer lot (N61H52.00) - **complete**
 - 6 wafers held at contact - **still held**
 - 25-wafer production run - **not started**



	# / wafer	45-wafer total	Needed	Spare
ECON-D	918	40392	27k	50%
ECON-T	752	33088	20k	65%

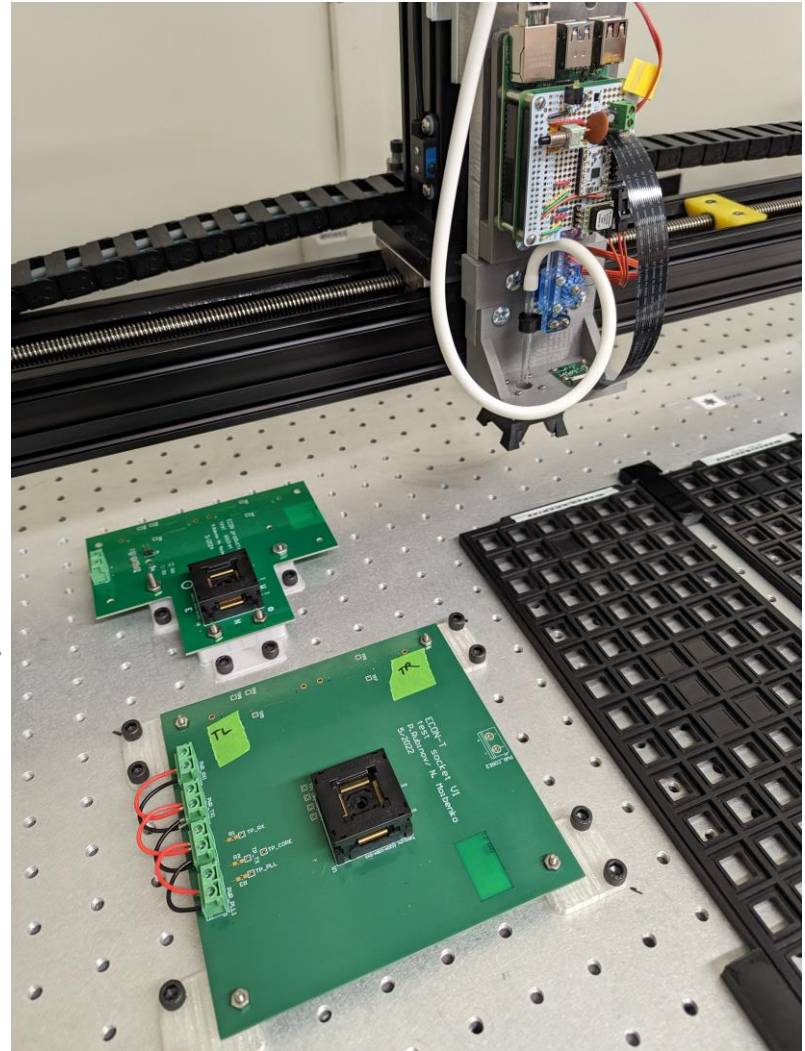
ECON Bench and QC testing

Two test programs:

- **Full functionality tests :**
 - Full coverage of all operating modes, configurations, etc.
 - Based on digital verification used for ECON design
 - Requires ~hours for full coverage
- **QC tests :** full testing of all essential blocks and primary operating modes/configs
 - ~3 minutes / chip
 - Automated / robotic ASIC tester

Status of ECON-D and ECON-T tests (in parallel):

- **Fully characterized** : PLL, eRx, eTx, bit alignment, power consumption, voltage range
- **Fully tested** : primary modes of all digital algorithms
- **Fully tested** : full coverage of all operational modes + configs
- **Tested** : 465 ECON-D + 360 ECON-T
 - Combined yield ~ 97%



SEE test summary

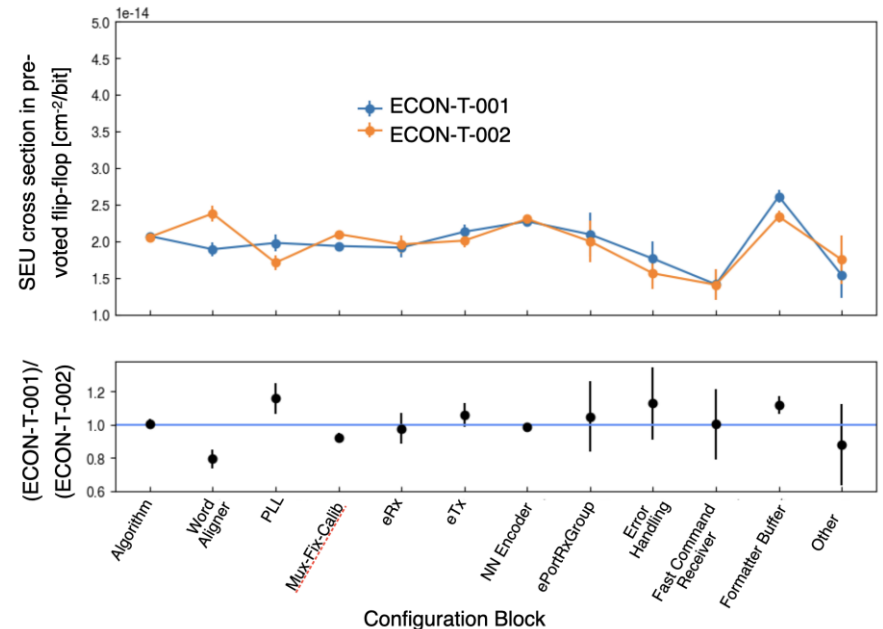
- Completed 3 test campaigns at a Proton Cyclotron for prototype and engineering run ECONs
- Latest test for eng run ECON-T and ECON-D:
- 217 MeV protons, Flux = $1e9-2e10$ /cm²/s
- Fluence = $3.8e13/cm^2$ per chip
- Tested 2 ECON-D + 1 ECON-T for total fluence = $1.1e14/cm^2$ = 1 x HL-LHC equivalent

Computed lower limit on period between SEE's requiring ECON reset for entire detector (47k ECONs) from combination of all 3 test campaigns:

- Reset period > 27 minutes
- Assumes SEE sensitivity is common to ECON-T and ECON-D
- Entire HGICAL : all 47k ECON-D + ECON-T
- Combination total fluence of all 3 SEE tests = $4.4e14$ cm⁻² = 4 x HL-LHC equivalent
- 95% CL Limit (one-sided)

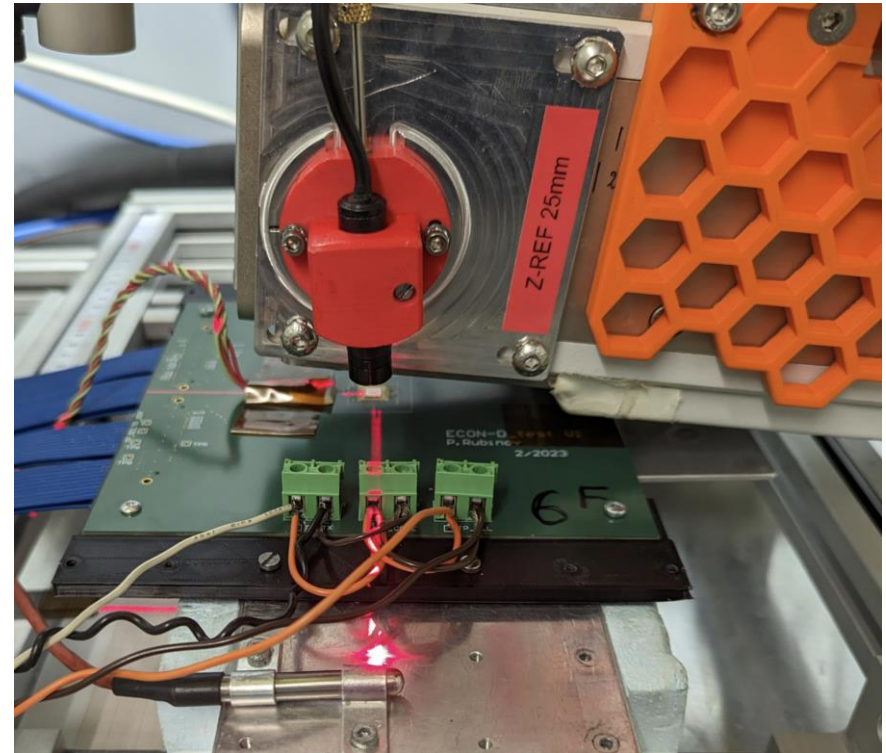
Results:

- Ran with 750 kHz L1A rate (now routine)
- Observed **zero errors requiring reset**
- Observed **zero configuration errors**
- Measured cross section for pre-voted bit flip **consistent with previous runs.**
- Analysis in progress for independent SEU cross section measurements in ePortRxGroup, Ping-pong SRAM, Output buffer, Serializer



TID test summary

- ECON tested for TID tolerance with CERN ObeliX x-ray machine
- Dose rate = 9 Mrad/hr; Temp = -20°C; VDD = 1.08-1.32V
- HGICAL requirement = 220 Mrad (no safety factor)
- Test campaigns:
 - Sep 2022 : 2 ECON-T-P1 (300 and 670 Mrad)
 - Aug 2023 : 3 ECON-D-P1 (3 x 660 Mrad)
 - Jul 2024 :
 - 1 ECON-T (660 Mrad)
 - 5 ECON-D (15, 170, 350, 600, 660 Mrad)



Preliminary results :

- Robust performance at (nominal) 1.2V for ECON-T-P1, ECON-D-P1, ECON-T
 - Observed expected TID-dependence on PLL cap bank setting, eRx phase window, etc.
- Observed non-zero bit errors on eTx at 1.08V and TID > ~450 Mrad
- **In progress:** detailed analysis of ECON-D SRAM performance as function of temperature, operating voltage, and TID to quantify final requirements.

Results and Conclusions

The ECON has landed

First look at ECON-T-Prod and
ECON-D-Prod from Engineering Run

Danny Noonan for ECON design and testing team
June 4, 2024
HGCAL Electronics Meeting



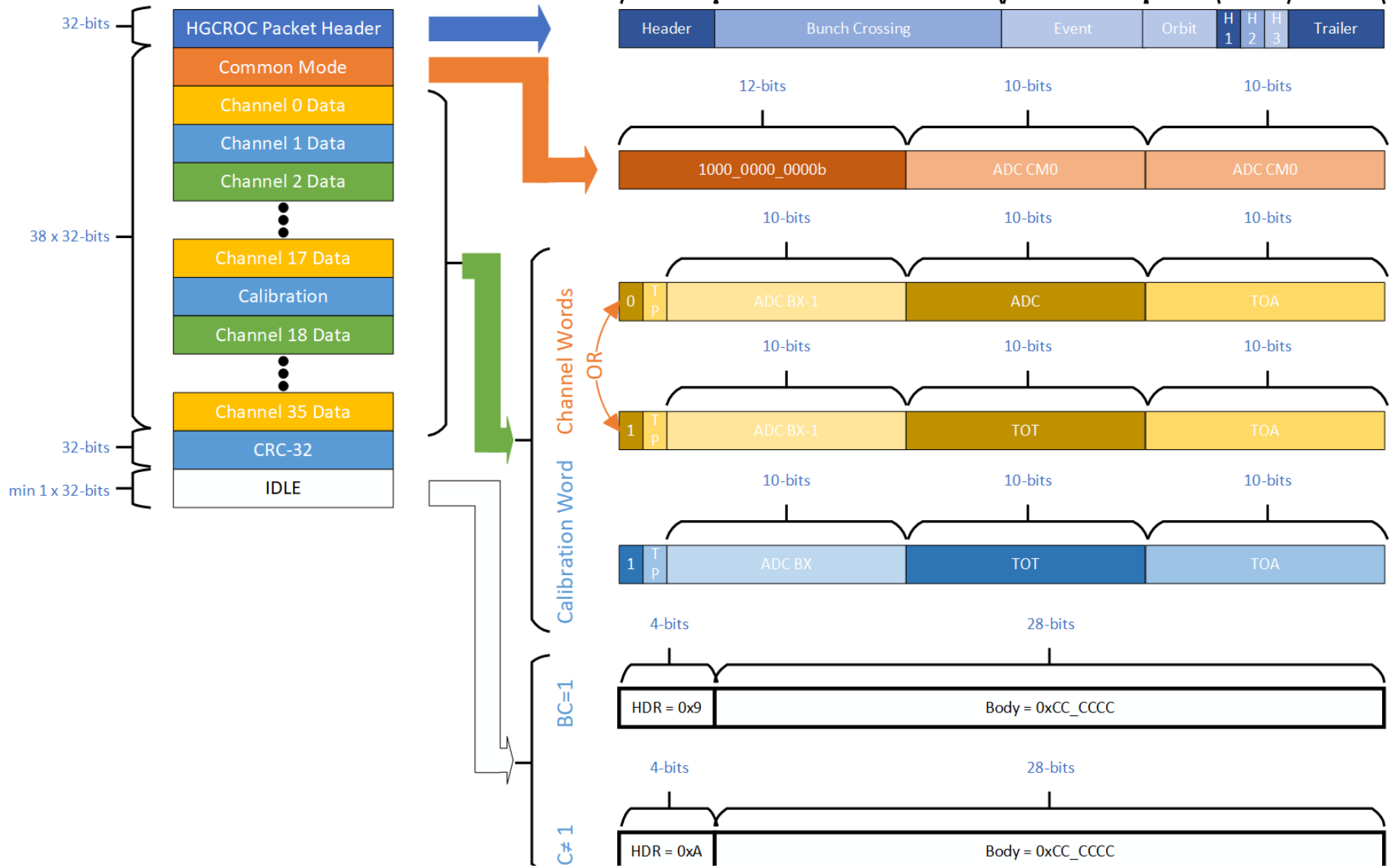


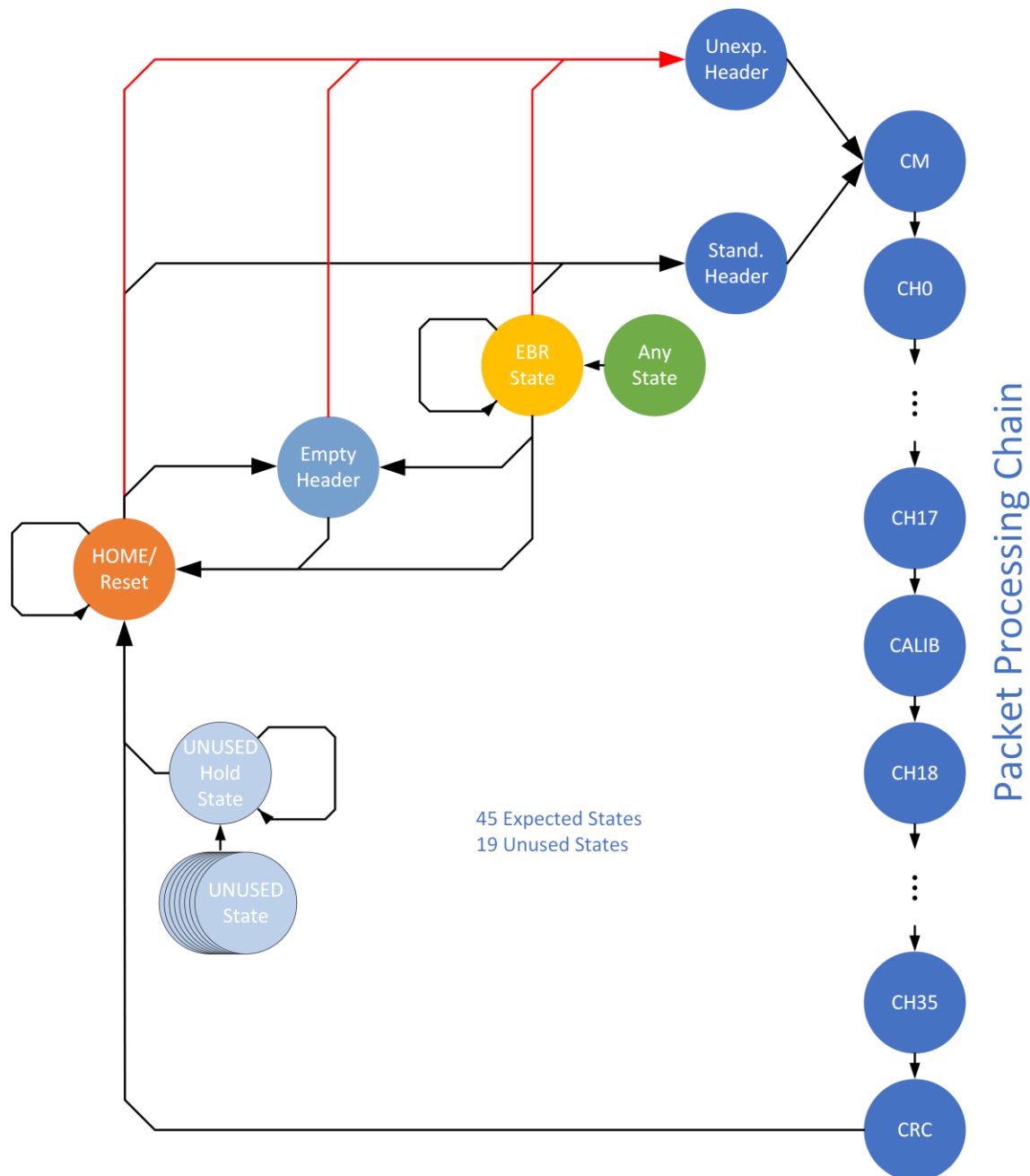
Backup Slides

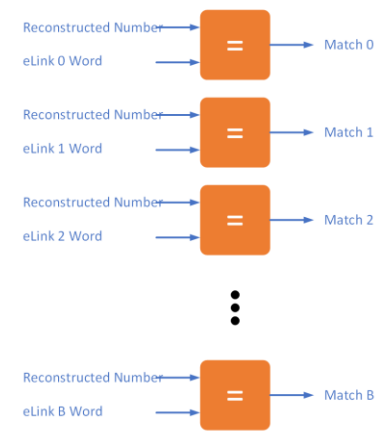
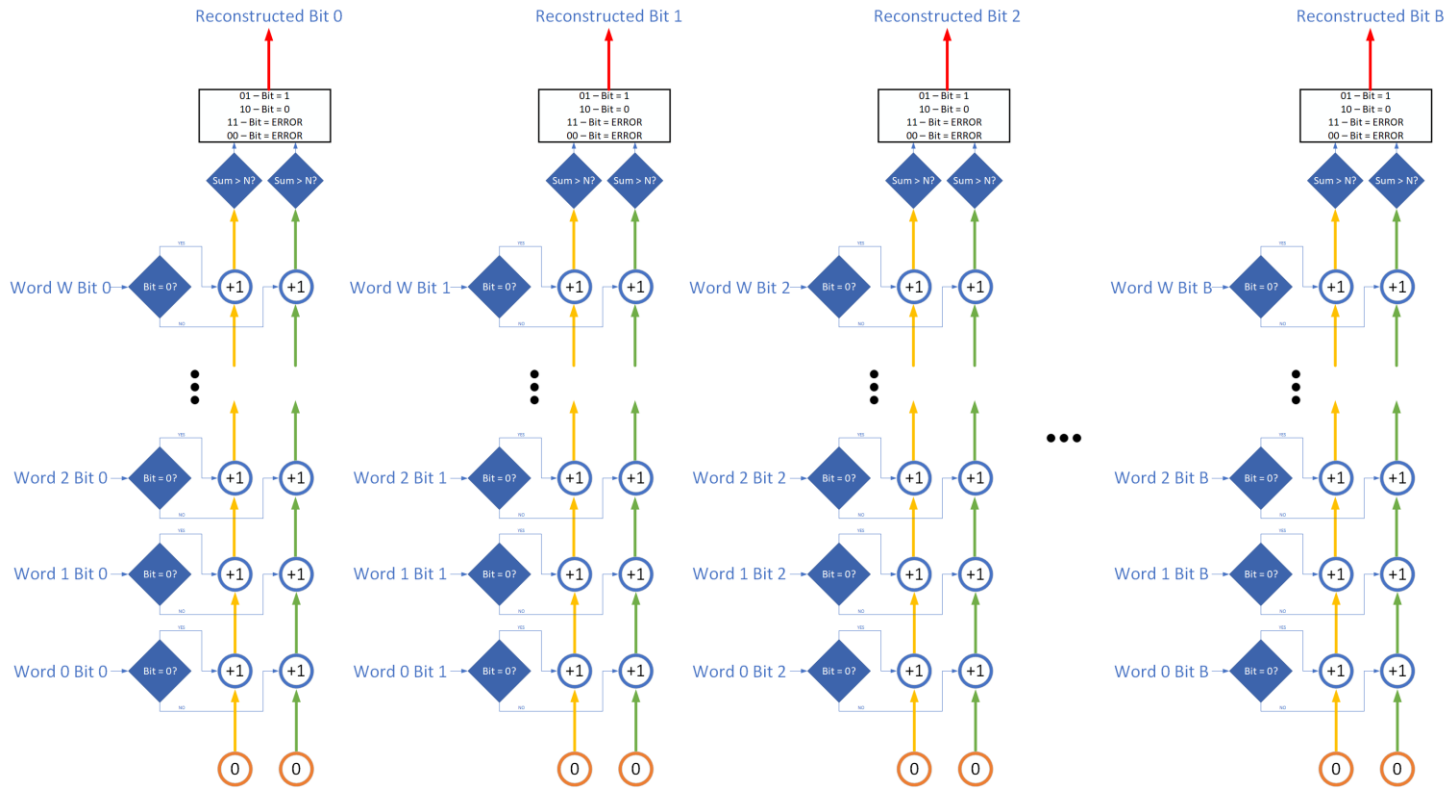
In partnership with:



HGCROC Data Frame





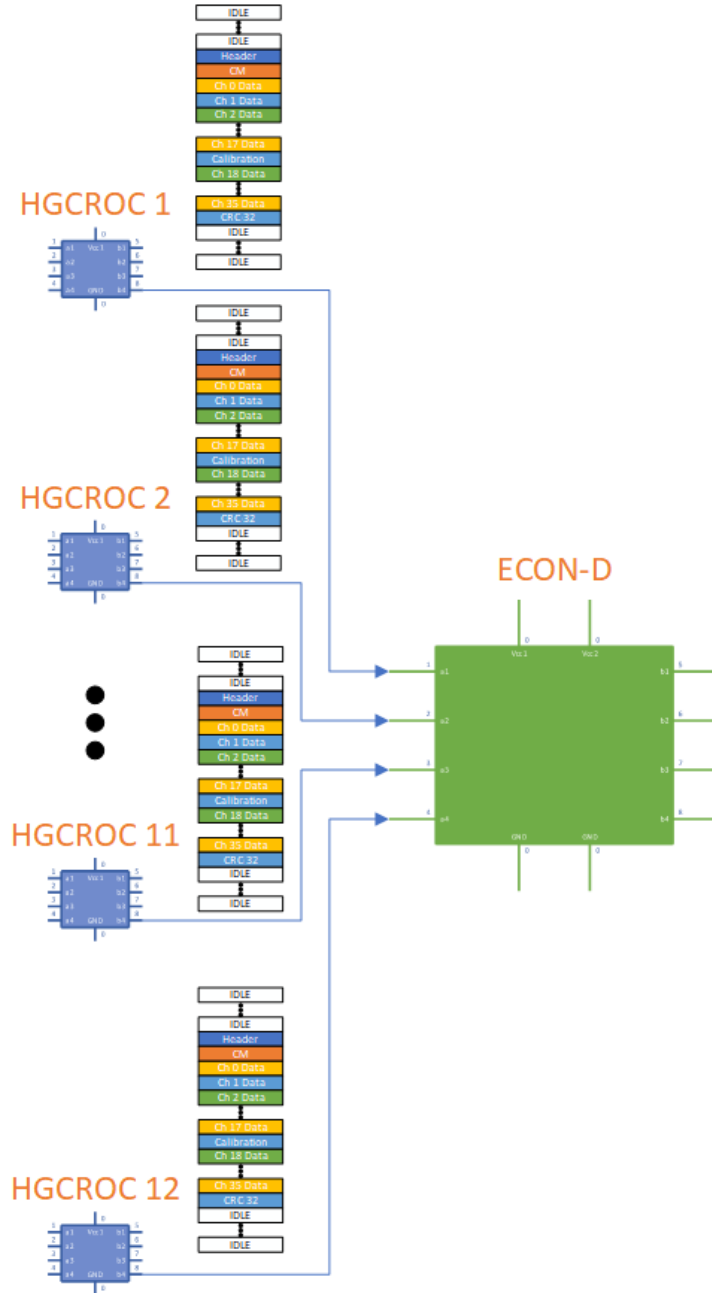


Packet Veto

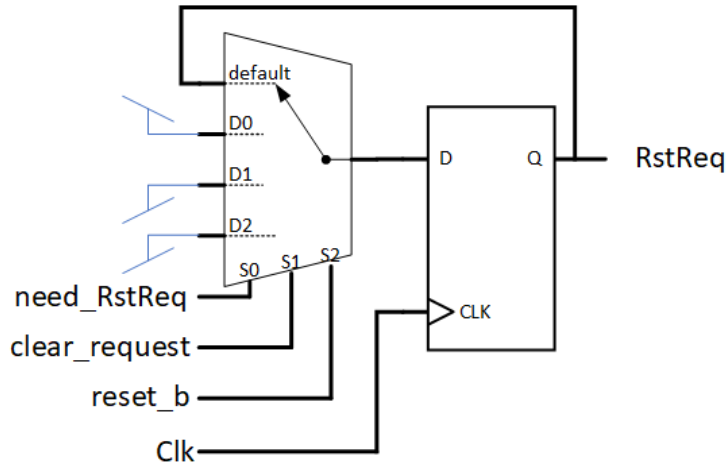
- **Expected or Unexpected Packet** – did the ECON get an L1A for this packet?
- **Matching or Unmatching Packet** – did the ECON’s internal event/bunch/orbit match that transmitted by the HGCROC?
- **Valid or invalid Header-Trailer** – was there a problem in the transmission of the HGCROC’s packet?
- **Valid or invalid EBO** – was there a problem in the transmission of the HGCROC’s packet?

- A simple lookup table allows user-definition of acceptable packets.

Binary Code	Address	Header	HT	EBO	HGCROC to ECON
0000	0	Unexpected	Valid	Valid	Mismatch
0001	1	Unexpected	Valid	Valid	Match
0010	2	Unexpected	Valid	Invalid	Mismatch
0011	3	Unexpected	Valid	Invalid	Match
0100	4	Unexpected	Invalid	Valid	Mismatch
0101	5	Unexpected	Invalid	Valid	Match
0110	6	Unexpected	Invalid	Invalid	Mismatch
0111	7	Unexpected	Invalid	Invalid	Match
1000	8	Expected	Valid	Valid	Mismatch
1001	9	Expected	Valid	Valid	Match
1010	10	Expected	Valid	Invalid	Mismatch
1011	11	Expected	Valid	Invalid	Match
1100	12	Expected	Invalid	Valid	Mismatch
1101	13	Expected	Invalid	Valid	Match
1110	14	Expected	Invalid	Invalid	Mismatch
1111	15	Expected	Invalid	Invalid	Match

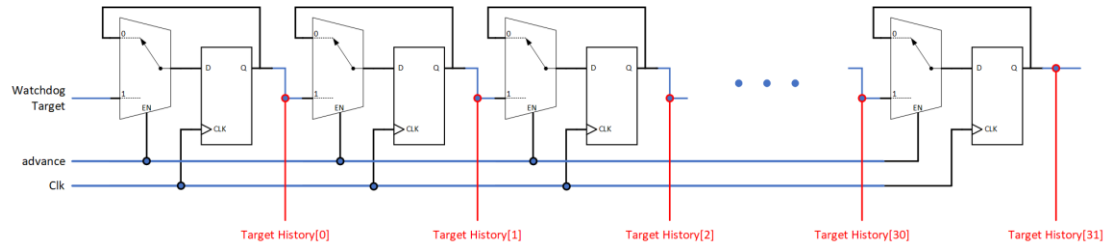


Persistence



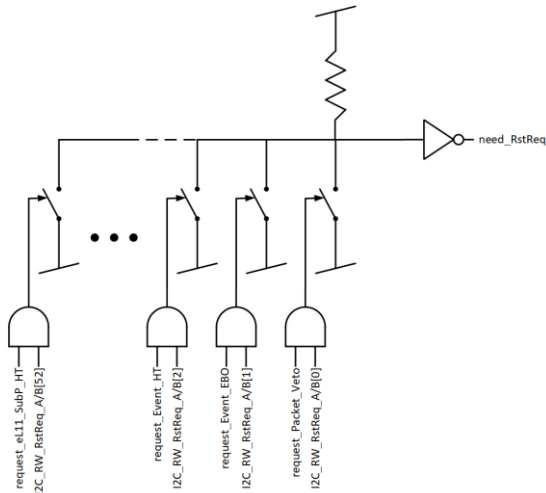
Reset Request

History



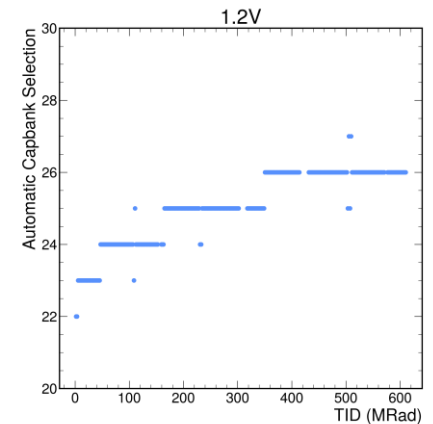
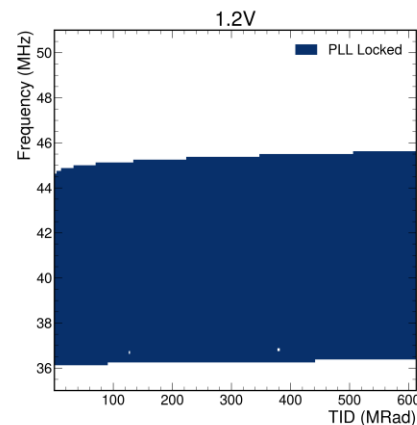
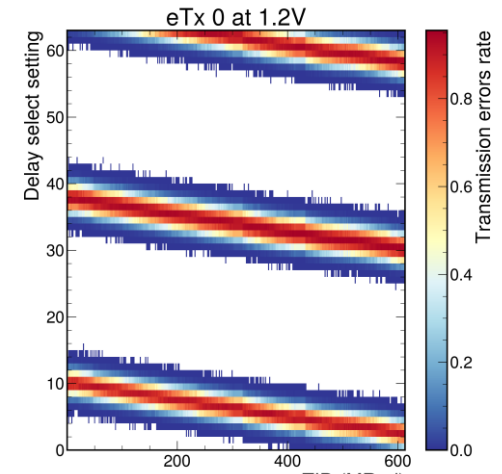
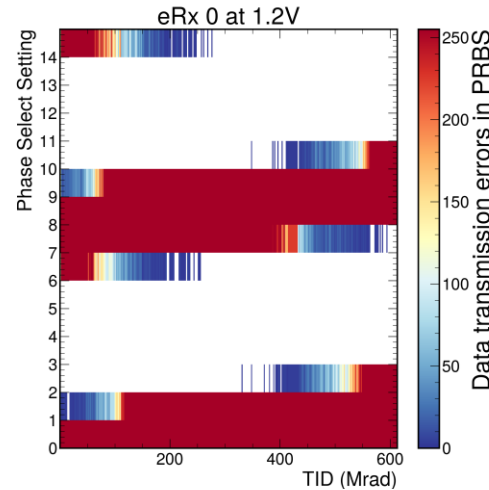
Condition		Slow Control Limit Register
Was the last target active?	Target History[0] == ONE	Watchdog's Limit[0] == 1'b1
Were the last two targets active?	Target History[1:0] == 2'b11	Watchdog's Limit[1] == 1'b1
Were the last four targets active?	Target History[3:0] == 0xF	Watchdog's Limit[2] == 1'b1
Were the last 8 targets active?	Target History[7:0] == 0xFF	Watchdog's Limit[3] == 1'b1
Were all the last 32 targets active?	Target History[31:0] == 0xFFFF_FFFF	Watchdog's Limit[4] == 1'b1
Were any 8 of the last 32 targets active?	Sum of active Target History bits >8	Watchdog's Limit[5] == 1'b1
Were any 16 of the last 32 targets active?	Sum of active Target History bits >16	Watchdog's Limit[6] == 1'b1
Were any 24 of the last 32 targets active?	Sum of active Target History bits >32	Watchdog's Limit[7] == 1'b1

User Definability

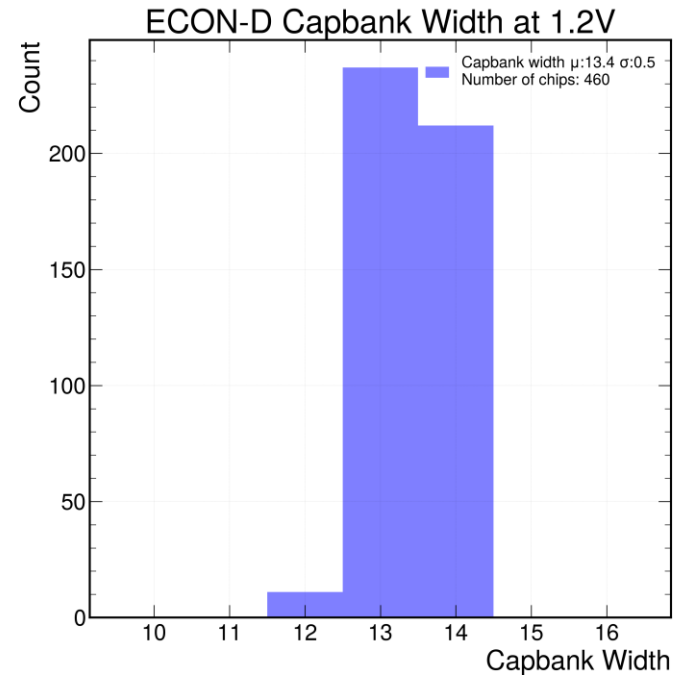
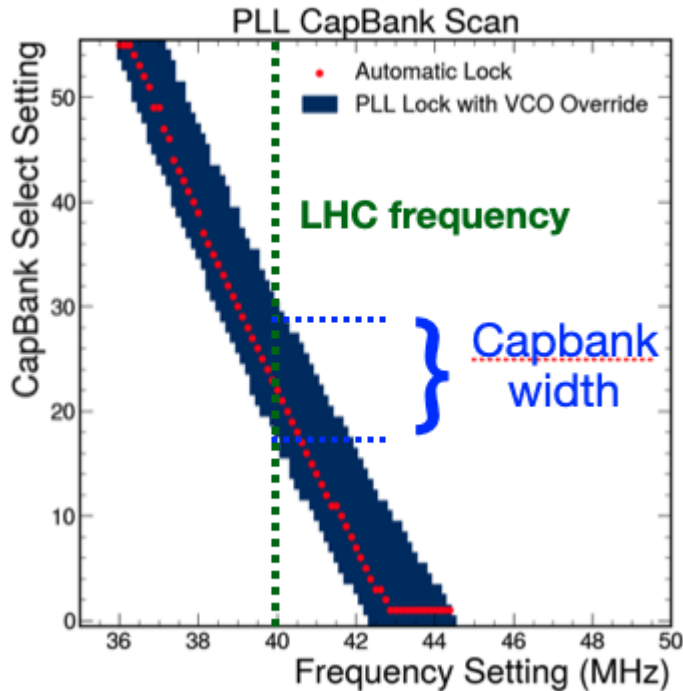


TID results

- As expected, observed small TID-dependence for “good phase” windows of 1.28 Gbps IOs
- As expected, observed small TID-dependence for PLL locking range and automatically selected reference capacitance (CapBank setting)



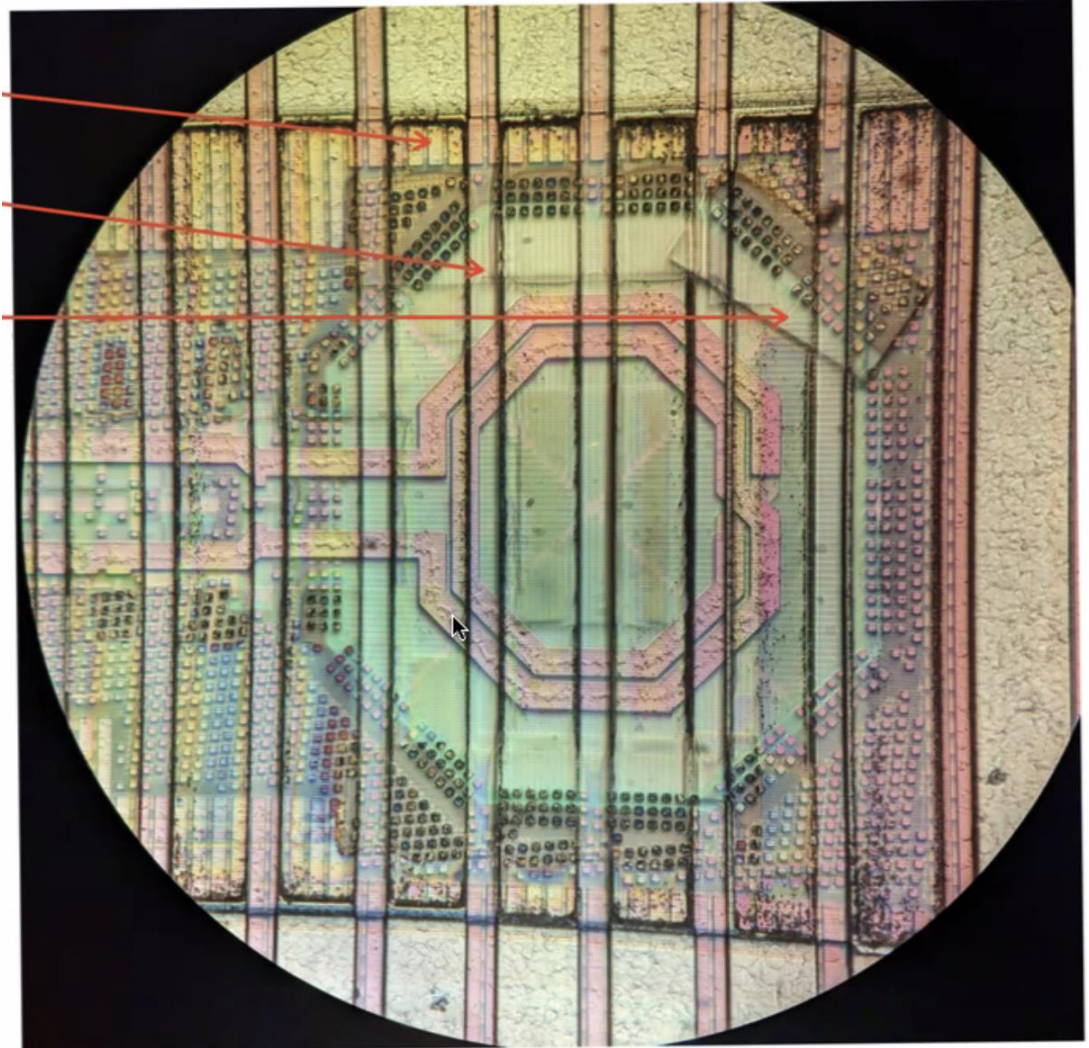
PLL frequency and capacitance scan



- **Test procedure:**
 - Scan reference clock (35-45 MHz) and reference capacitance for PLL LC VCO (54 internal “CapBank” settings)
 - Identify “good” scan points where PLL locks to reference clock
- **Result :**
 - PLL locks reliably in range 36-44 MHz using full range of CapBank settings
 - PLL has wide range of CapBank settings that lock at LHC frequency (~40 MHz)
 - Good uniformity of “CapBank width” over all ~800 ECON tested so far.
- **Notes :**
 - PLL automatically selects reference capacitance during normal operation

Fixed problem from ECON_D_P1

- Erroneously placed top level metal above PLL's VCO. This changed its frequency response.
- FIB Processing removed the unwanted layer in ECON_D_P1.
- Specialized DRC checks added to ensure we didn't do this again



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