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ECON-D and ECON-T: Design and Production Testing

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With over 6 million channels, the High Granularity Calorimeter (HGCAL) for the CMS HL-LHC Upgrade presents a unique data challenge. The ECON ASICs provide critical on-detector data reduction for the 40 MHz trigger path (ECON-T) and 750 kHz data acquisition path (ECON-D) of the HGCAL. The ASICs, fabricated in 65nm CMOS, are rad-tolerant (600 Mrad) with low power consumption (<2.5 mW/channel). This presentation is the first comprehensive description of the ECON designs, first functionality and radiation tests for the ECON-T ASIC, and first high statistics characterization results from the full production of 75k ECON-D and ECON-T ASICs.

Summary (500 words)

The CMS HGCAL is a 47-layer sampling calorimeter that features fine readout segmentation, and which replaces the existing endcap calorimeter detectors for the High Luminosity phase of the LHC (HL-LHC). Overall, the HGCAL has more than six million channels spanning an area of 600 m2 with 0.5-1.0 cm2 sensor pads. The sensor signals are digitized by HGCROC ASICs. This digitized data must then be processed and zero-suppressed along two independent pathways. The trigger path is the responsibility of the ECON-T ASIC and provides information to the Level 1 Trigger every bunch crossing at the 40 MHz event rate. The data path is the responsibility of the ECON-D ASIC and provides packets to the data acquisition system from events that have passed the Level 1 Trigger (750 kHz L1 accept rate).

In broad terms, ECON-D and ECON-T share the same infrastructure. Both ECON chips receive a 320 MHz system clock and a fast command stream from the back end. A beam synchronous clock is then recovered in each chip from this stream. Both designs receive slow control data as a means of user-defined programming. Both chips receive up to twelve 1.28 GHz input streams from HGCROC front-end chips. Both chips align to their input streams identically. Finally, both chips transmit their resultant data frames to the back end via a variable number of 1.28 GHz serial streams. All these aspects of the ECON chips were deliberately held common to both designs and as many of these elements as possible have been obtained from the use or reuse of silicon-proven IP.

ECON-D (Figure 1) receives a continuous stream of 32-bit words from each of its HGCROC inputs every 40 MHz event period. Those words are either idle words or components of the 41-word HGCROC event packet. Properly aligned in an error-free system, all HGCROC output the same packet component at the same time. It is the responsibility of ECON-D to recognize the transmission of packets from the HGCROC, extract vital information, reformat that data into outbound ECON-D packets, buffer and transmit them. ECON-D also corrects errors where possible, vetoes unacceptable packets, monitors status and requests resets when necessary.

The ECON-T (Figure 2) is fundamentally different from the ECON-D in that, as part of the trigger path, it receives a unique and complete packet every bunch crossing from each of its HGCROC inputs. Each HGCROC trigger packet is 32-bits wide and consists of a 4-bit header and 7-bits of charge data from four trigger channels. ECON-T applies one of five algorithms to the data received, formats the data into a common frame, buffers data and drives its frames onward.

The first ECON-T prototype was submitted in June of 2021. Comprehensive chip testing and radiation characterization since December of that year has revealed no major issues. The first ECON-D prototype was sub-

mitted in March of 2023. Comprehensive chip testing and radiation characterization since June has likewise revealed no major issues. Final production versions of the chip were submitted for fabrication in December of 2023.

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