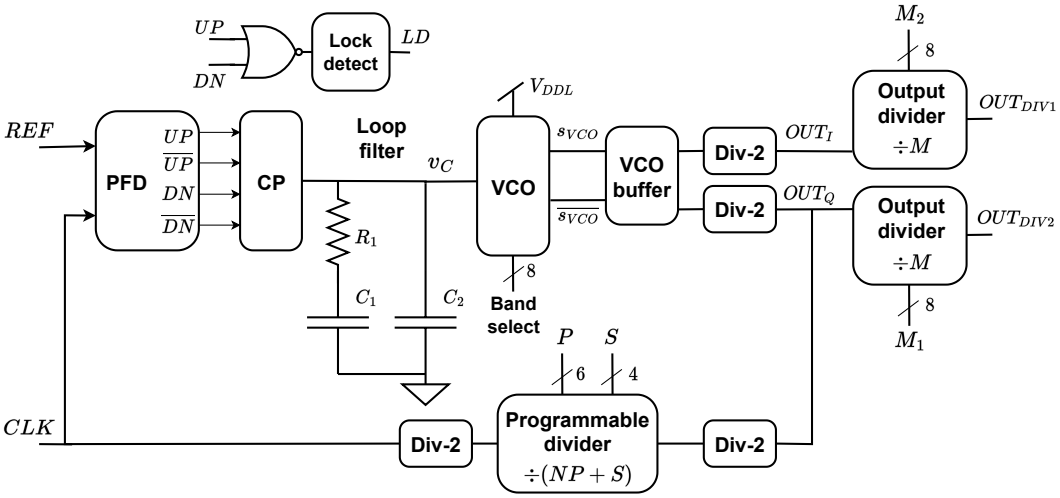

Figure 1: Top-level block diagram of the proposed frequency synthesizer.

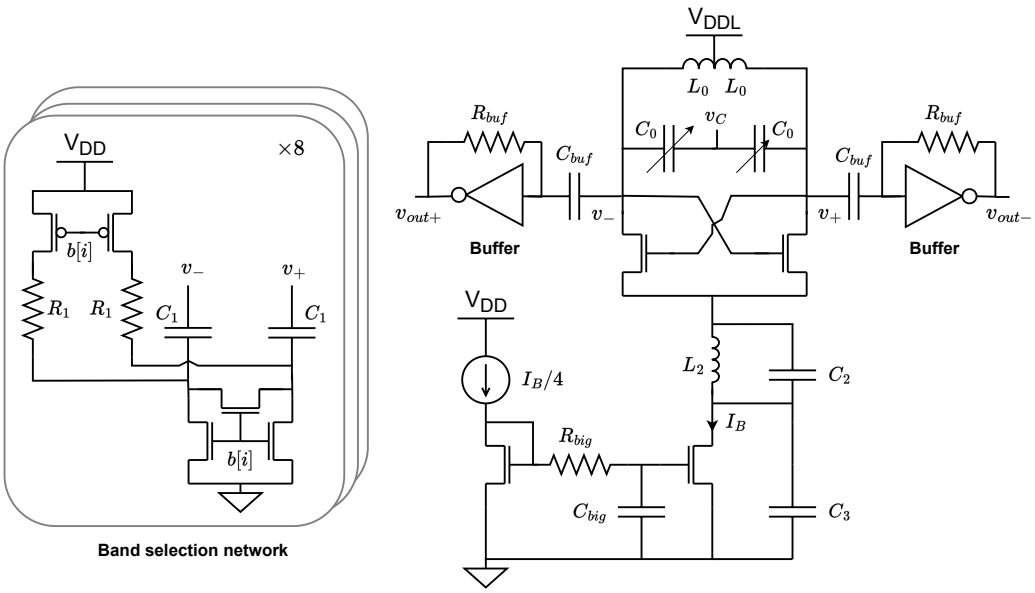

Figure 2: Schematic of the voltage-controlled oscillator (VCO) used within the frequency synthesizer.

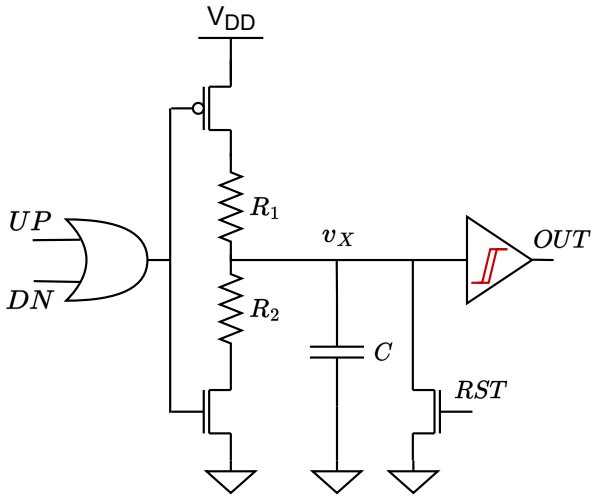

Figure 3: Schematic of the lock-detector circuit.

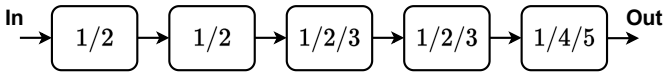

Figure 4: Block diagram of the output frequency divider. The divide ratio of each stage can be independently switched between two values, as shown.

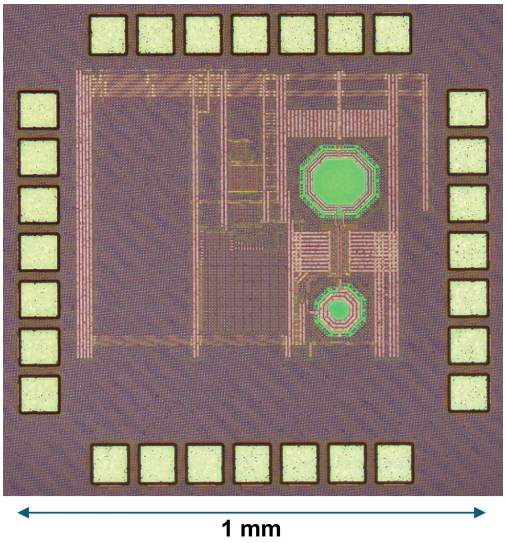

Figure 5: Die photograph of the proposed frequency synthesizer. The inductors used by the VCO are visible.