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U.S. DEPARTMENT OF ENERGY

An Integer-N Frequency Synthesizer for Flexible On-Chip Clock Generation

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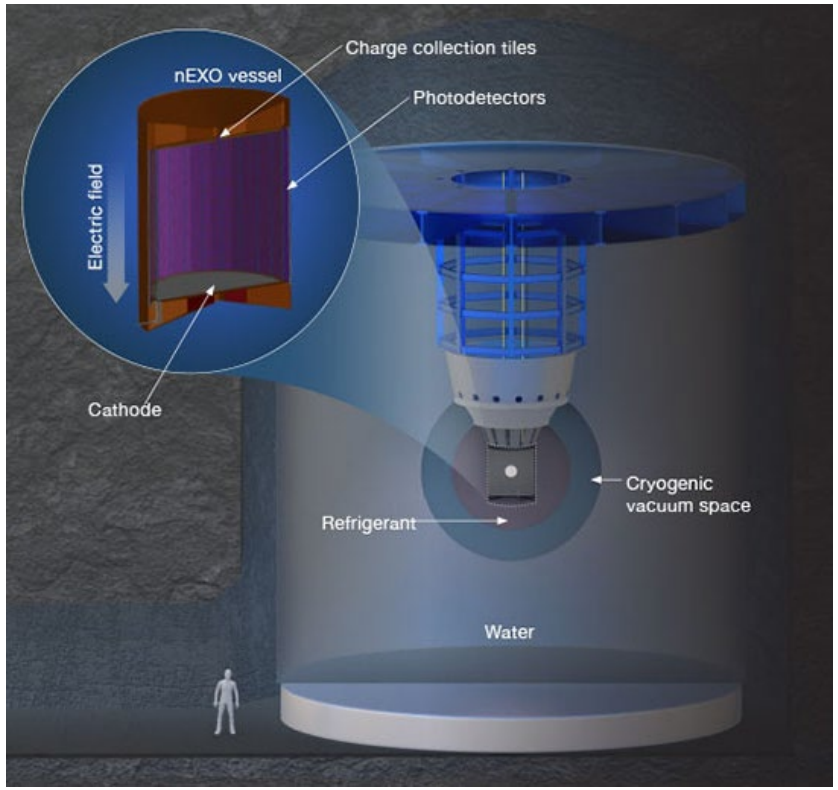
Introduction

- Several rare-event search experiments, such as nEXO, require high-data-rate links between AFEs and digital back-ends over lossy channels (e.g., radio-pure cables within a noble liquid cryostat).
- Preferred solution using a single high-speed cable:
  - To simplify clock distribution, the back-end forwards a low-frequency clock (e.g., from a crystal oscillator) to the AFE over a separate low-speed cable.
  - In downlink mode, the AFE synchronizes an internal high-frequency oscillator to the forwarded clock and uses this to serialize the downlink data stream.
  - In uplink mode, the AFE recovers non-return-to-zero (NRZ)-encoded serial data sent by the digital back-end.



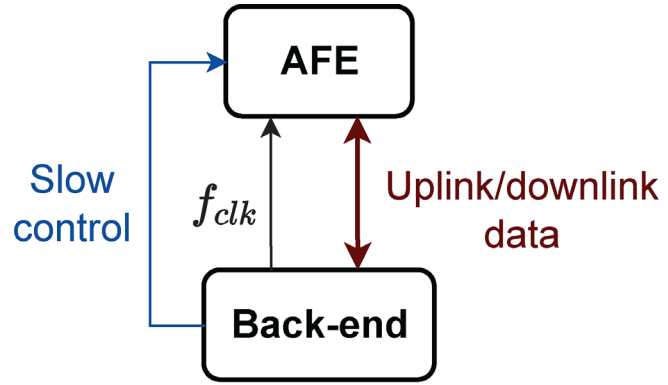
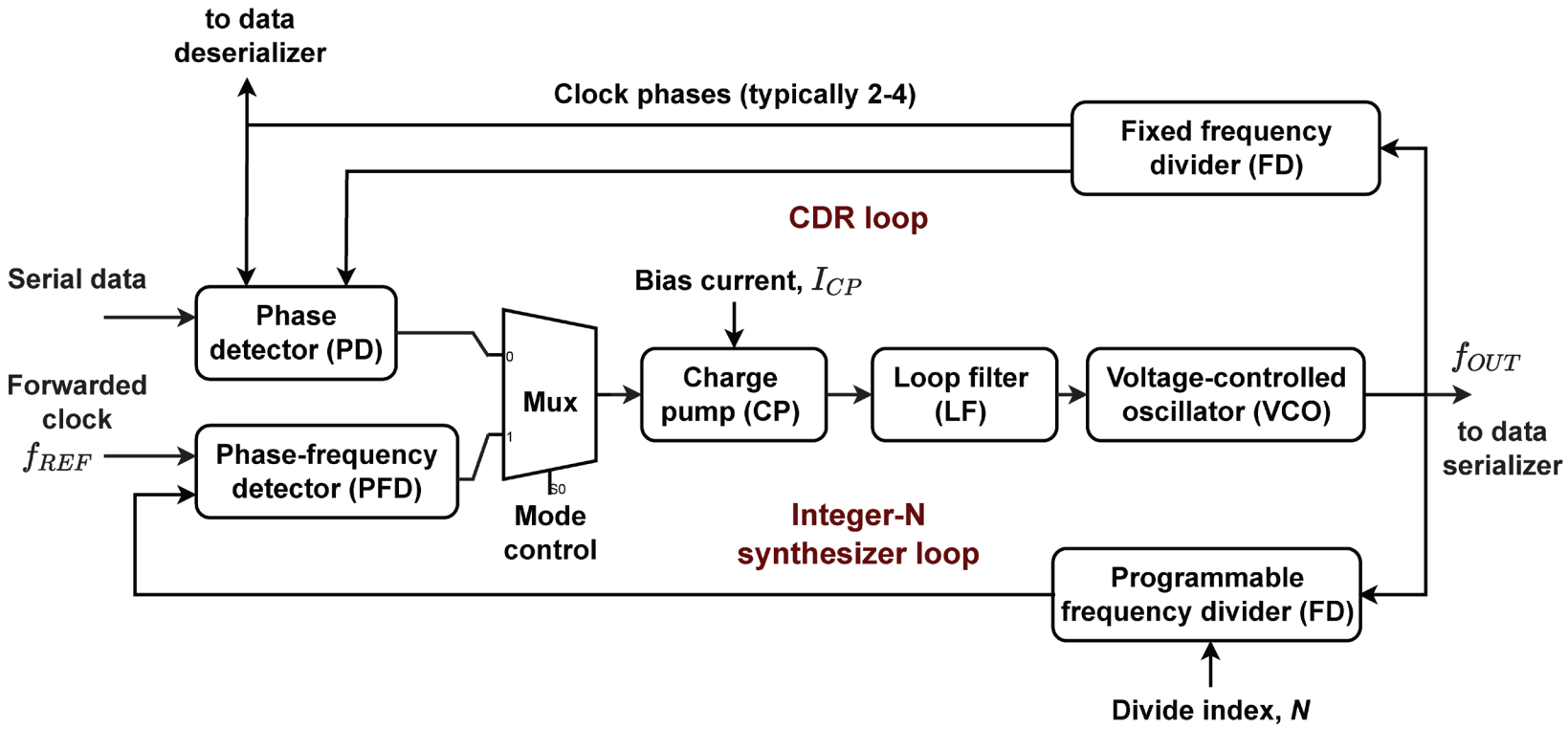


Image source: https://nexo.llnl.gov/nexo-overview

Circuit architecture

- Proposed solution (similar to the lpGBT clock management system):
  - PLL-based integer-N frequency synthesizer for high-speed clock generation and data serialization in downlink mode.
  - PLL-based clock-and-data-recovery (CDR) circuit for data retiming and high-speed clock recovery in uplink mode.
  - Both modes use a PLL, so several building blocks can be combined (or reused) to save chip area.

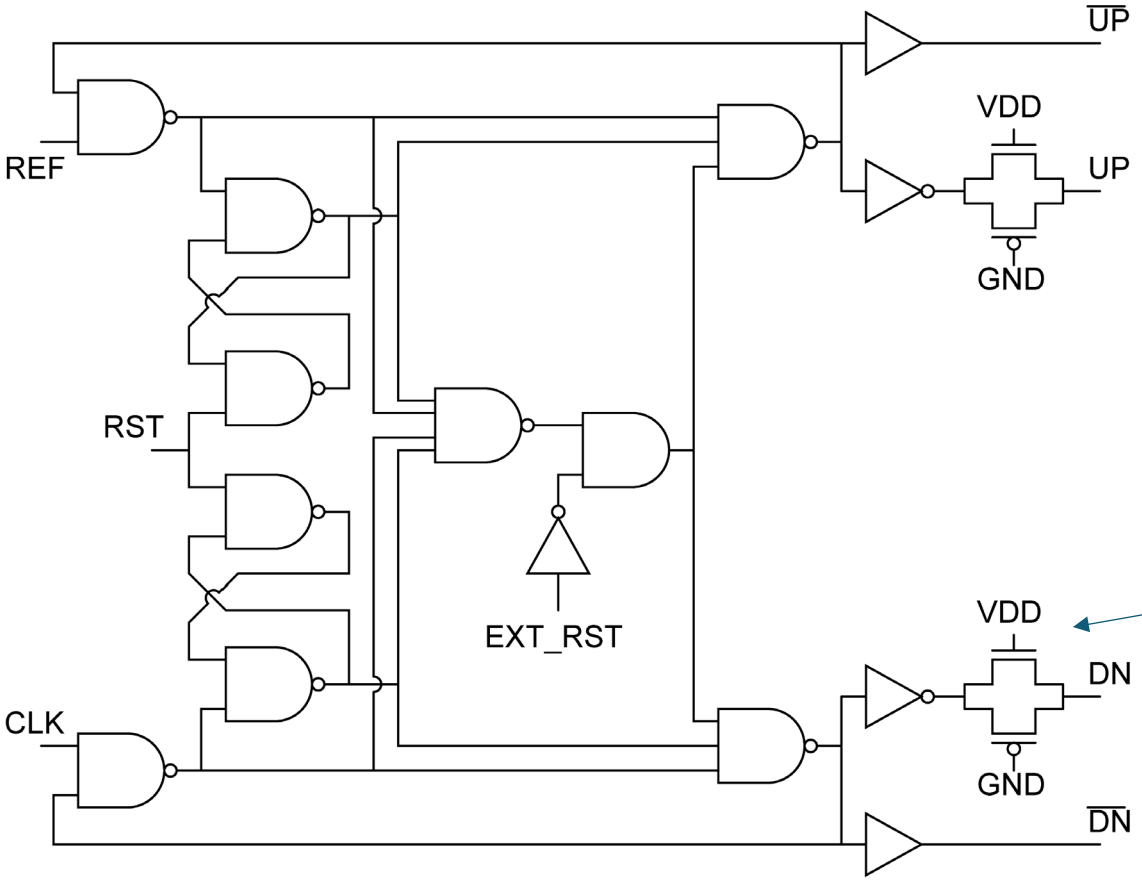


Initial design specifications

- Nominal forwarded clock frequency, f_{REF} = 50 MHz
- Nominal VCO frequency, f_{OUT} = 6 GHz
  - Chosen to enable use of LC oscillators (preferred over ring oscillators due to lower phase noise and power supply sensitivity) using high-Q on-chip inductors
- Nominal uplink data rate, $f_{UP} = f_{OUT}/2$ = 3 Gb/s
  - Chosen to enable 2x oversampling of the input data stream, which simplifies the design of the CDR phase detector (PD)
- This talk focuses on the design of the frequency synthesizer
  - Implemented in the TSMC 65 nm CMOS process.
  - No radiation hardness requirements
  - Power consumption should be less than ~5 mW
  - Results acquired at room temperature, but operation down to 77K is desirable

Integer-N synthesizer design

Phase-frequency detector (PFD)



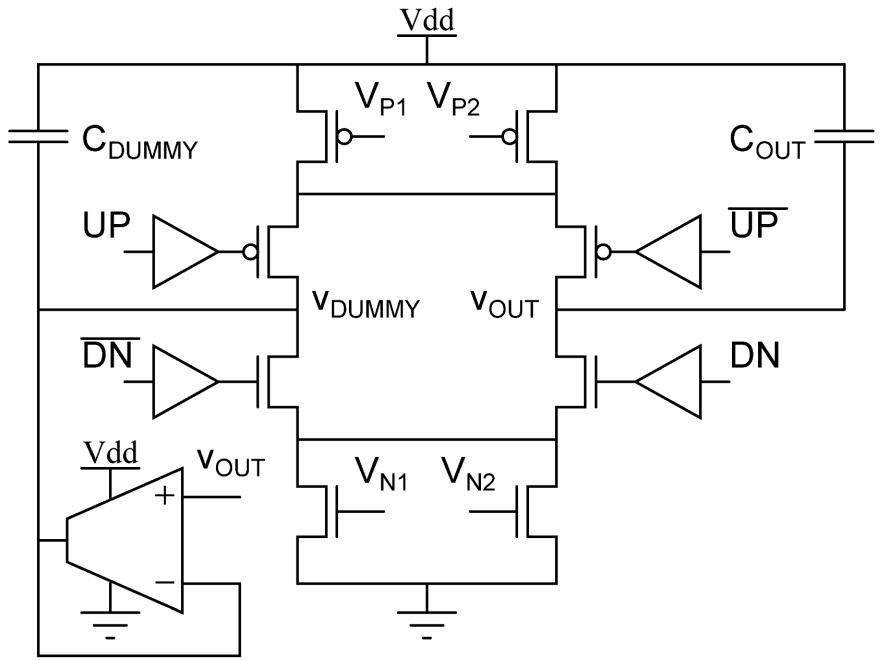
- Used in the frequency synthesizer loop
- Efficient implementation of the commonly-used sequential PFD circuit
- Guarantees minimum UP/DN pulse width even in the locked state, thus eliminating any dead zone around the origin of the PFD transfer curve
- Insensitive to input duty cycle
- Relatively low time delay (three NANDs plus a couple of inverters)

"Always on" transmission gate for equalizing time delays

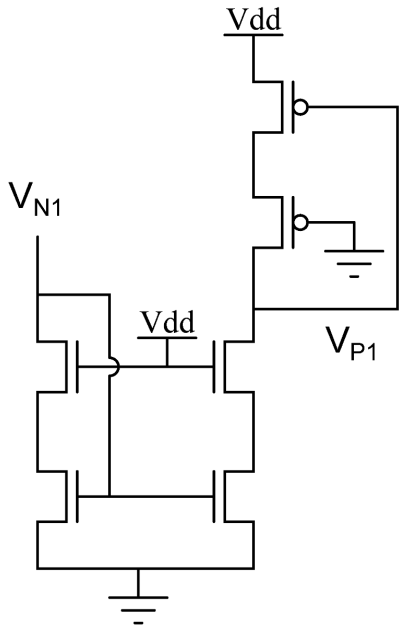
Young, I. A., Greason, J. K., & Wong, K. L. (1992). A PLL clock generator with 5 to 110 MHz of lock range for microprocessors. *IEEE Journal of Solid-State Circuits*, *27*(11), 1599-1607.

Charge pump (CP)

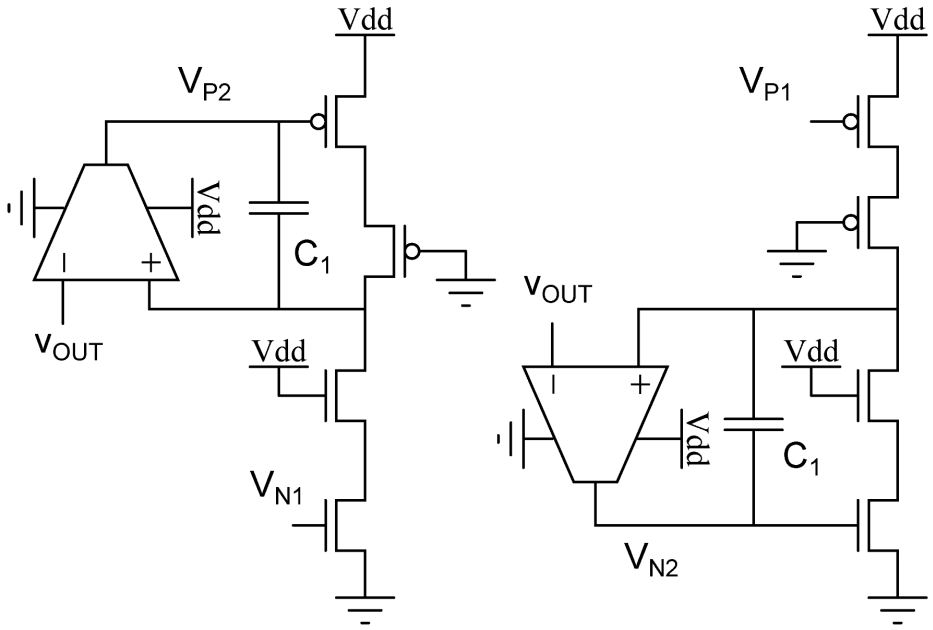
- Fully-differential structure to minimize charge injection errors
  - An OTA maintains the dummy voltage (V_{dummy}) near the output (V_{out}) to minimize switching transients
- Cascoded current sources to improve matching between N- and P-sides
  - Matching is further improved by using matched replica biasing
  - Both the N- and P-side bias currents are split into 2 equal parts to minimize N- and P-side mismatch:
    - One part is set by a fixed input current, the other is adaptively set by a replica biasing network



Main charge pump



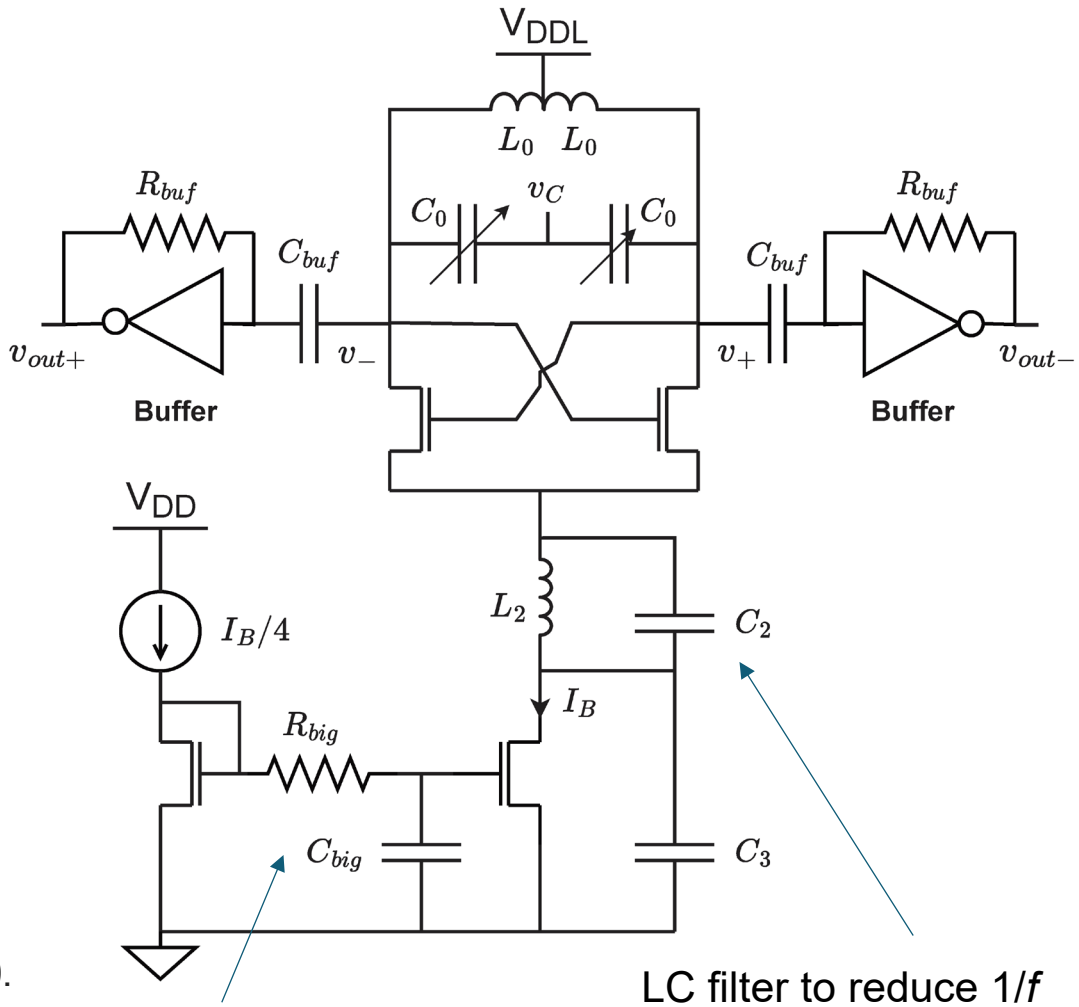
Fixed bias generation network



Replica biasing network

Voltage-controlled oscillator (VCO)

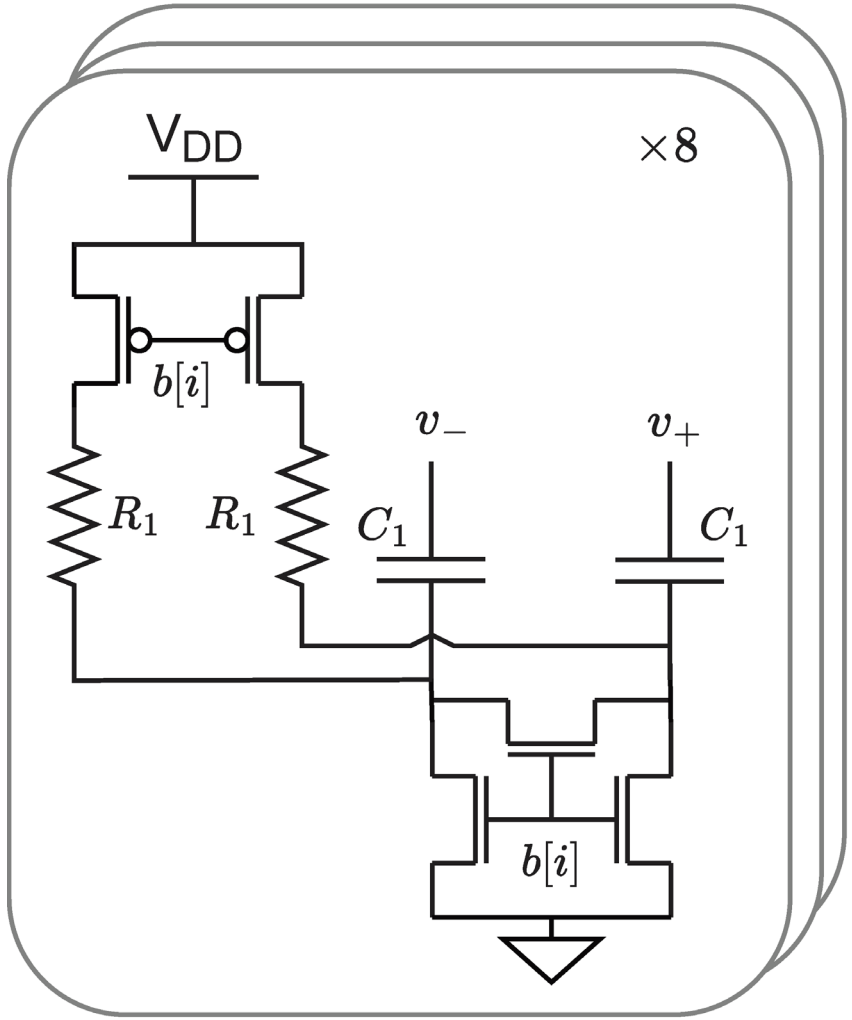
- Cross-coupled CMOS VCO design.
  - The *LC* tank uses an on-chip center-tapped circular spiral inductor.
- Two levels of frequency tuning:
  - Coarse tuning (band switching) using a network of 8 equal-valued switched capacitors.
  - Fine tuning (by the PLL) using accumulation-mode MOS varactors.
- Switch, resistor, and varactor sizes were optimized to minimize phase noise for a given tuning range.
- A tail current *LC* filter (tuned to $2f_0$) reduces $1/f$ noise up-conversion but at the cost of additional layout area.



Hegazi, E., Sjoland, H., & Abidi, A. A. (2001). A filtering technique to lower LC oscillator phase noise. *IEEE Journal of Solid-State Circuits*, *36*(12), 1921-1930.

Switched capacitor network

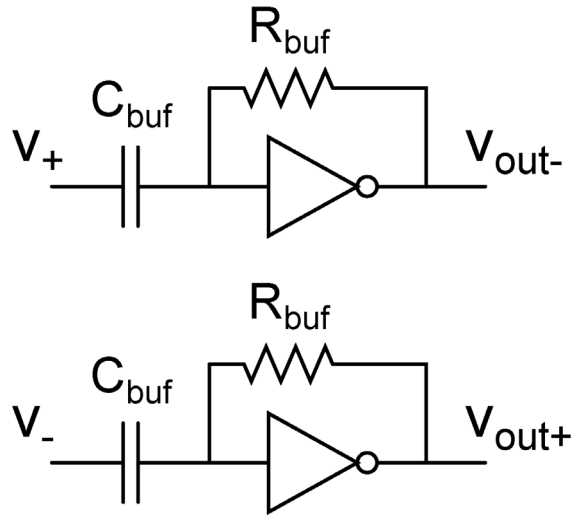
- Differential switched capacitor circuit.
  - Differential switch configuration reduces impact of R_{on} on tank Q.
  - Small NMOS switches to ground define the drain/source voltages of the main switch when it is “on”.
  - Small PMOS switches and series resistors to V_{DD} prevent the drain/source voltages from exceeding V_{DD} when the main switch is “off”.



Band selection network

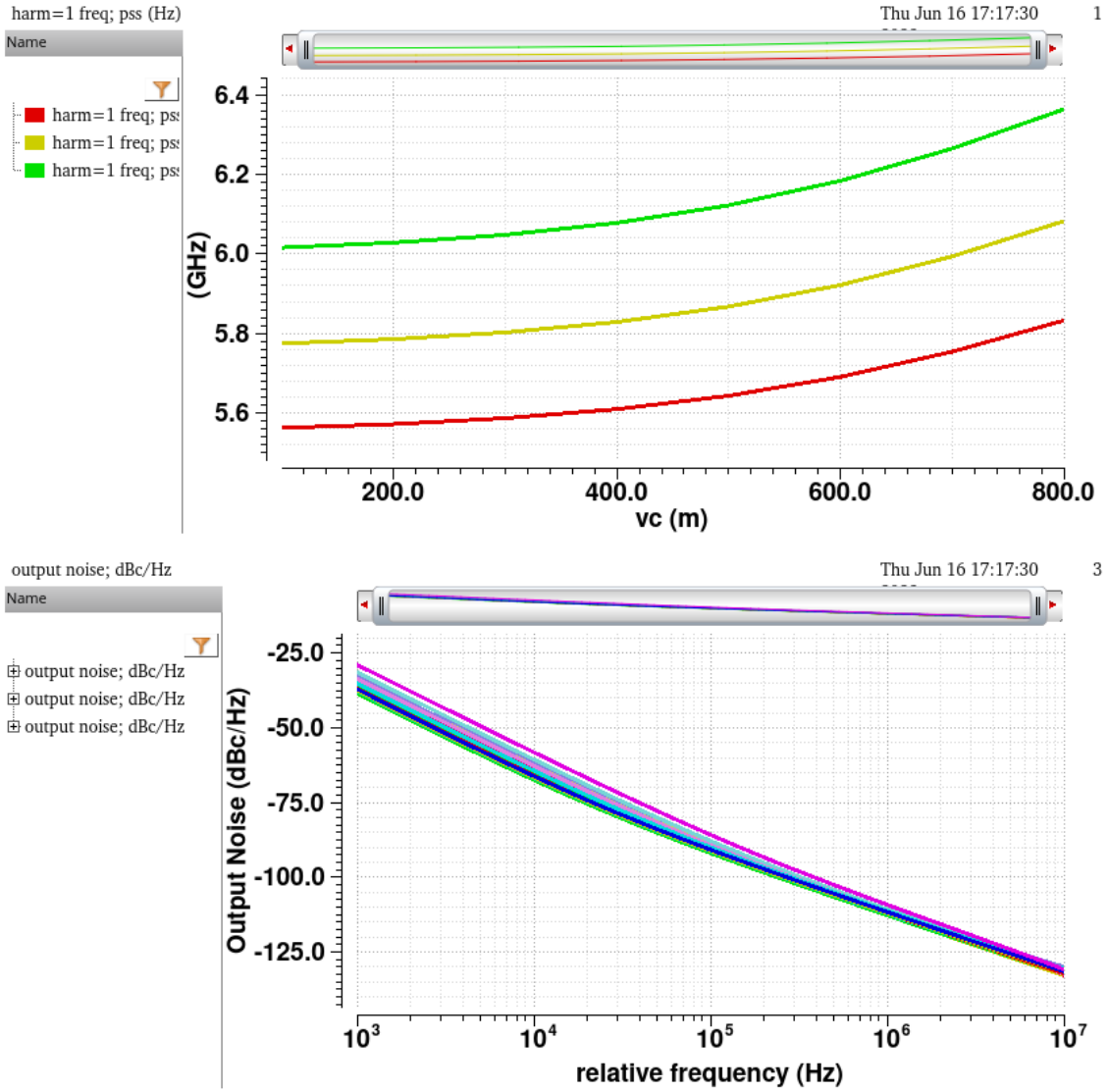
VCO buffer

- Converts the sinusoidal signals generated by the VCO into logic-level outputs.
- AC-coupled and self-biased design ensures insensitivity to the common-mode level of the VCO outputs.
- The supply-dependent input capacitance of the inverters degrades VCO supply sensitivity by modulating the total tank capacitance.
  - This effect can be reduced by running the buffer off its own high-PSRR LDO.



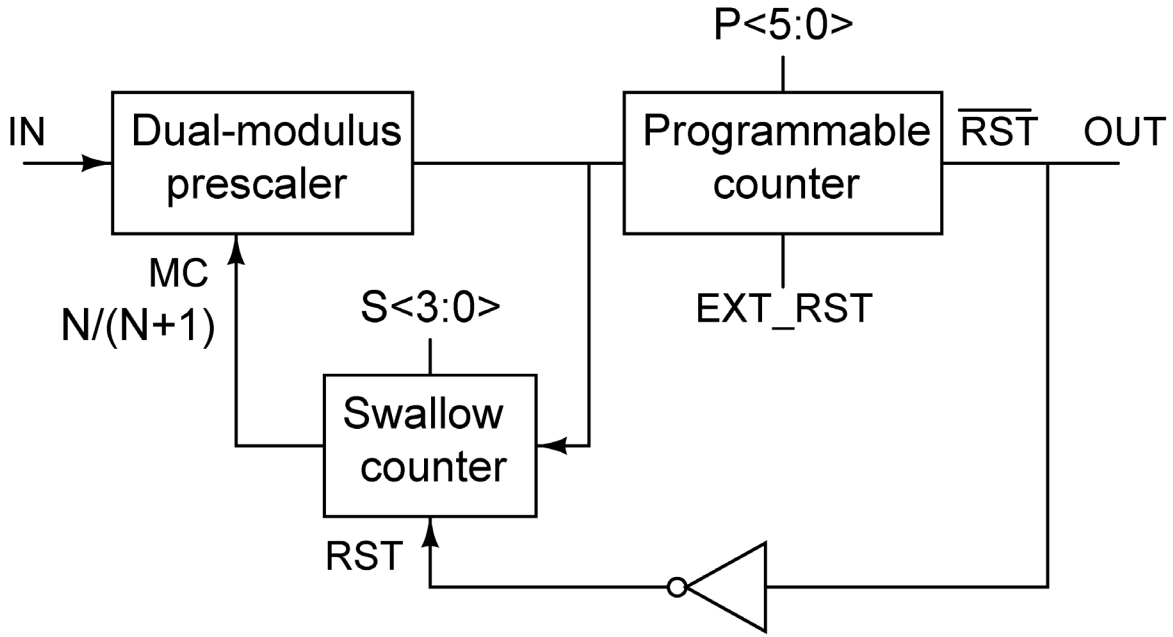
Optimized VCO (V_{DDL} = 0.8 V, I_B = 1.6 mA)

- Total tuning range = 5.6 GHz – 8.6 GHz (only the three lowest-frequency bands are shown).
  - Tuning voltage range reduced to 0.2-0.8 V to simplify the charge pump design.
  - VCO control gain $K_v \approx 0.6$ GHz/V.
- Phase noise ≈ –110 dBc/Hz at 1 MHz offset.
  - Significantly improved over unoptimized design.
  - The close-in phase noise shown in the figure includes the noise of an on-chip linear regulator (LDO) used to improve PSRR.
  - The LDO will be described later if time permits.



Programmable frequency divider (FD)

- Standard pulse-swallow counter topology.
- Total divide ratio = (NP + S), N = 2, P = 1-63, S = 0-15 (S < P).
- Output may need to be further divided by 2 to obtain a 50% duty cycle.



- Prescaler uses dynamic (TSPC) flip-flops to minimize propagation delay.
- Programmable counter uses a one-level carry select adder (CSA) to reduce propagation delay at the cost of a relatively small increase in complexity.

Lock detector (LD)

- Detects when total duty cycle of the PFD UP/DN outputs, D, is less than a fixed threshold, D_{min}.

Currents must balance in steady state, so

$$D\left(\frac{v_x}{R_2}\right) = (1-D)\left(\frac{V_{DD}-v_x}{R_1}\right) \Rightarrow v_x = \frac{V_{DD}}{\left(\frac{D}{1-D}\frac{R_1}{R_2}+1\right)}$$

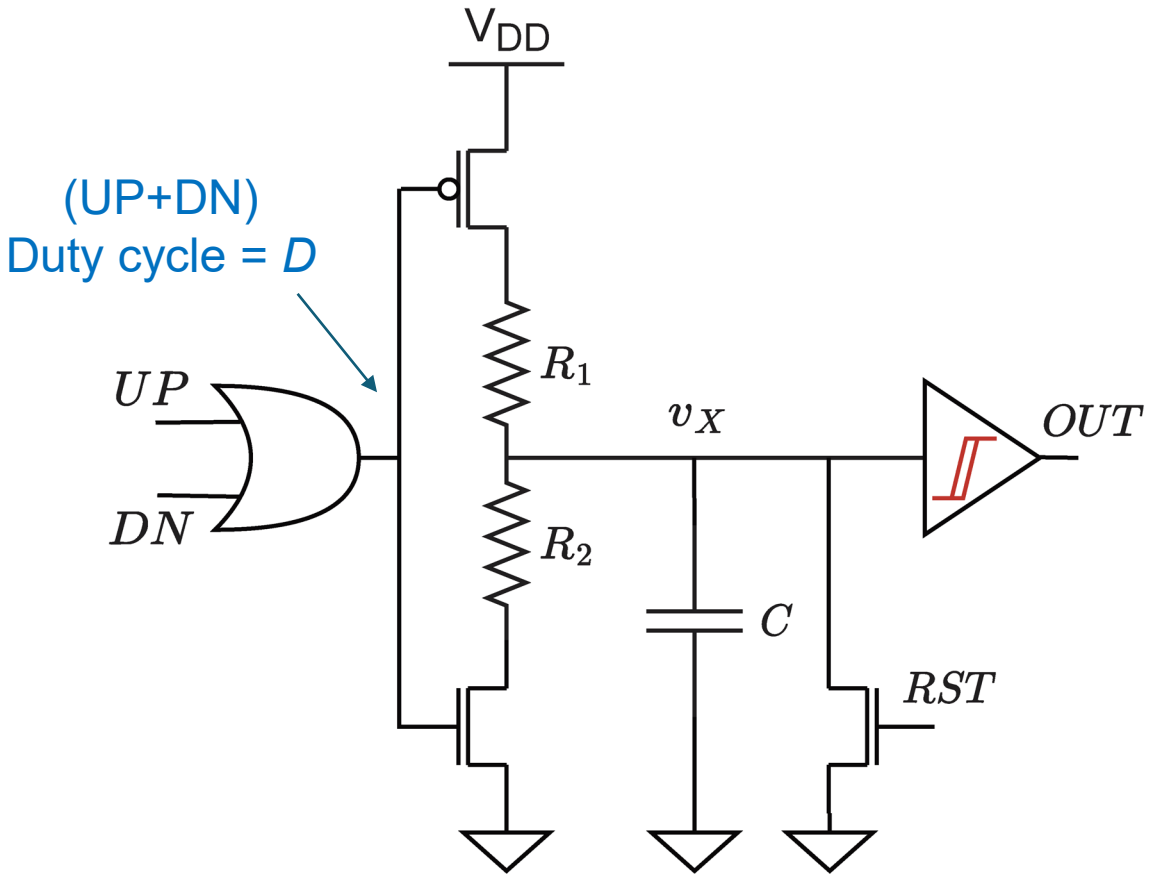
Schmitt trigger output goes high when $v_x \geq \alpha V_{DD}$

$\alpha =$ set by relative size of feedback transistors

$$\frac{V_{DD}}{\left(\frac{D}{1-D}\frac{R_1}{R_2}+1\right)} \geq \alpha V_{DD} \Rightarrow \boxed{D \leq \frac{1}{1+\left(\frac{\alpha}{1-\alpha}\right)\frac{R_1}{R_2}}}$$

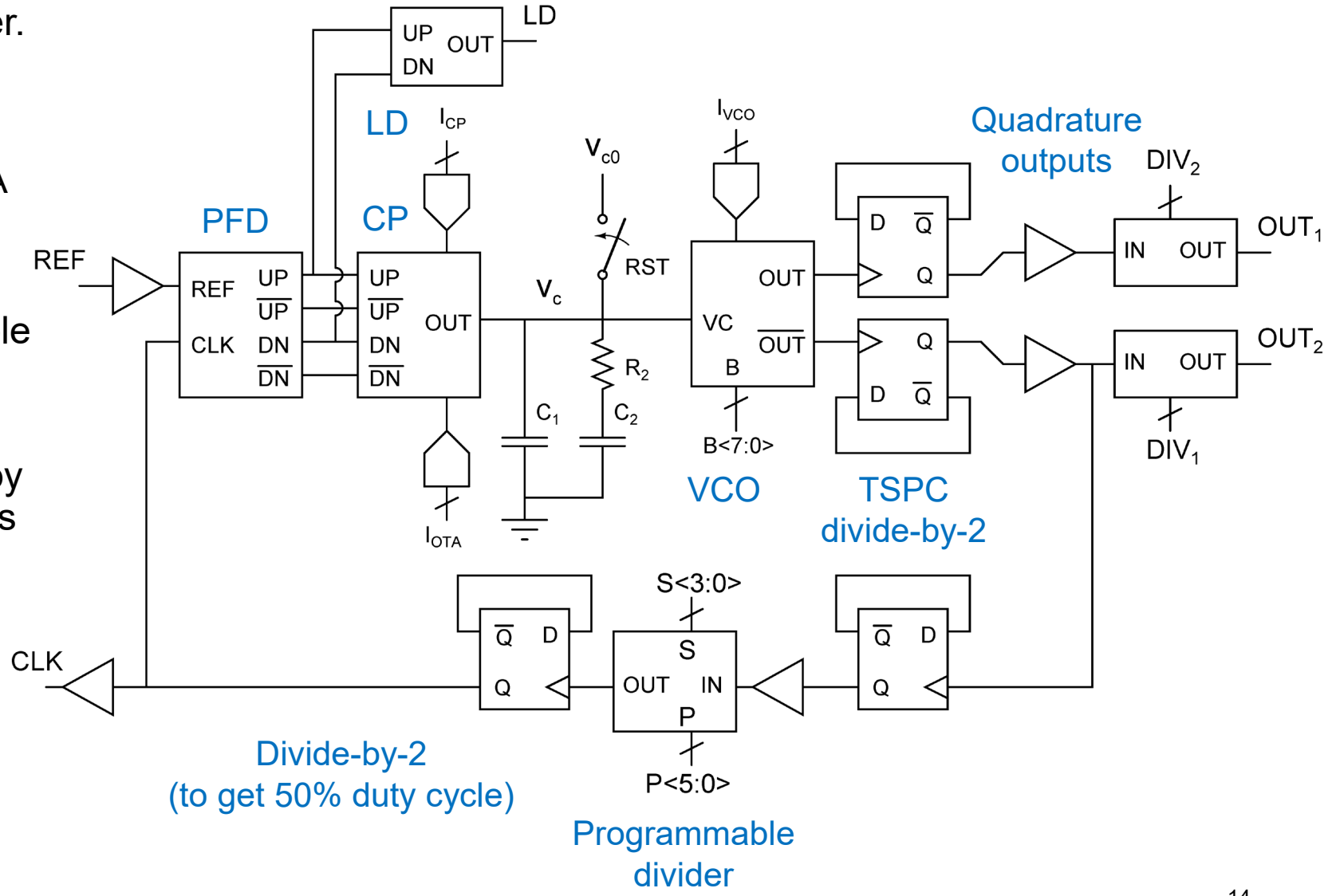
Current design: $\alpha \approx 2/3,\ R_1/R_2 = 8 \Rightarrow D_{min} \approx \frac{1}{17} = 0.059$

Note that D_{min} is ratiometric and thus PVT-robust



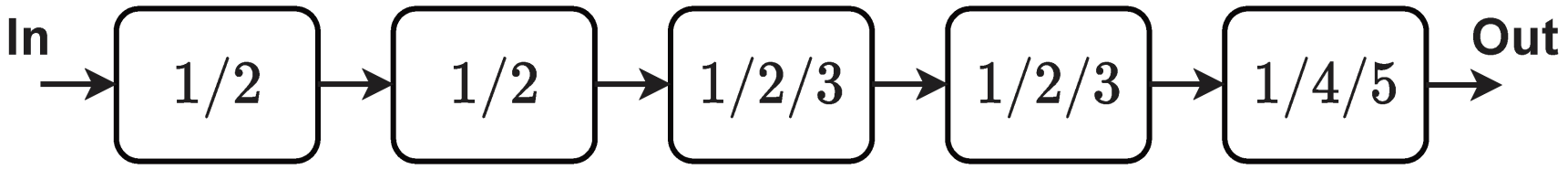
Complete frequency synthesizer design

- Passive second-order loop filter.
- Nominal design parameters:
  - Reference input = 50 MHz
  - Charge pump current = 10 μA
  - Loop bandwidth = 230 kHz.
- Dual output dividers allow generation of two programmable output frequencies.
- No external analog inputs required: all bias currents set by on-chip constant-G_m references via 5-bit current DACs
- All parameters set over a standard I^2C serial interface

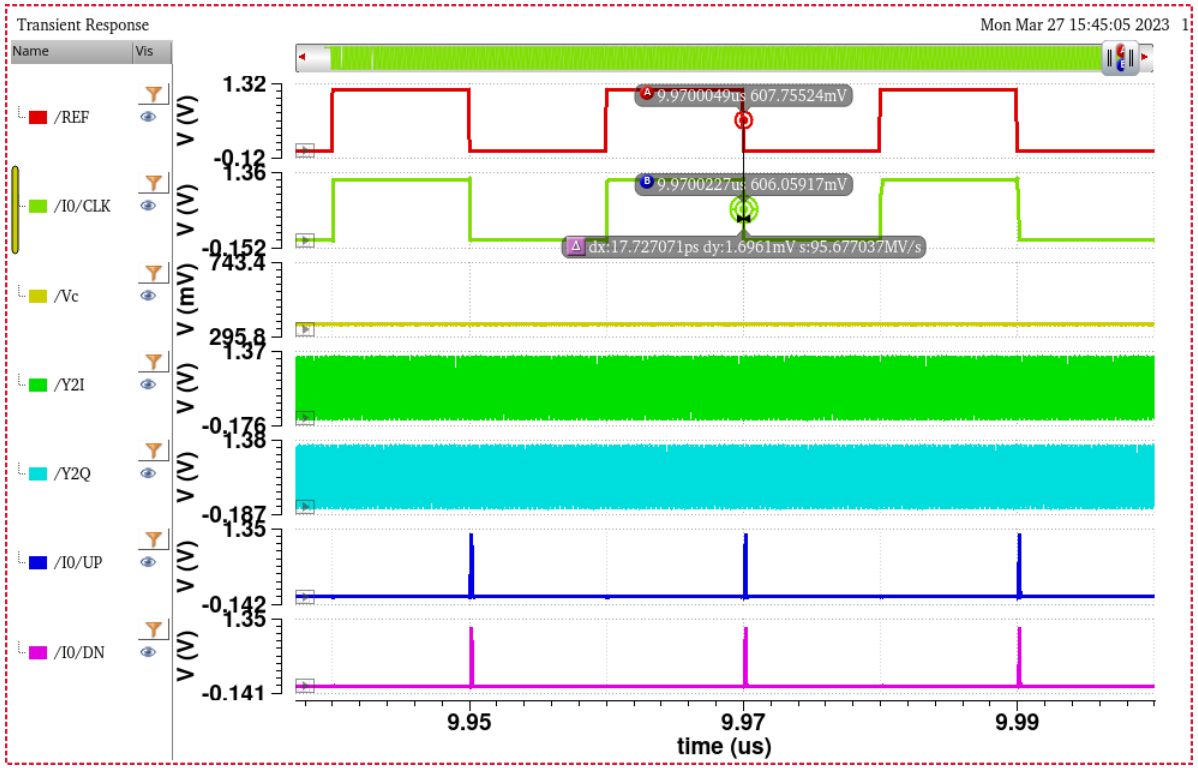


Programmable output divider

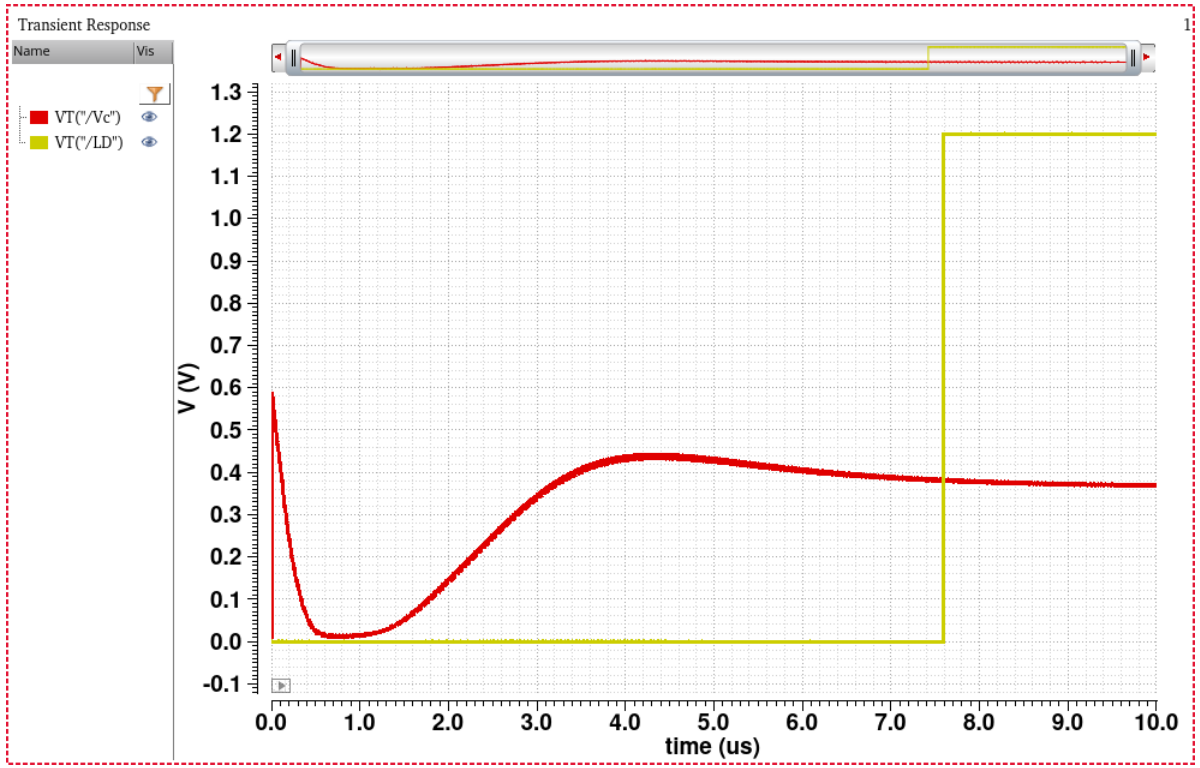
- Uses a cascade of stages with smaller division ratios.
- This allows a wide range of divide values (most composite numbers < 31) to be generated while maintaining an output duty cycle close to 50%.
- Stages are bypassed by transmission gate multiplexers when in “divide by 1” mode.



Simulation of the frequency synthesizer



Major waveforms, f_{OUT} = 6 GHz



VCO control voltage and LD signal

- Simulated behavior is in excellent agreement with the predicted loop dynamics.

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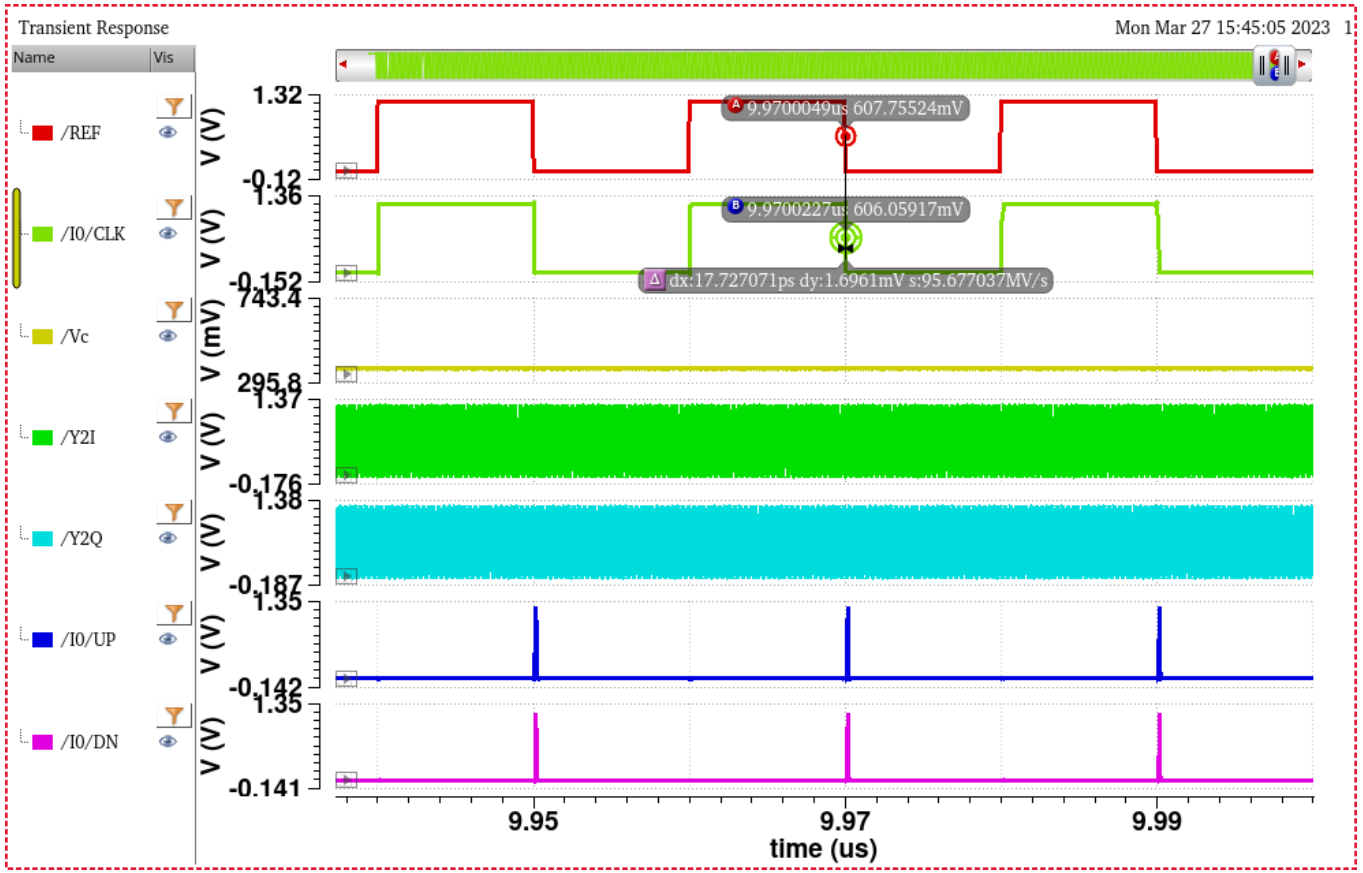
Simulation of the frequency synthesizer (2)

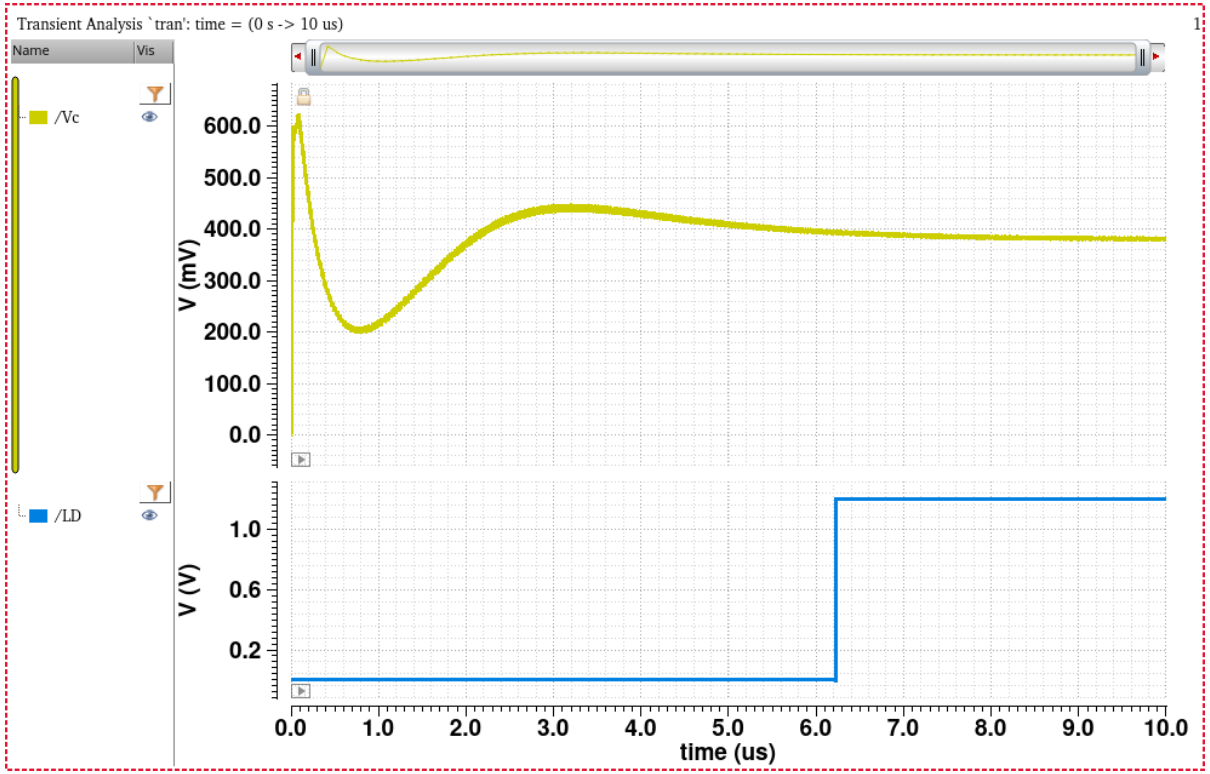


Zoomed-in view in steady-state conditions

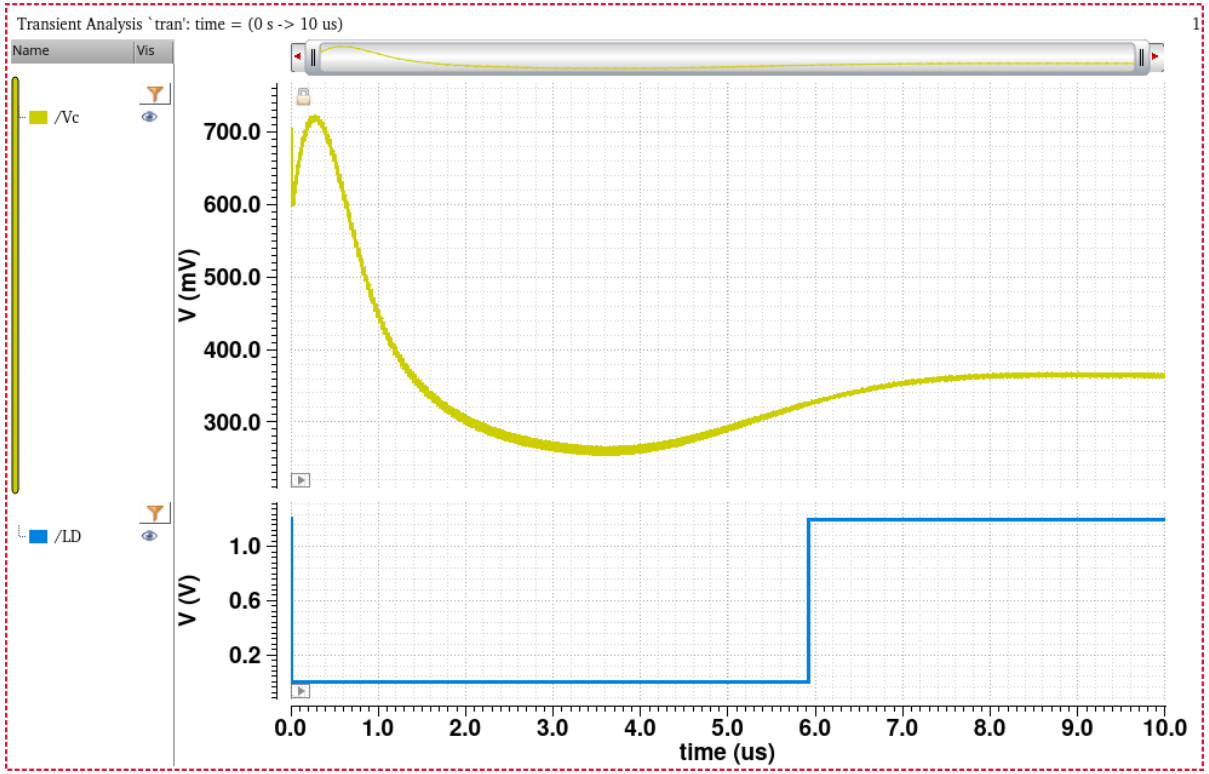
- The static timing error is negligible (~18 ps, 0.09% of T_{REF}) due to the use of replica-based self-biasing to equalize the positive and negative CP currents.

Simulation of the frequency synthesizer (3)

- Effect of process variations was studied by simulating using corner models.



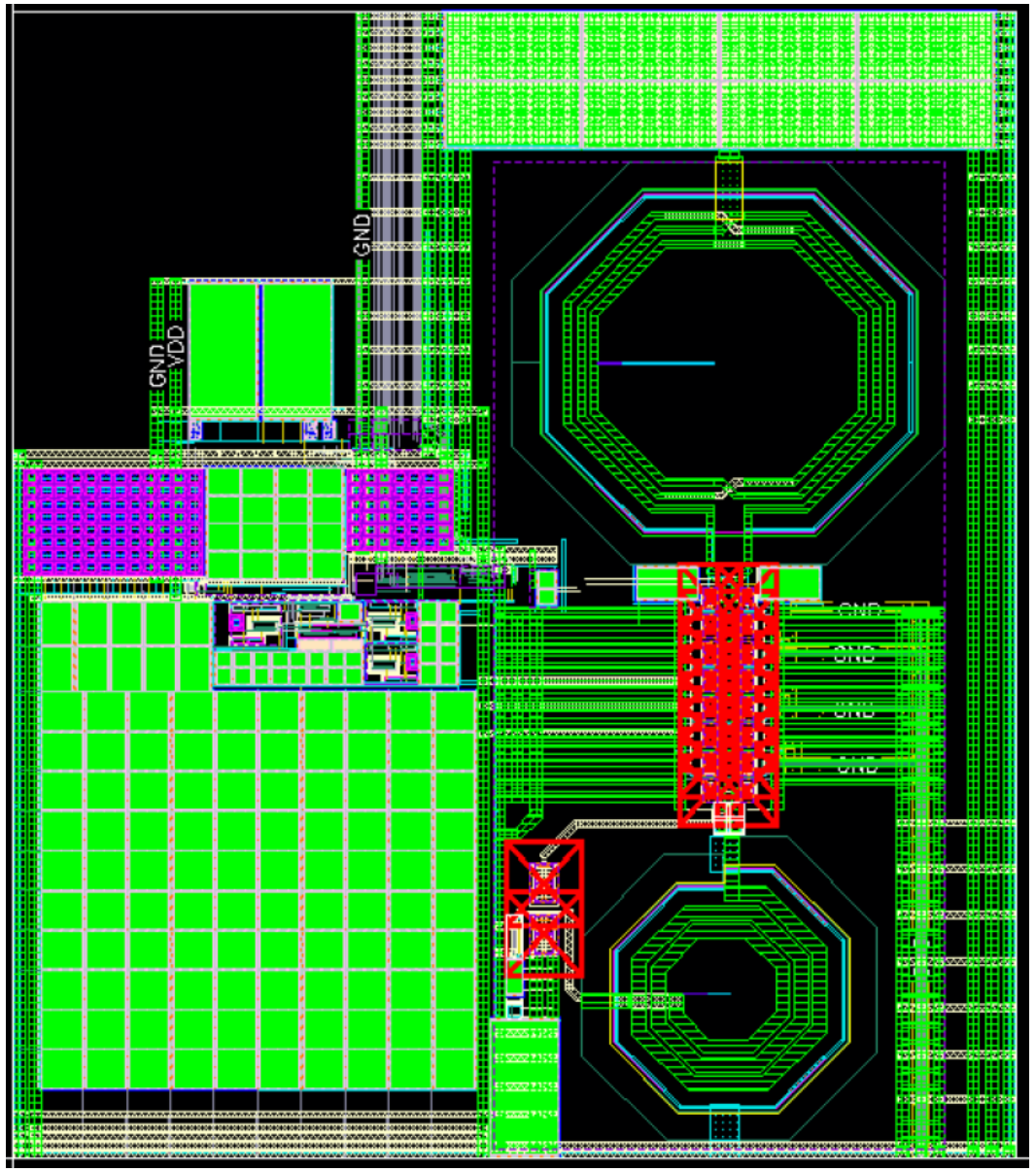
Fast N, Slow P (FNSP) corner



Slow N, Fast P (SNFP) corner

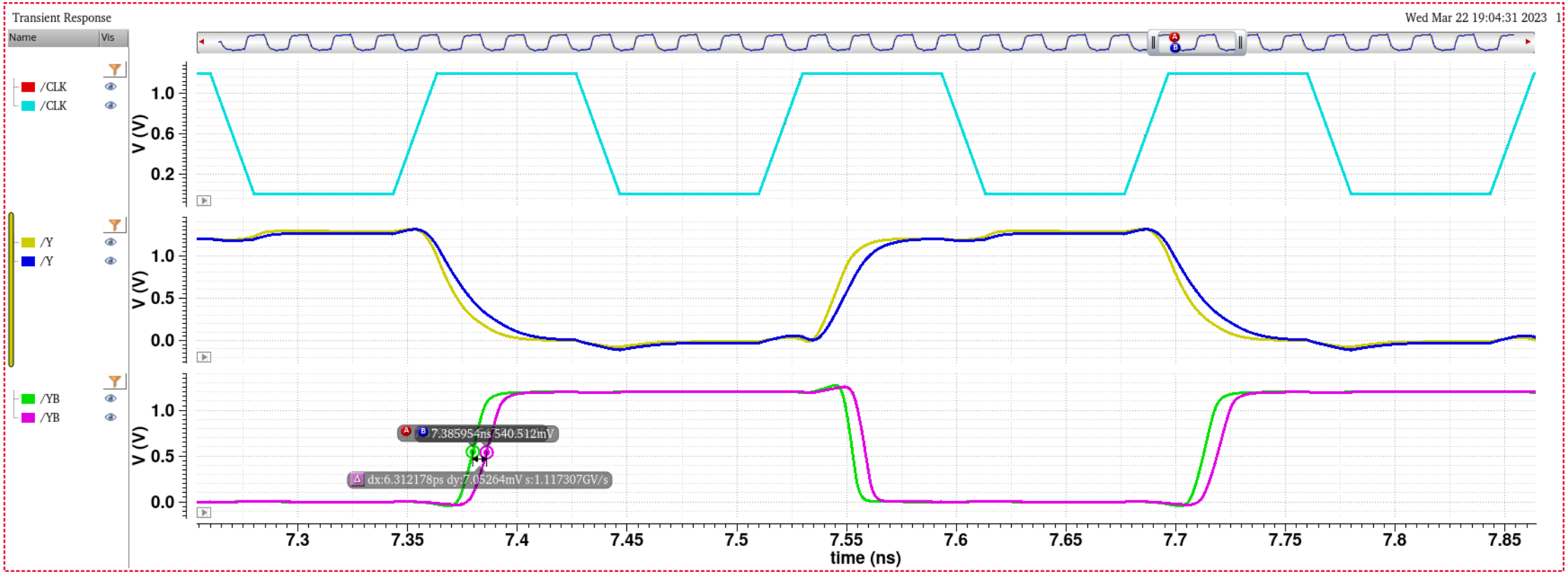
Layout of the frequency synthesizer

- Overall layout area: 450 µm x 500 µm
  - About 50% of the area is occupied by the VCO.
  - About 25% is occupied by the main loop filter capacitor.
- Nominal power consumption:
  - From V_{DD} = 1.2V (used by most circuits): 2.4 mA
  - From V_{DDL} = 0.8V (only used by the VCO): 1.45 mA
  - Total = 4.0 mW



Post-layout simulation of the TSPC divider

- No issues noticed while operating at 6 GHz (for all process corners).



Comparison of pre- and post-layout simulation results (tt corner)

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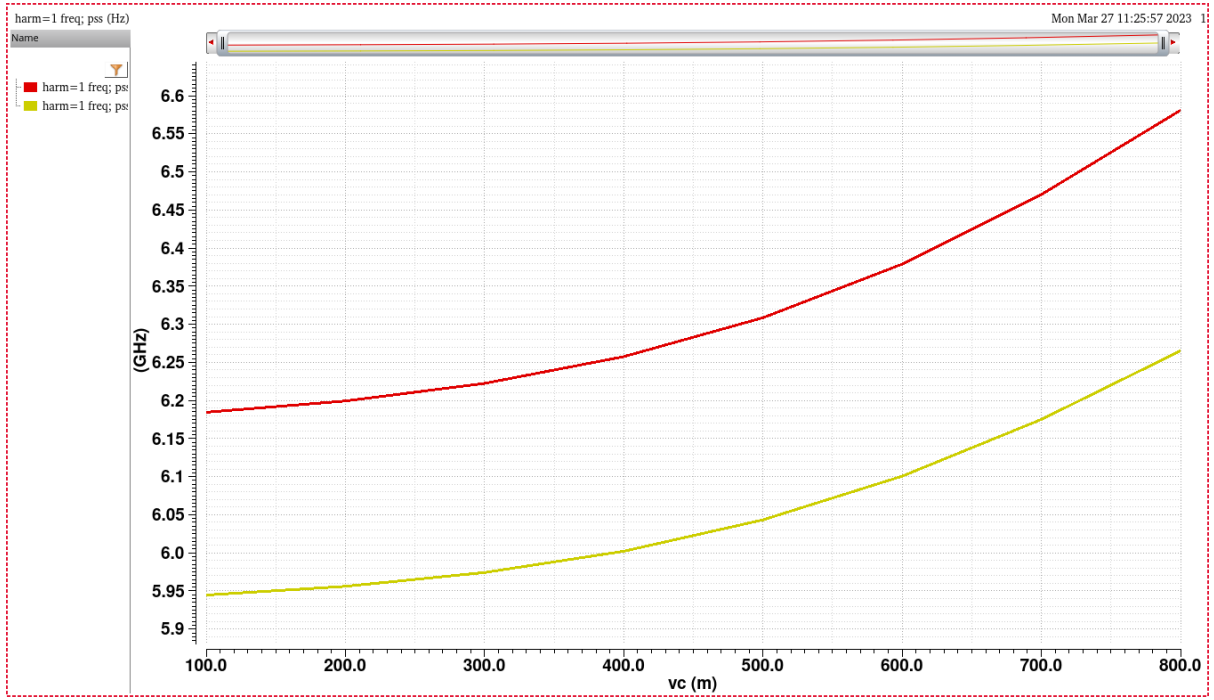
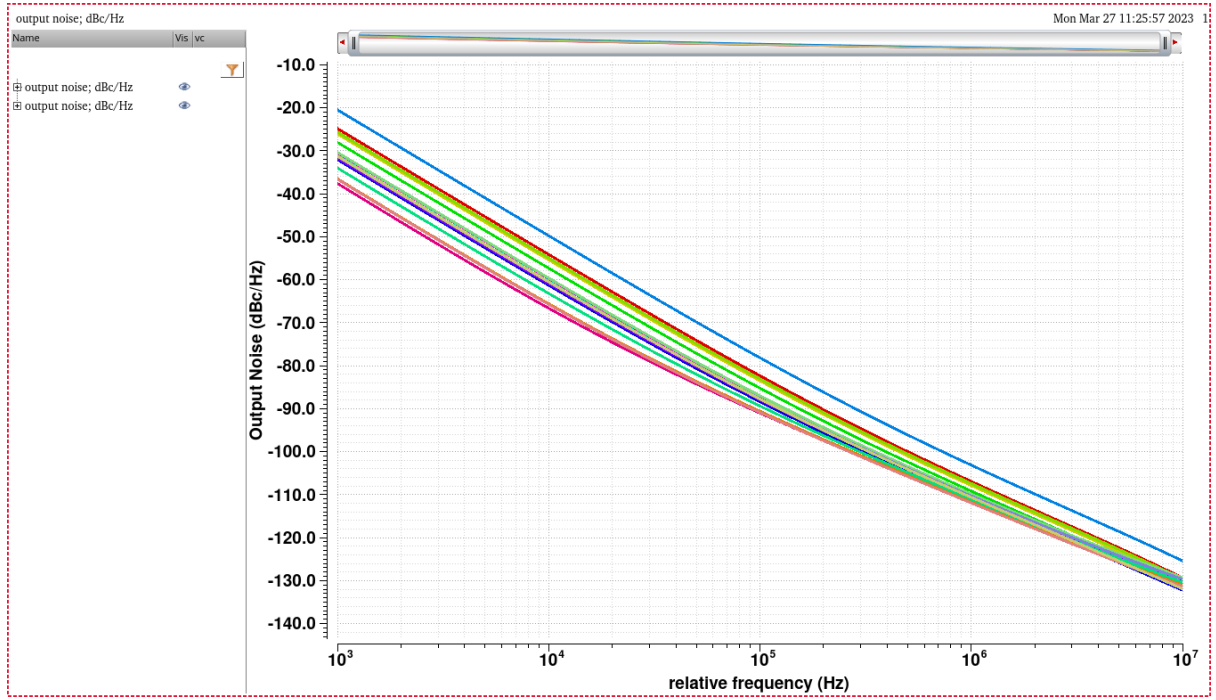
Post-layout simulation of the VCO

- No significant changes to oscillation frequency or phase noise (tt corner).
- Simulation accuracy may be limited by the fact that only *RC* extraction was performed (trace inductances were not extracted).



Tuning range for the two lowest bands



Phase noise for the two lowest bands

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Post-layout simulation of the whole synthesizer

- Output dividers were set to divide ratios of 2 and 4, respectively.
- Transient simulation in “conservative” mode took ~18.5 hours.

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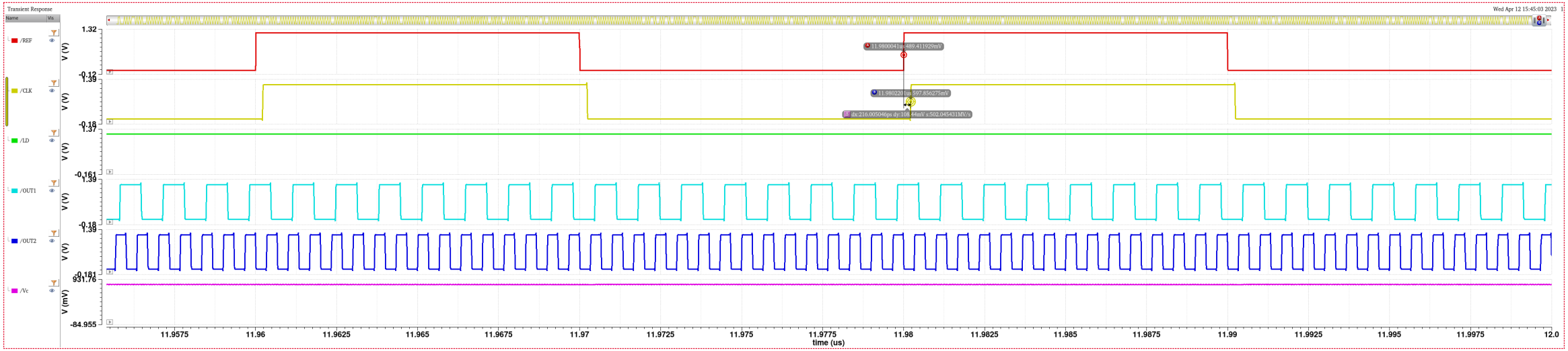

Zoomed-in view in steady-state conditions (after locking)

- Settling time is increased by cycle slips → suggests that the initial frequency offset increased due to a shift in the VCO’s free-running frequency compared to pre-layout simulations.
- A small static timing error (~200 ps, 1% of T_{REF}) is observed.

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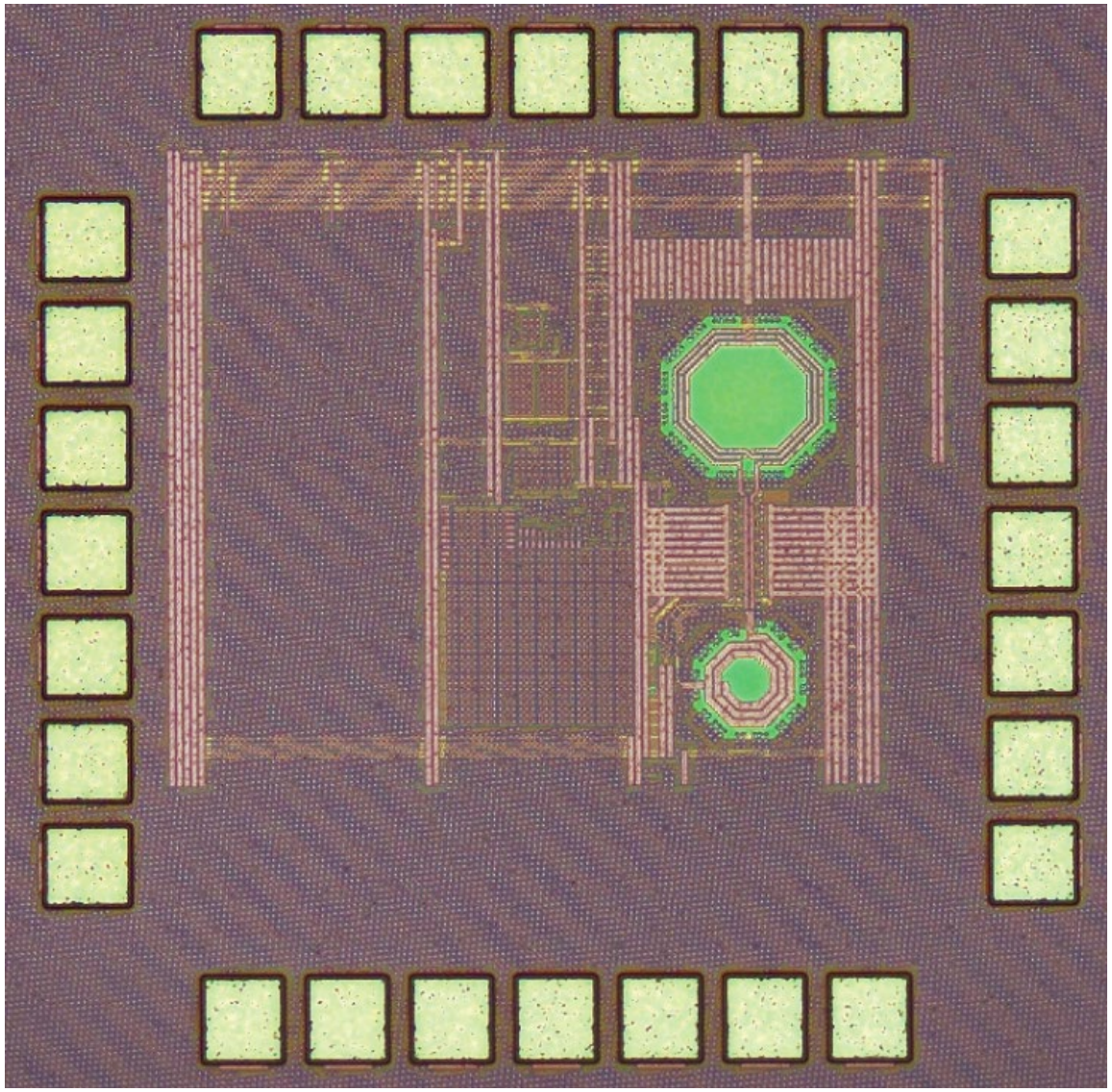
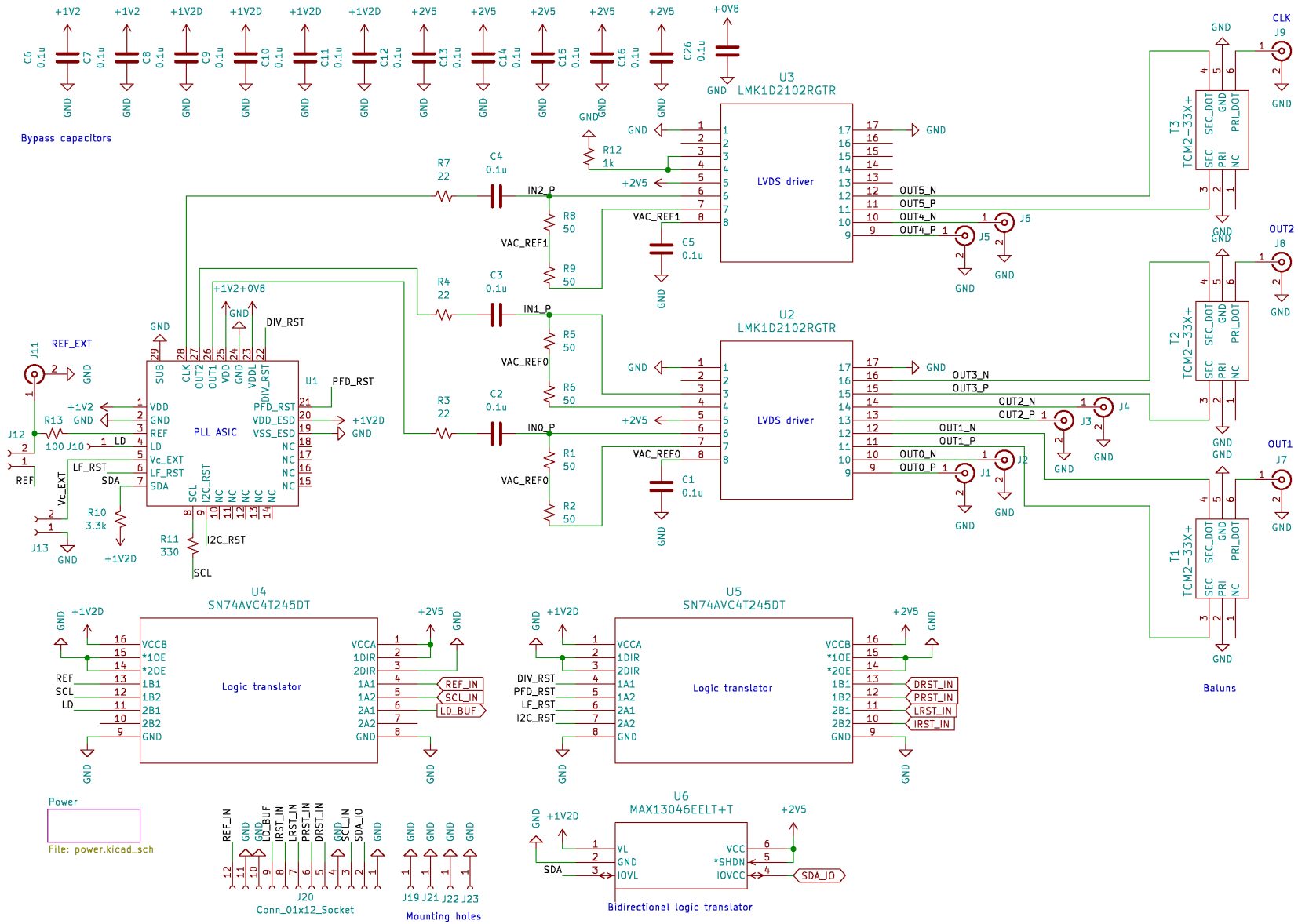
Die photograph



1 mm

Design of the test board (1)

- Simple design
- Allows chip to be programmed from a processor using 2.5V logic
- Differential outputs available from LVDS drivers
  - Drivers have a maximum specified data rate of 2 Gb/s
  - Baluns used to generate single-ended outputs from LVDS to simplify testing
- No impedance matching at the reference input due to its “low” frequency (<50 MHz)
  - This was not a good idea; external matching resistor had to be added later



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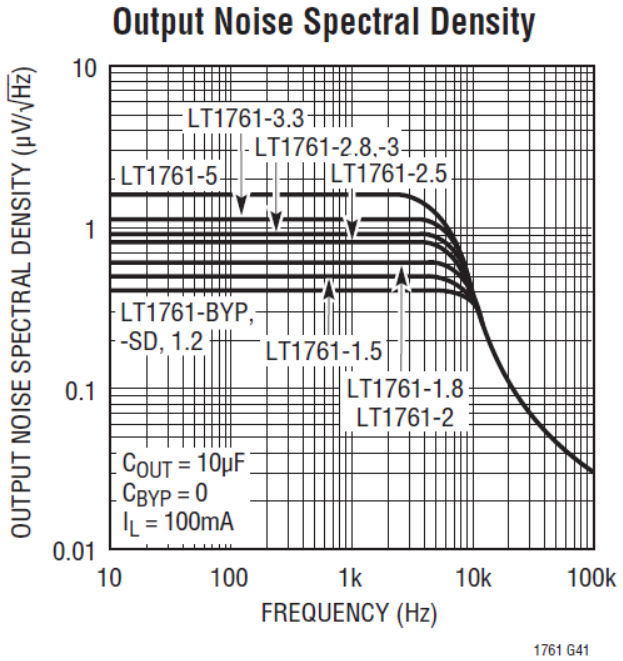
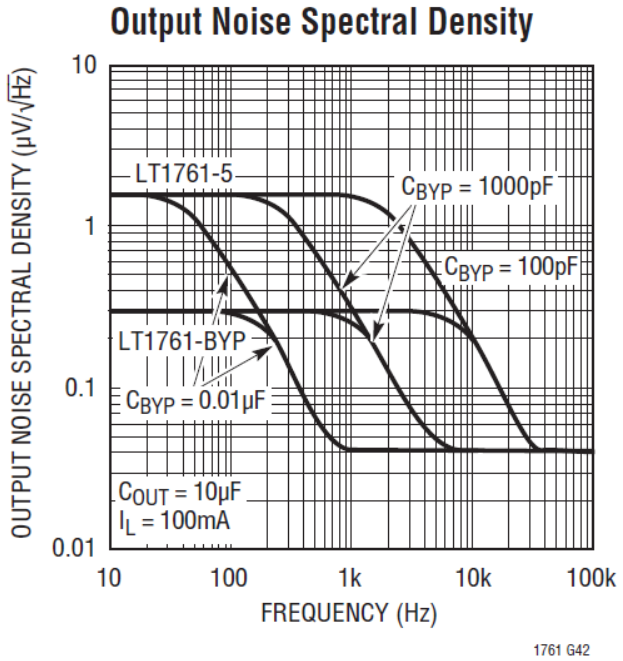
Design of the test board (2)

- The VCO power supply has a low value (~0.8V) and must also have extremely low noise to minimize phase noise due to supply modulation
- Most low-noise linear regulators set the output voltage by comparing a band-gap reference (V_{BG} ≈ 1.2V) with a fraction, α, of the output voltage (set by a resistive divider)
  - It is impossible to generate regulated outputs below V_{BG} ≈ 1.2V
  - Attenuation of α in the feedback path results in closed-loop gain of 1/α for reference noise, which thus tends to dominate the output noise PSD
  - Example: LT1761 low-noise micropower LDO (Analog Devices)



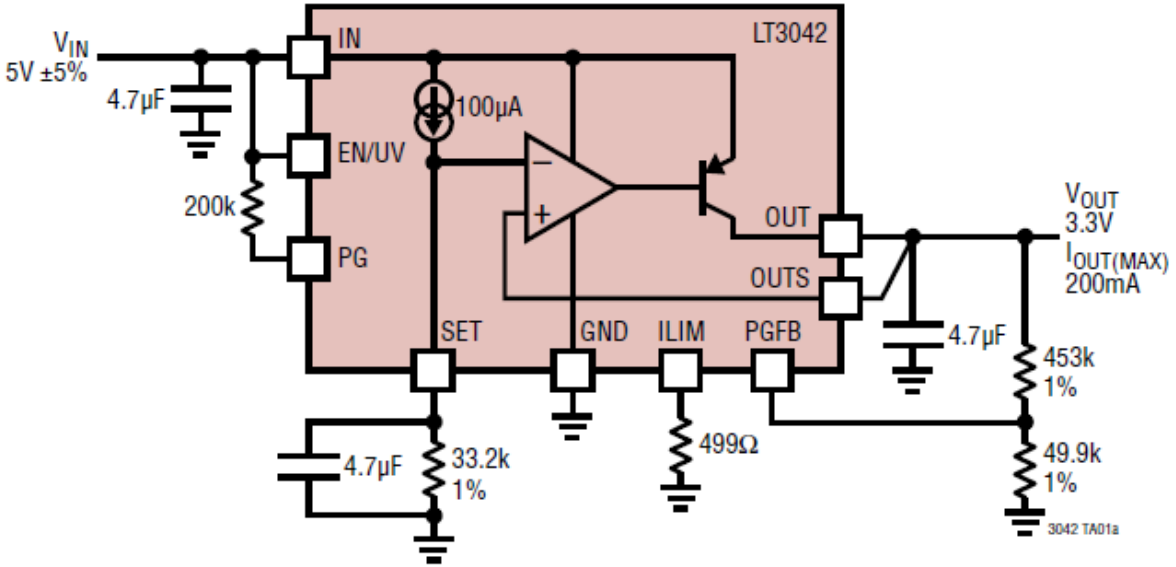


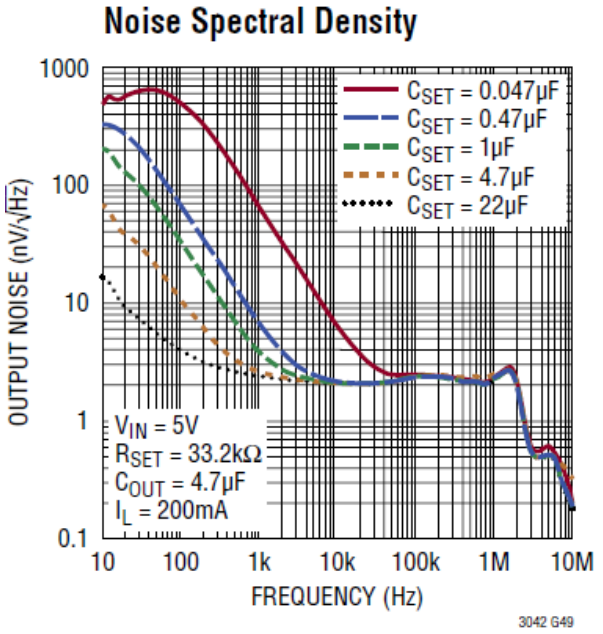
- Output noise PSD increases with output voltage → as expected for reference noise.
- Total integrated (rms) noise can be decreased by using a bypass capacitor, C_{BYP}, to low-pass filter the reference noise.
- Nevertheless, the low-frequency noise (which translates to close-in phase noise) remains poor → about 300 $nV/Hz^{1/2}$ for V_{OUT} = 1.2V

Source: LT1761 data sheet

Design of the test board (3)

- Obtaining a regulated supply voltage with significantly lower noise requires a different regulator architecture.
- Example: LT3042 (Analog Devices)
  - Replaces the voltage reference with a low-noise current reference, which drives an external resistor that sets the output voltage
  - Allows the output voltage to be regulated all the way to zero by a unity-gain buffer
  - Eliminates multiplication of reference noise at the output terminal

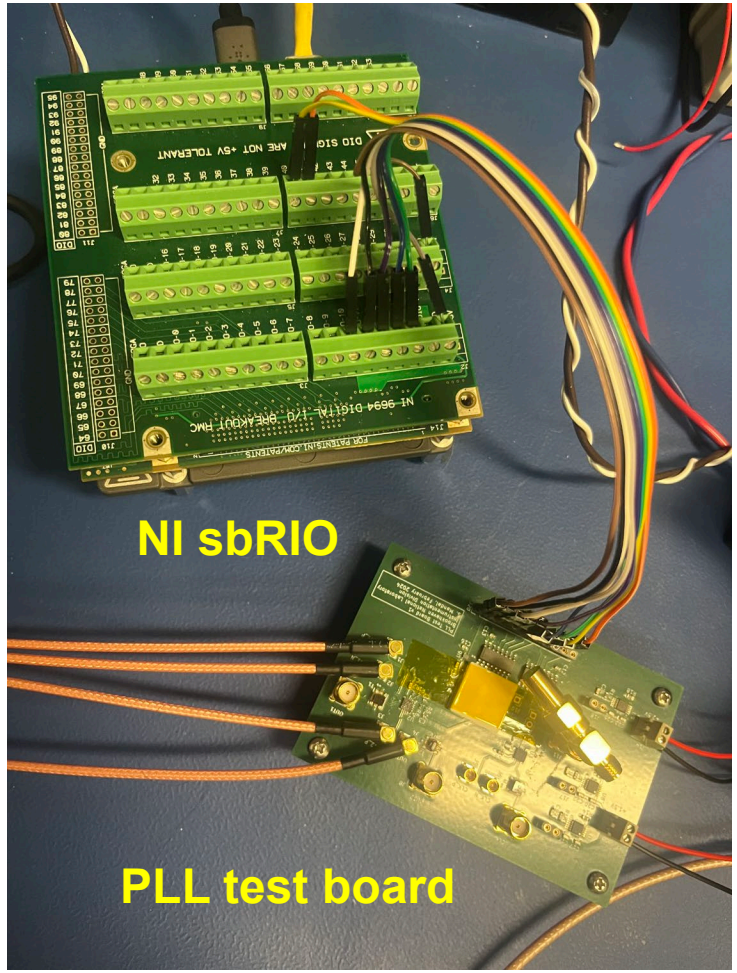


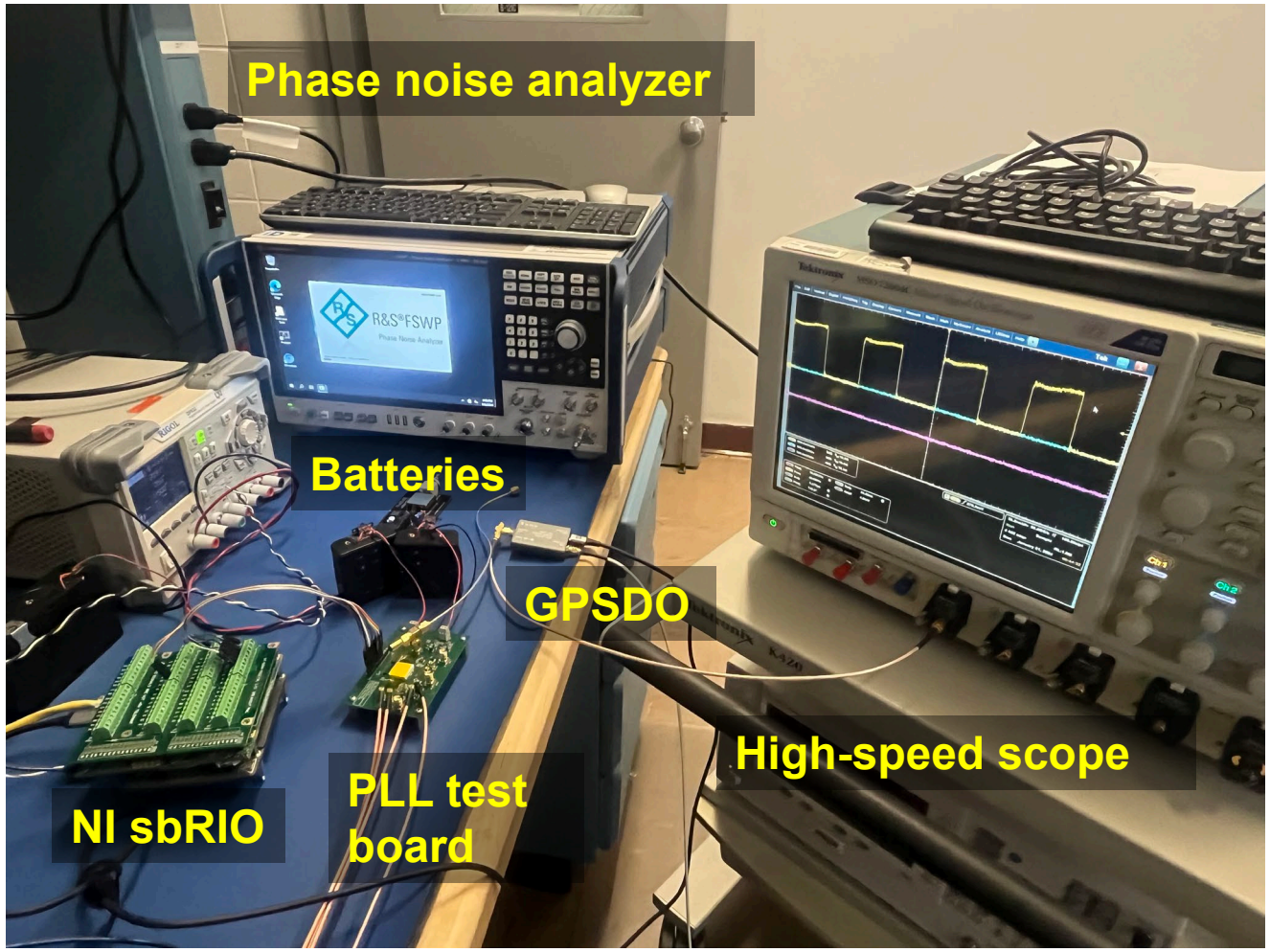


- Greatly improved low-frequency noise → for C_{SET} = 22 µF, ~2 nV/Hz$^{1/2}$ above 200 Hz

Source: LT3042 data sheet

Test setup





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Control application

- Developed by Piotr Maj (BNL)
  - Allows all parameters to be set over I^2C from a NI sbRIO board
  - Reports PLL status via the lock detect (LD) signal
  - Also reports locking time (in units of the FPGA clock period of 25 ns)
- Testing revealed that all reset signals (DIV_RST, PFD_RST, LF_RST, and I2C_RST) must be actively pulled low → logic translator inputs drift high when they are left floating

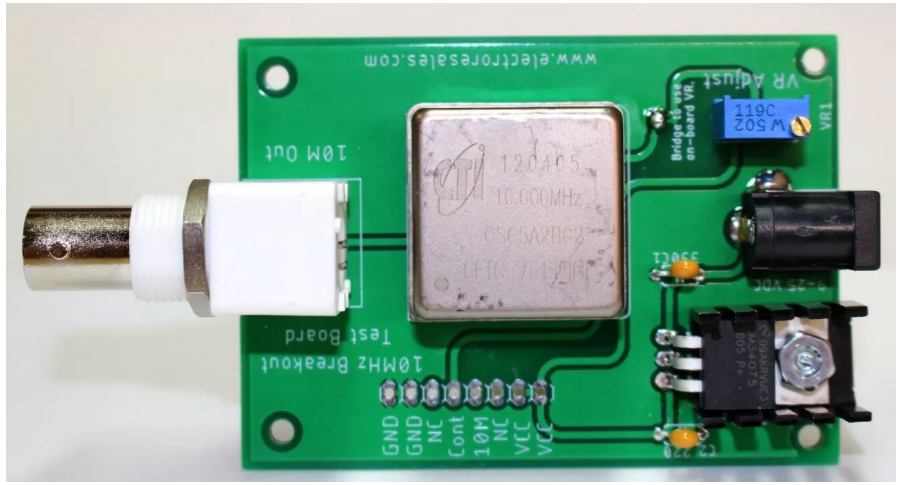
$$f_{VCO} = f_{REF} N_{tot} = f_{REF} \times 8 \times (NP + S)$$

$$f_{OUT} = \frac{f_{VCO}}{2M}$$

Output divide ratio

Conclusions from initial testing

- PLL operates as expected, but output jitter dominated by the reference (a function generator)
  - Estimating the added jitter requires a low-jitter reference source
- Option 1: Low-cost OCXO ($25 on eBay)
  - Output frequency is fixed at 10 MHz
- Option 2: Moderate-cost GPSDO ($150 from Leo Bodnar Electronics)
  - Preferred since the output frequency is adjustable over a broad range using an internal multi-loop analog-digital PLL that multiplies the output of the internal TCXO
  - However, requires access to a room with a sky view to allow locking to GPS

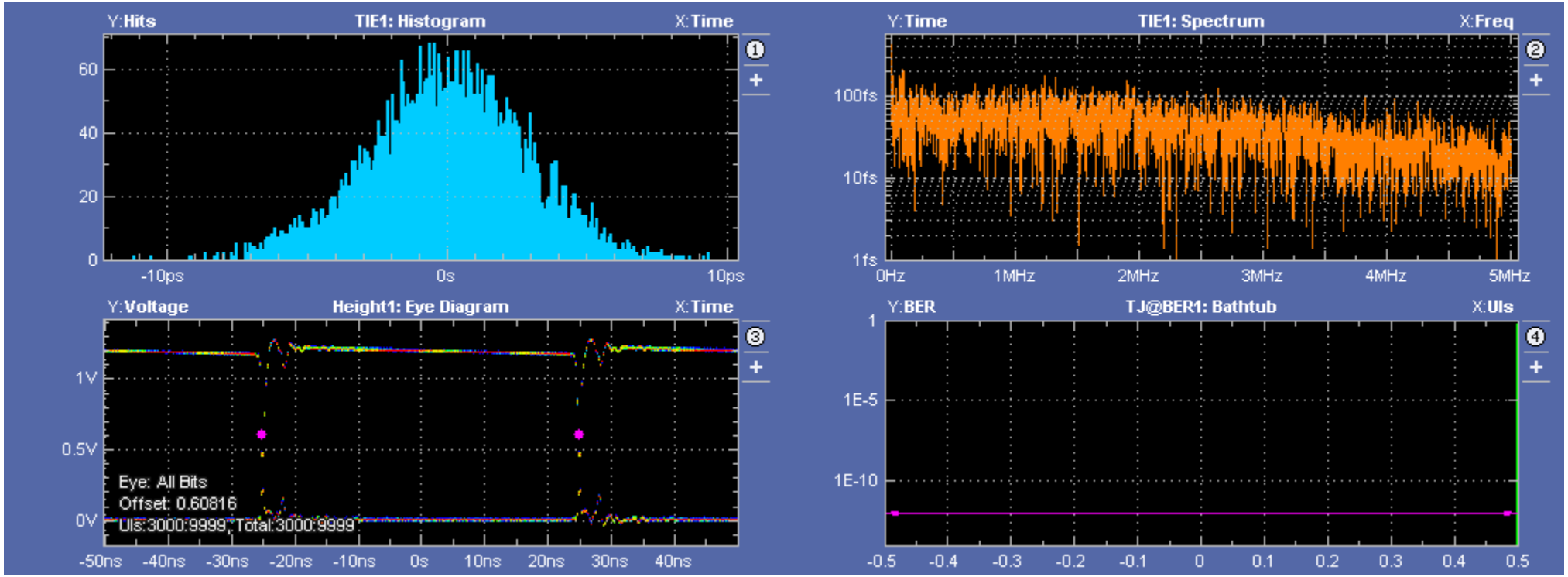


OCXO

GPSDO

Jitter measurements: Reference input

- Reference source: CTI OCXO @10 MHz
- OCXO output is ~5Vpp into a 50 Ω load, has to be attenuated before feeding the chip
- Significantly lower jitter than the function generator



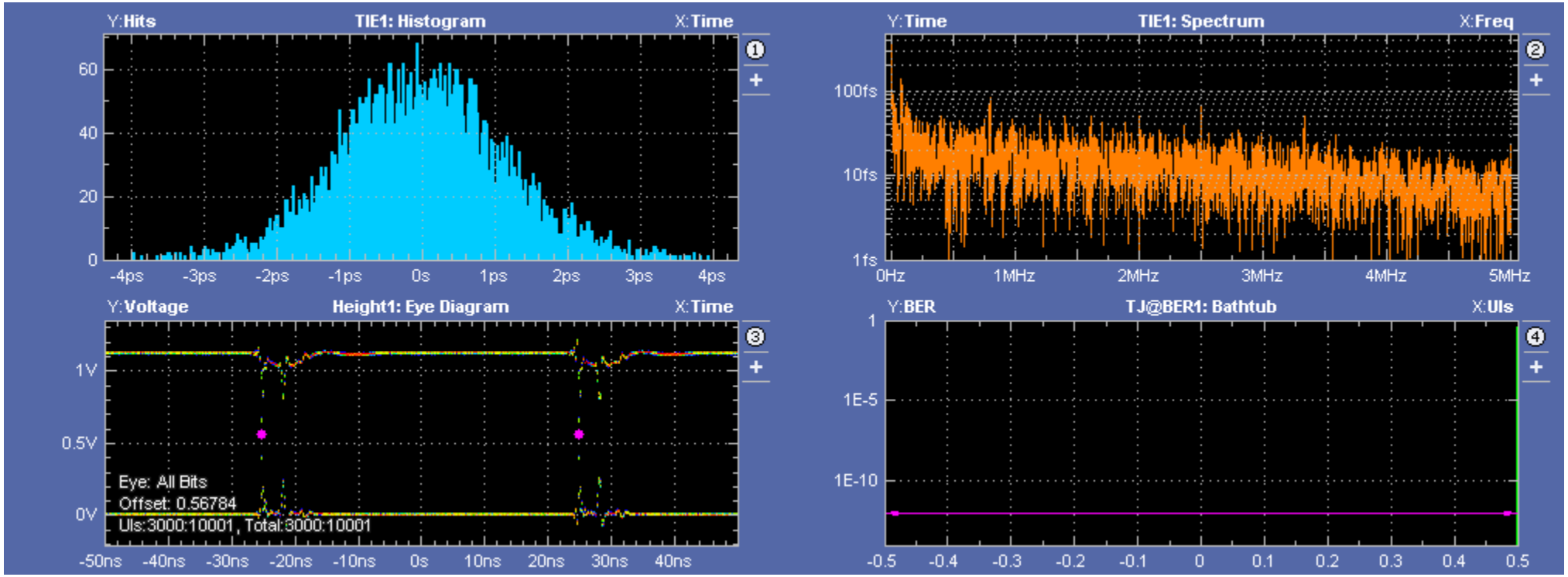
RMS jitter = 2.9 ps, Peak-peak jitter = 21.7 ps

Using the GPSDO

- Availability of an active GPS antenna (with built-in preamp) allows the antenna to placed quite far from the GPSDO
  - Connection uses ~8 m of coaxial cable
  - Enables the antenna to be placed near a window, thus ensuring a good sky view

Jitter measurements: Reference input

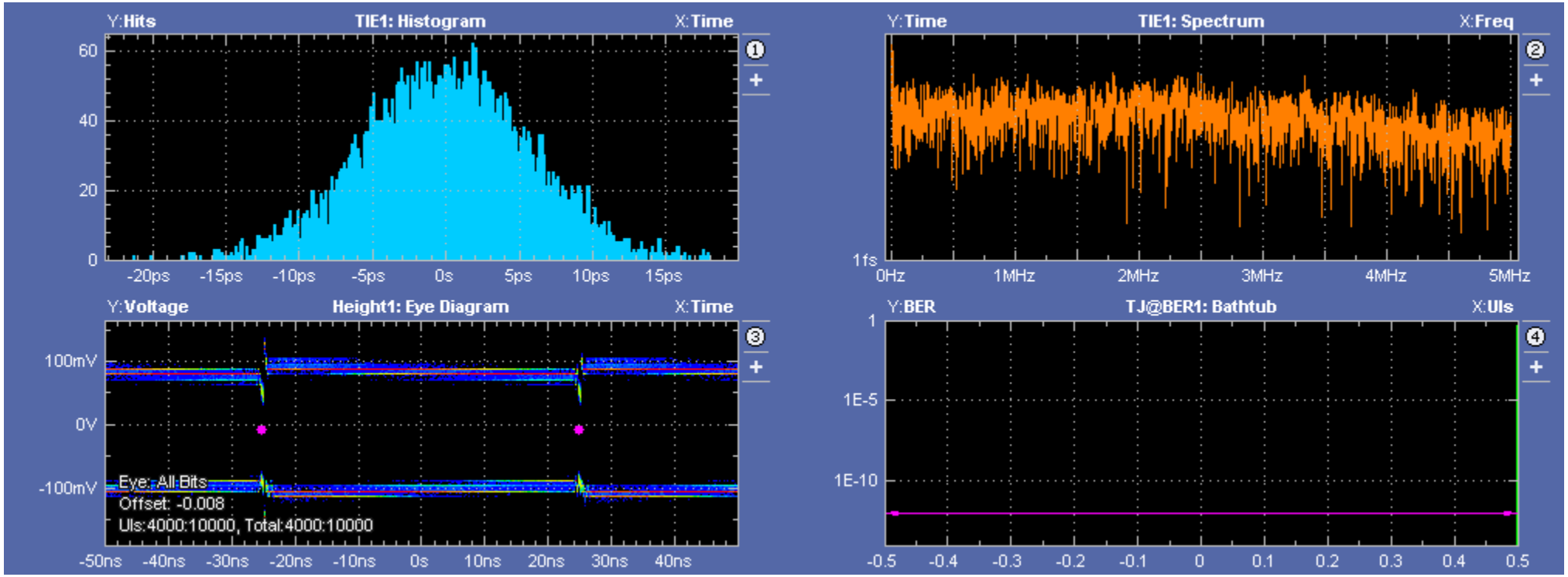
- Reference source: Leo Bodnar GPSDO @10 MHz
- GPSDO output is ~3.3Vpp into a 50 Ω load, has to be attenuated before feeding the chip
- Output jitter is ~2.5x better than the OCXO at the same frequency



RMS jitter = 1.1 ps, Peak-peak jitter = 7.9 ps

Jitter measurements: Recovered clock

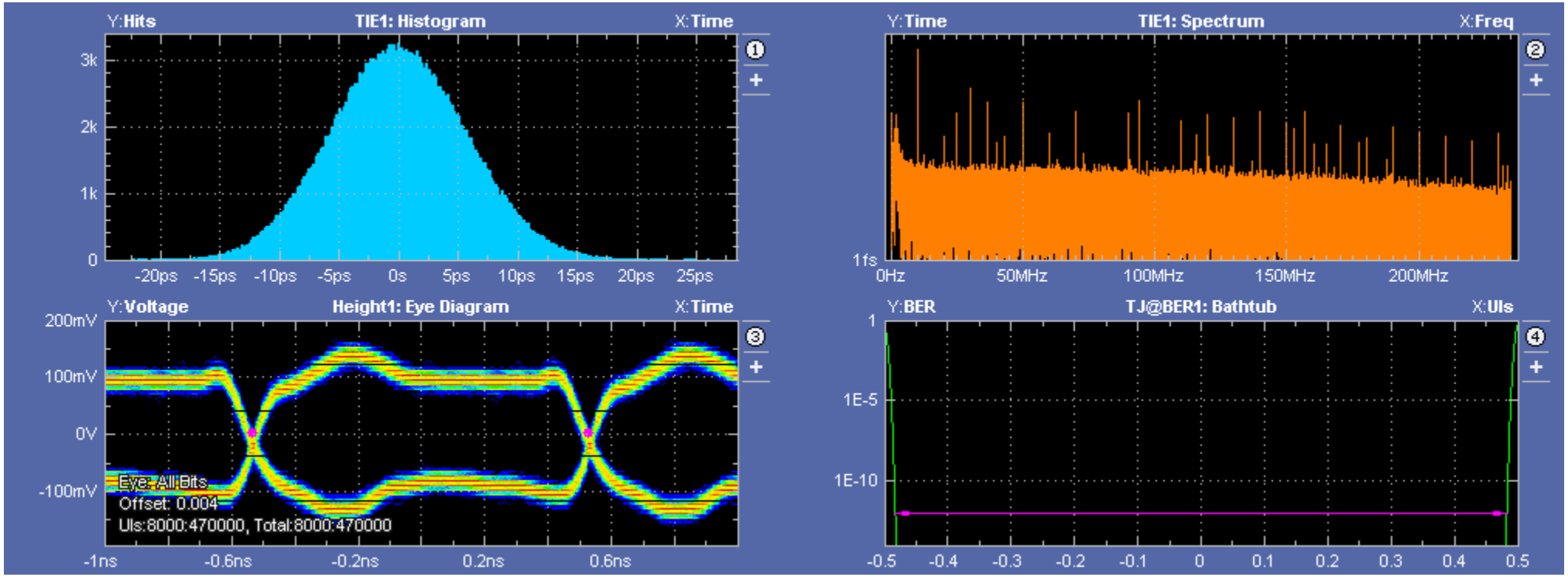
- Reference source: Leo Bodnar GPSDO @10 MHz
- Output jitter is ~5x larger than that of the reference
- Output jitter does not change significantly if board is powered using benchtop DC power supplies rather than batteries → on-board LDOs have good PSRR



RMS jitter = 5.7 ps, Peak-peak jitter = 39.3 ps

Jitter measurements: Output 1 (M = 8, 480 MHz)

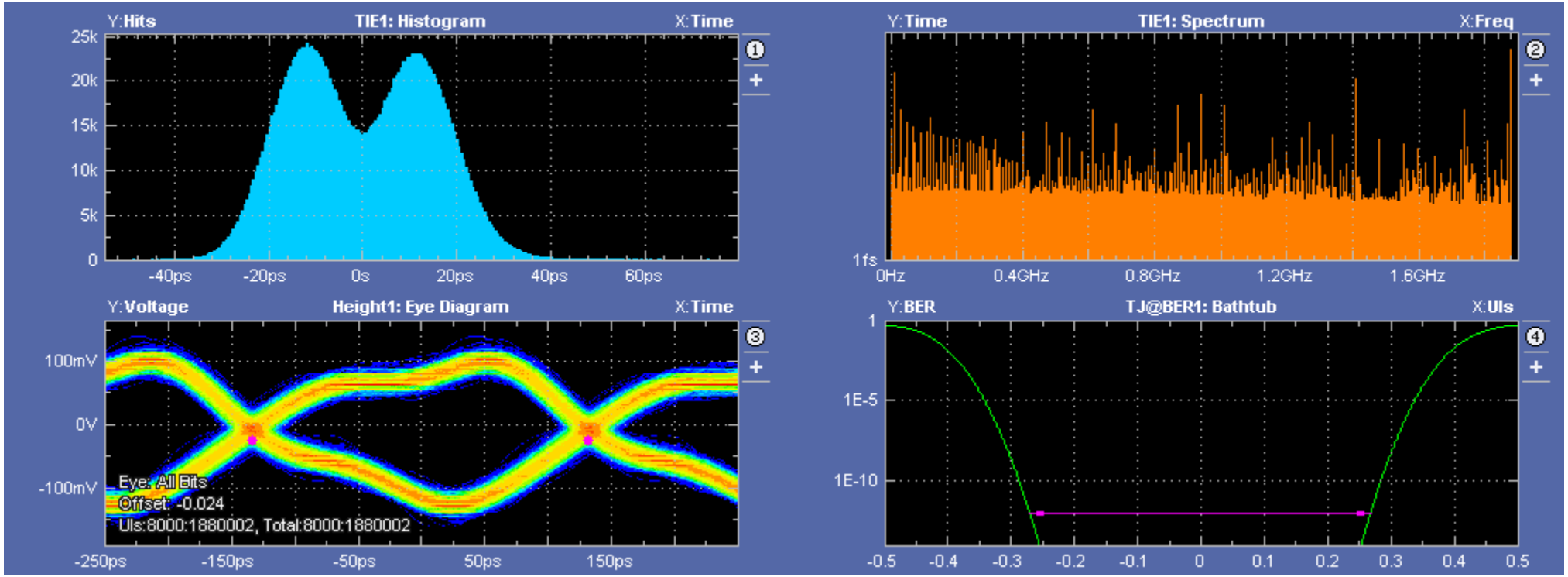
- Reference source: Leo Bodnar GPSDO @10 MHz
- Overall jitter is similar to that obtained with the OXCO, showing that the contribution of the reference to output jitter is relatively small



RMS jitter = 5.7 ps, Peak-peak jitter = 48.4 ps

Jitter measurements: Output 2 (M = 2, 1.92 GHz)

- Reference source: Leo Bodnar GPSDO @10 MHz
- Peak-to-peak jitter increases due to asymmetry between the rising and falling edges, which is determined by the on-board LVDS driver and not the PLL



RMS jitter = 14.6 ps, Peak-peak jitter = 122.4 ps

Summary of jitter measurements

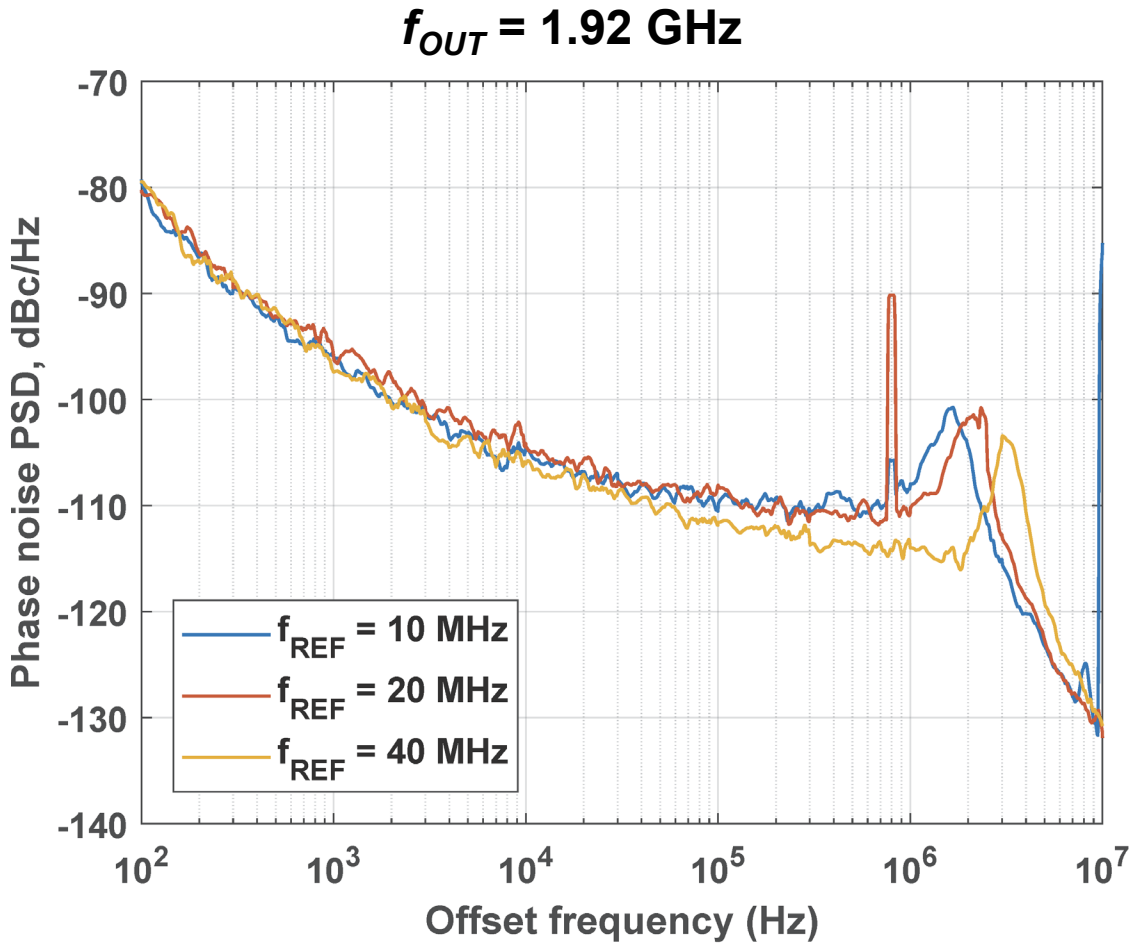
- Reference source: Leo Bodnar GPSDO
- Jitter decreases with increase in f_{REF} due to the smaller multiplication factor for input-reference noise sources (reference, divider, etc.).

Measured jitter: rms | peak-to-peak

f_{REF} (MHz)	Reference (ps)		Recovered clock (ps)		f_{OUT} = 480 MHz (ps)		f_{OUT} = 1.92 GHz (ps)	
10	1.1	7.9	5.7	39.3	5.7	48.4	14.6	122.4
20	1.5	10.6	5.4	40.5	4.9	49.8	10.0	80.3
40	1.25	10.4	5.1	37.6	4.7	38.7	9.5	74.5

Phase noise measurements

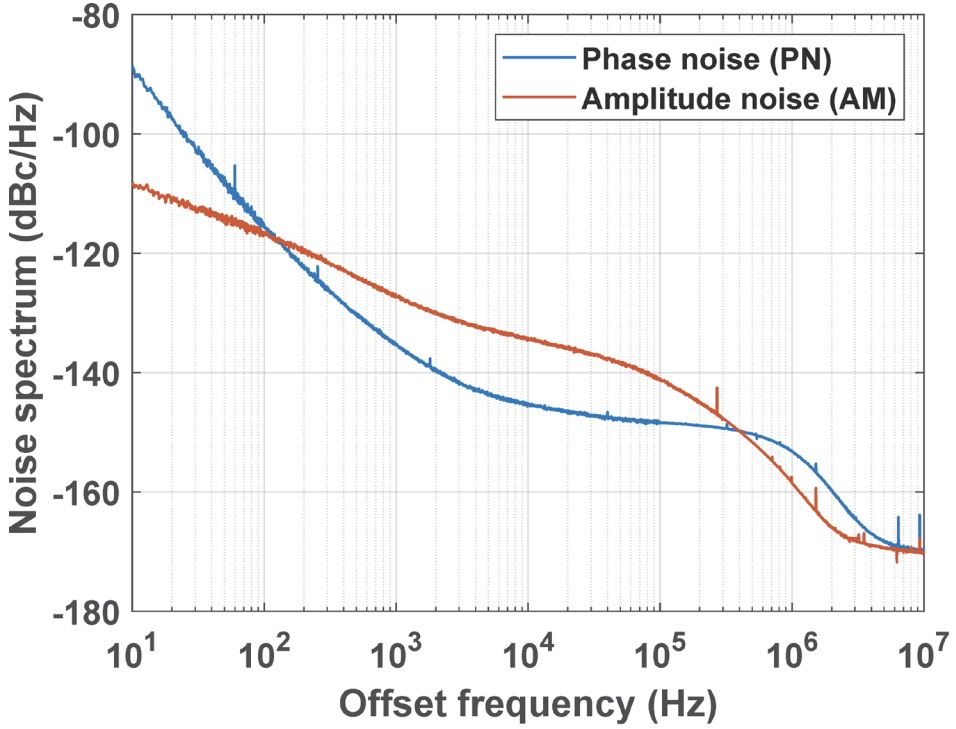
- Phase noise measured at different reference frequencies using a spectrum analyzer (Rohde & Schwarz FSW)
- Increase in reference frequency reduces the feedback division ratio, resulting in
  - Increased loop gain and closed-loop bandwidth
  - Reduced multiplication of reference phase noise



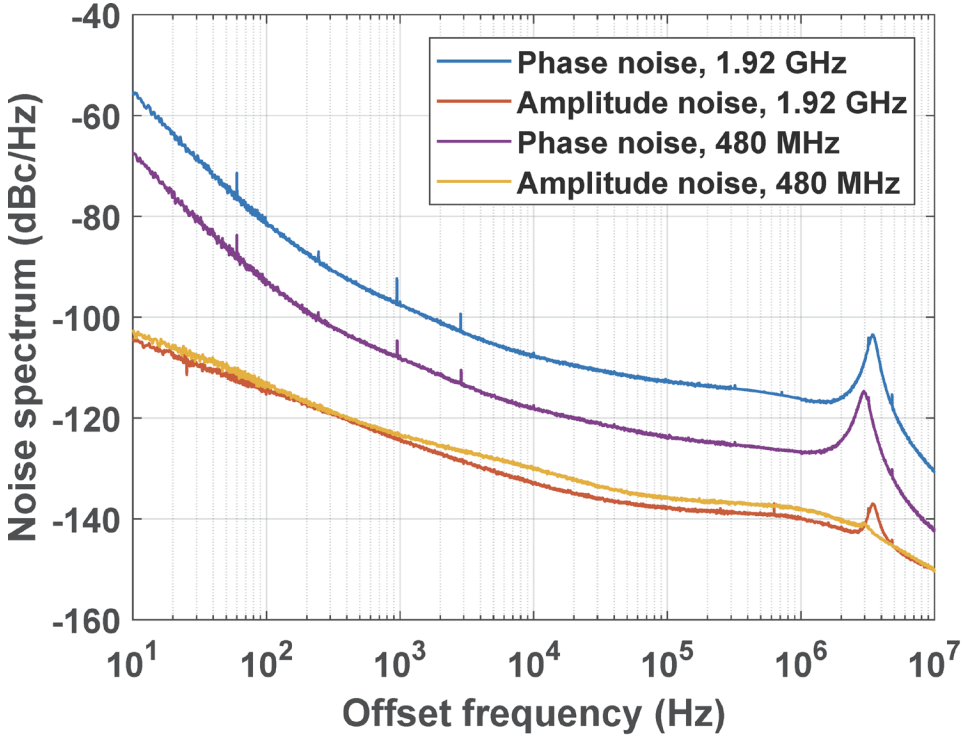
Phase noise measurements (2)

- Measurements repeated using a dedicated phase noise analyzer (Rohde & Schwarz FSWP)
  - Uses the cross-spectrum method to suppress internal noise sources
  - Can separate noise into phase and amplitude components
  - Reduces both the noise floor and trace variance (DANL) for a given total measurement time

Reference noise, GPSDO @ 40 MHz



Output noise, f_{REF} = 40 MHz



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Rubiola, Enrico, and François Vernotte. "The cross-spectrum experimental method." *arXiv:1003.0113* (2010).

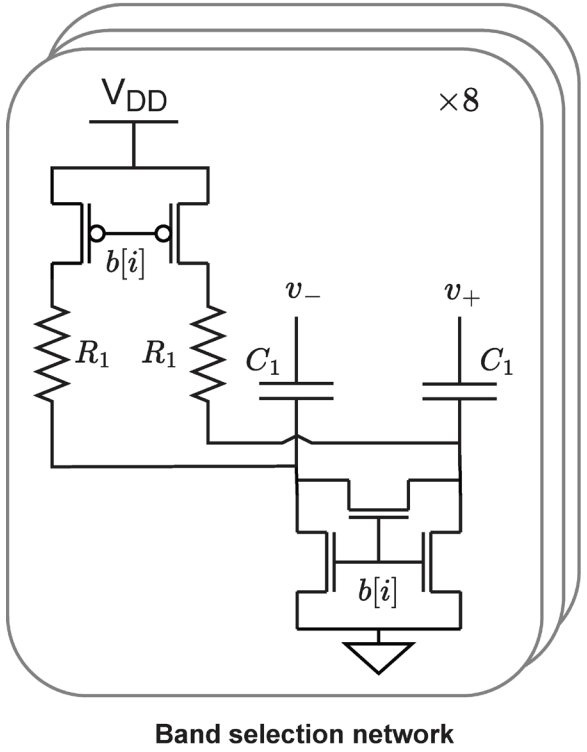
Conclusions and future work

- An integer-N synthesizer suitable for flexible on-chip clock generation has been designed and tested at 300K
  - Jitter and phase noise performance is suitable for downlink data transmission up to 3 Gb/s
  - Tests only carried out till an output frequency of 1.92 GHz due to the limited data rate of external LVDS drivers
- Modification of the test board to permit cryogenic operation is underway
  - Requires LDOs to be moved outside the cryostat and/or design of custom LDOs without built-in thermal shutdown circuits
  - Similar approach was recently used to test a quadrature *LC* VCO down to 8K

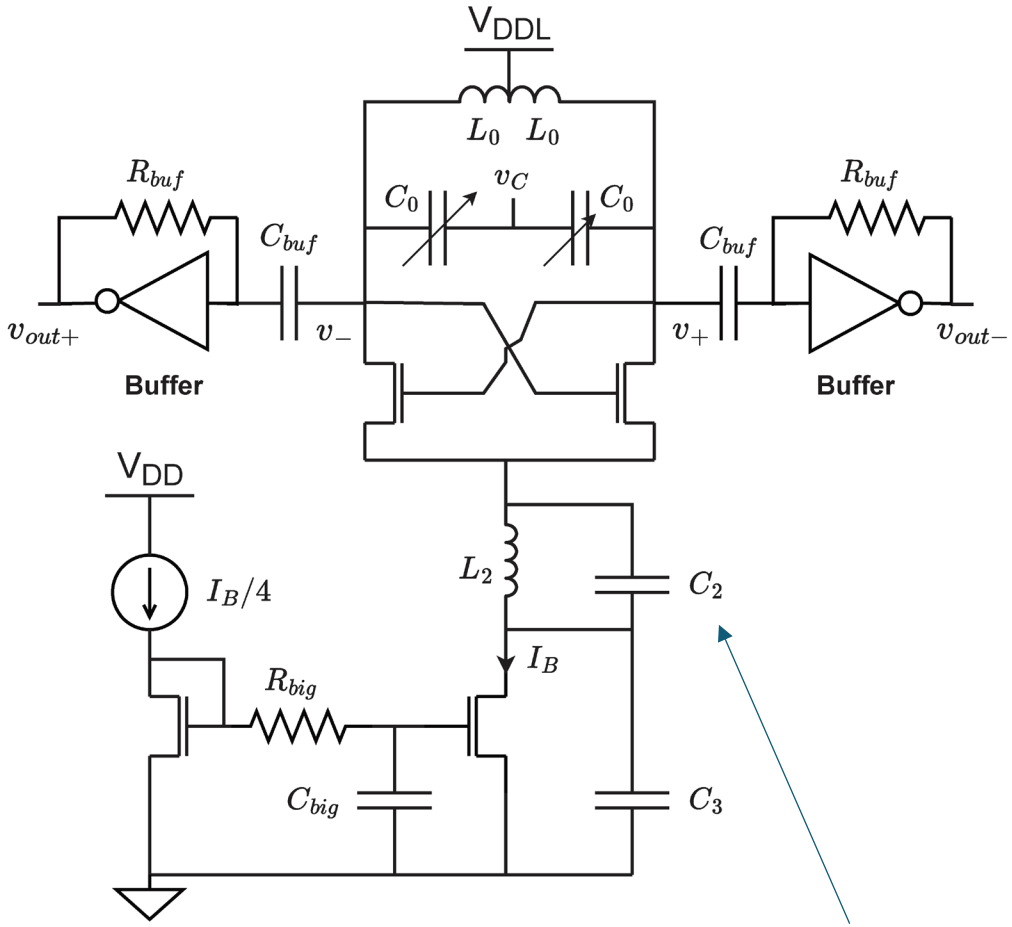
Backup slides

Improved VCO design

- Switch, resistor, and varactor sizes optimized to reduce phase noise while maintaining sufficient tuning range.
- A tail current *LC* filter (tuned to $2f_0$) reduces $1/f$ noise up-conversion but at the cost of additional layout area.



Band selection network

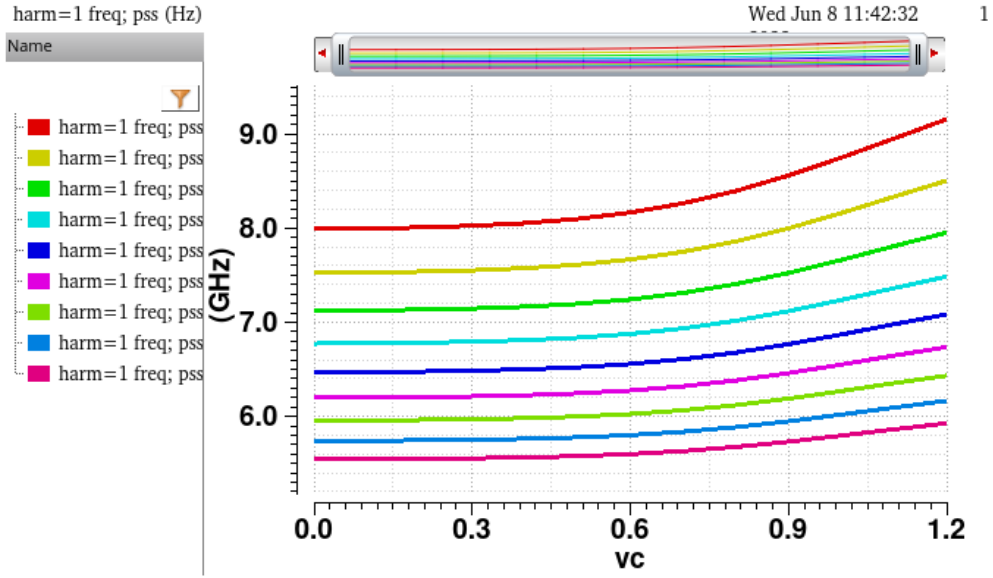


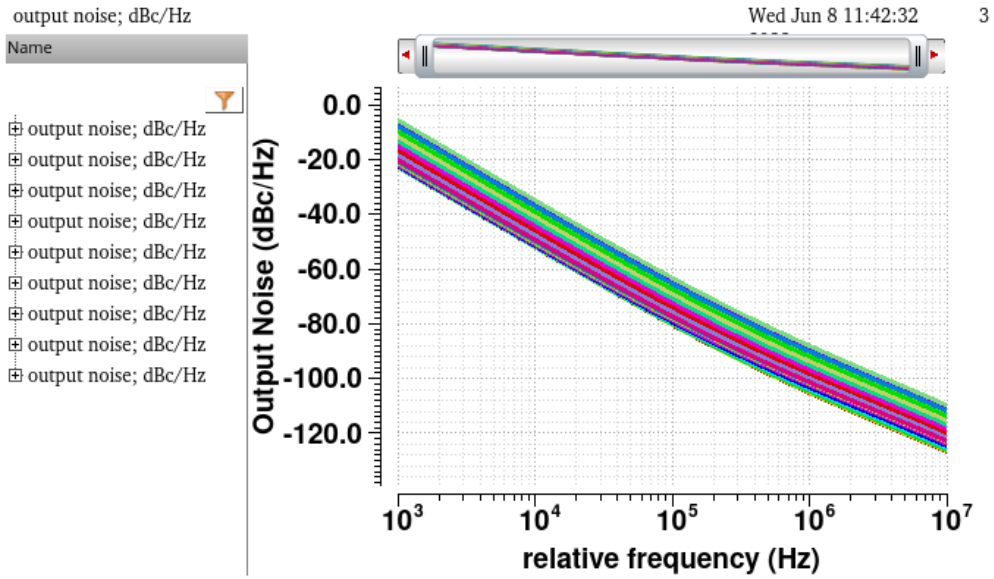
LC filter to reduce $1/f$ noise up-conversion

Hegazi, E., Sjoland, H., & Abidi, A. A. (2001). A filtering technique to lower LC oscillator phase noise. *IEEE Journal of Solid-State Circuits*, *36*(12), 1921-1930.

VCO simulation (V_{DDL} = 0.8 V, I_B = 1.6 mA)

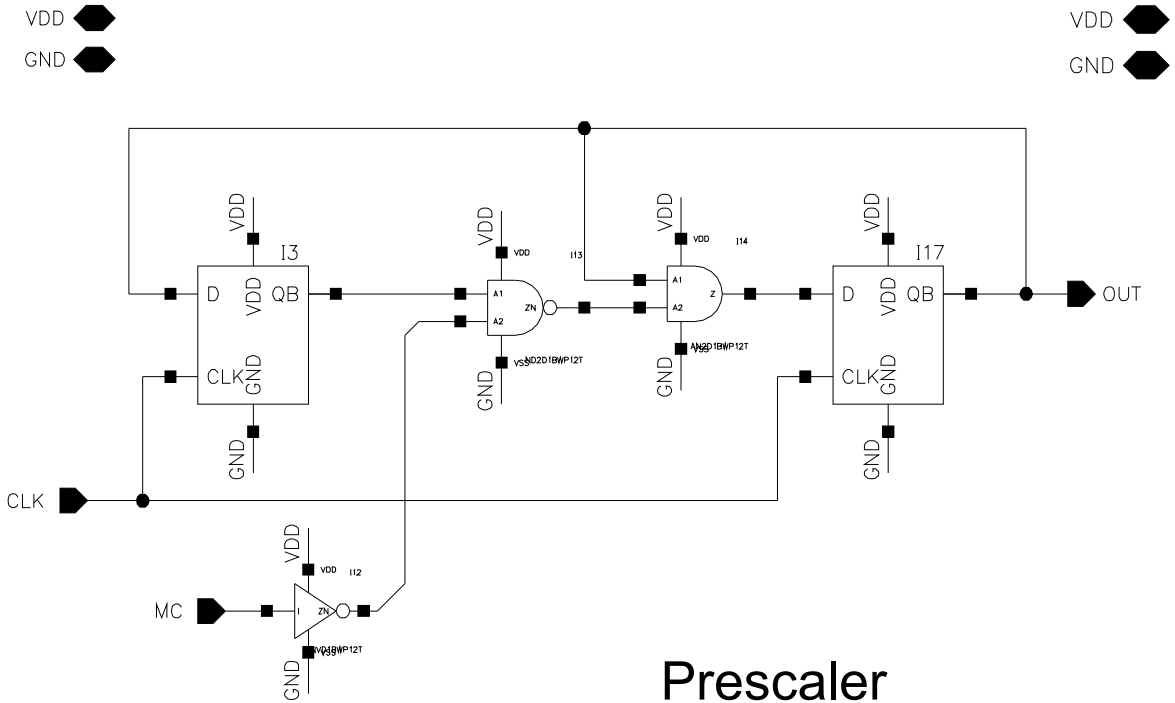
- Total tuning range = 5.5 GHz – 9 GHz.
- Phase noise = –90 to –105 dBc/Hz at 1 MHz offset (depending on the output frequency).
- Phase noise needs further optimization:
  - Modify the value of DC bias resistors in the varactor network to reduce their noise contribution.
  - Increase switch sizes in the switched capacitor network to reduce impact on tank *Q*.
  - Filter out 1/*f* noise from the tail current source to reduce degradation of close-in phase noise (caused by up-conversion of the 1/*f* noise).



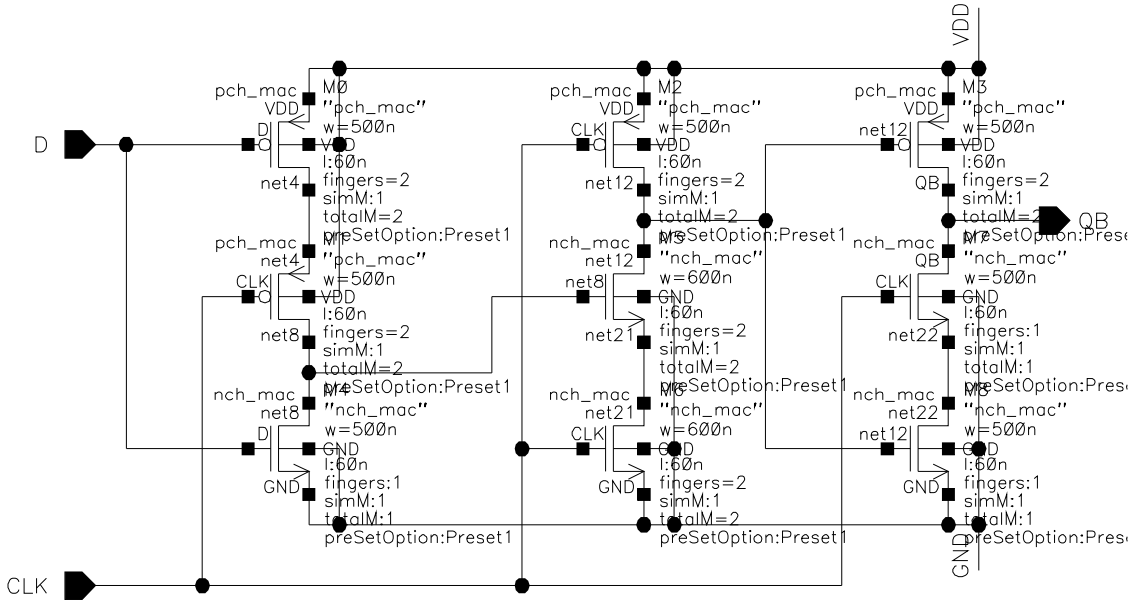


Dual-modulus prescaler

- Standard divide-by-2 or 3 circuit.
- Dynamic (TSPC) flip-flops used to minimize propagation delay.



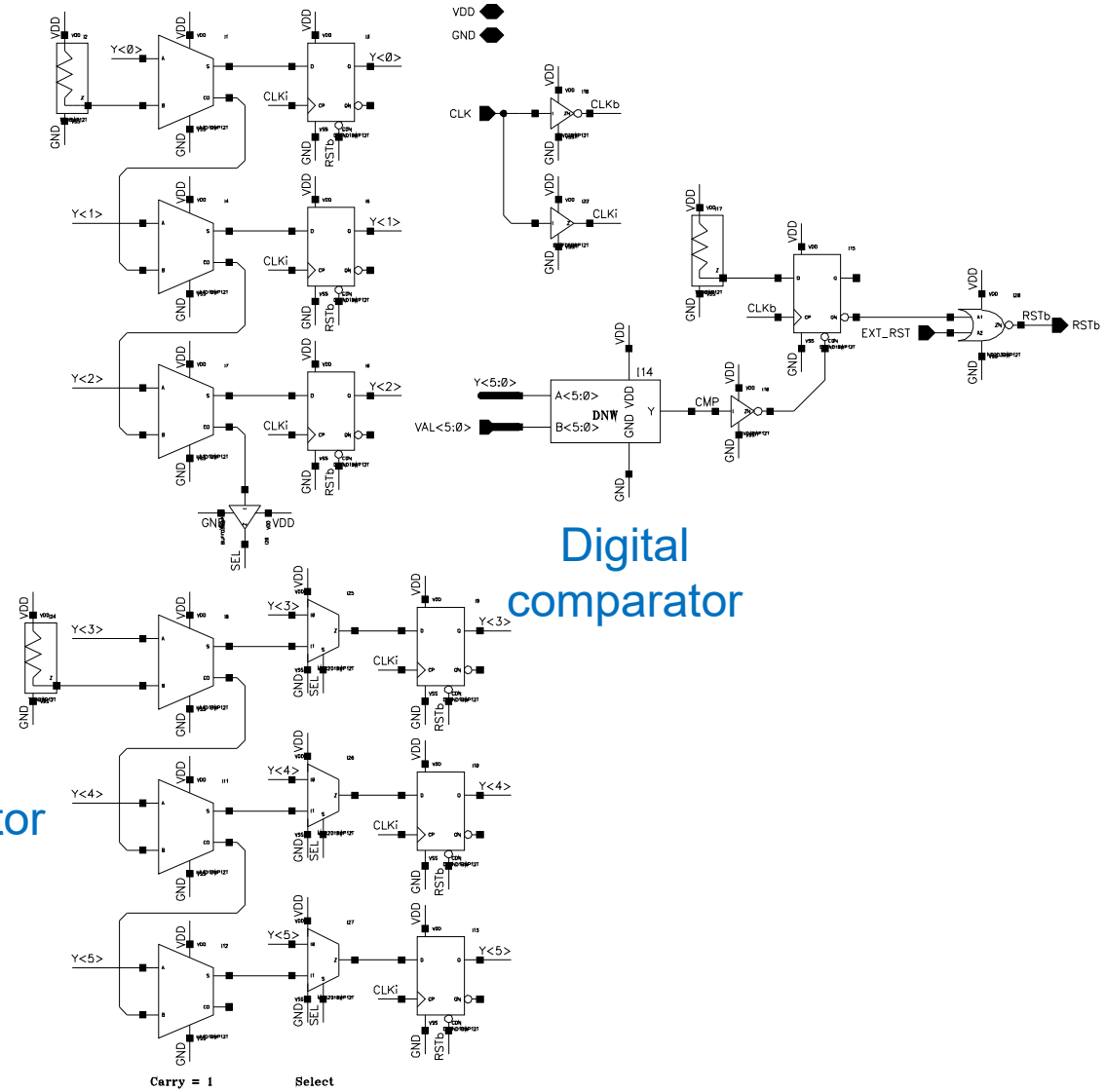
Prescaler



TSPC flip-flop

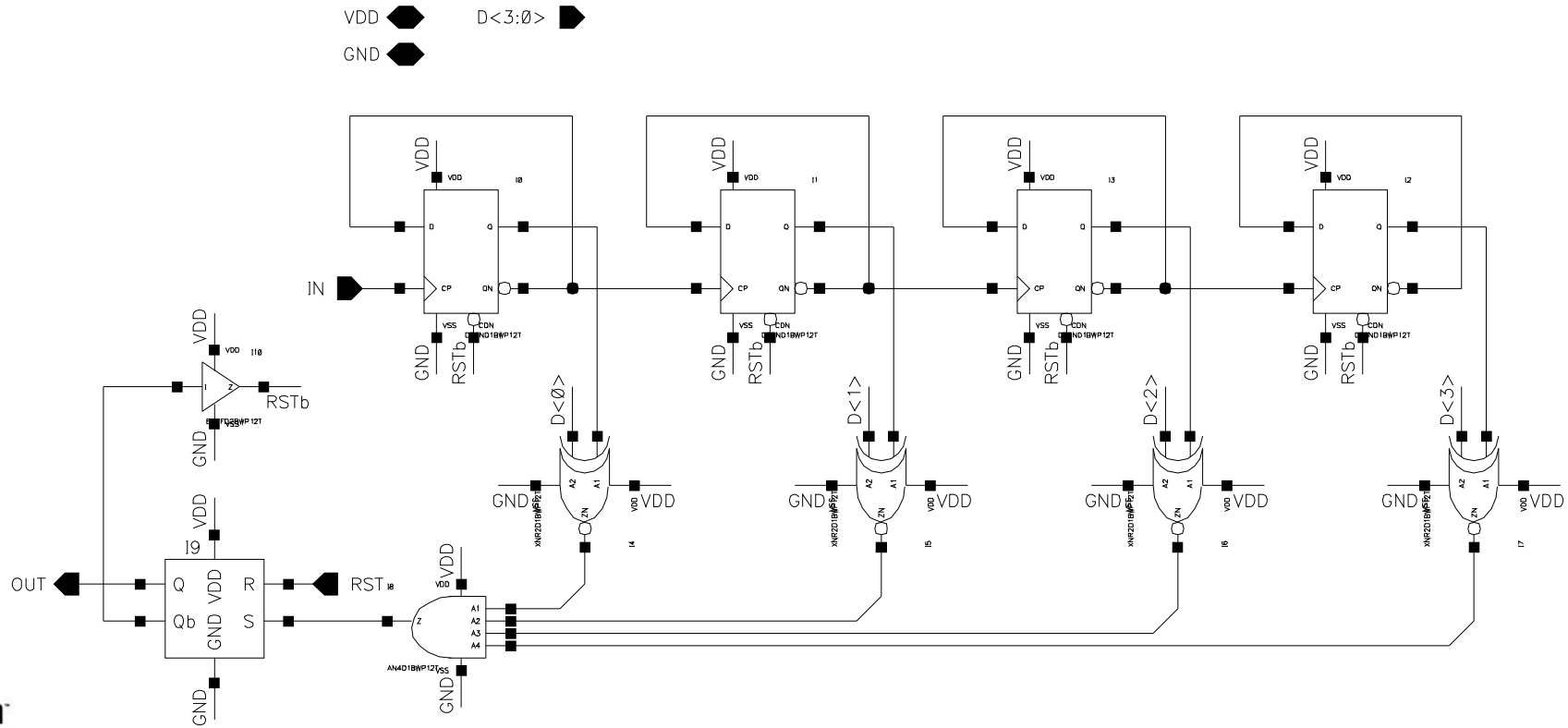
Programmable counter (6-bit)

- The accumulator value increments on every rising clock edge.
- A one-level carry select adder (CSA) is used since it has lower propagation delay than a standard ripple carry adder at the cost of a relatively small increase in complexity.
- The accumulator is reset when the value reaches the 6-bit number *P* (set by the user).



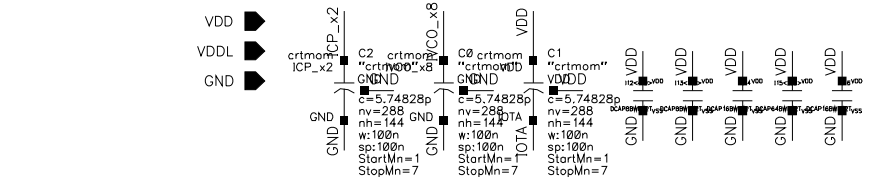
Swallow counter (4-bit)

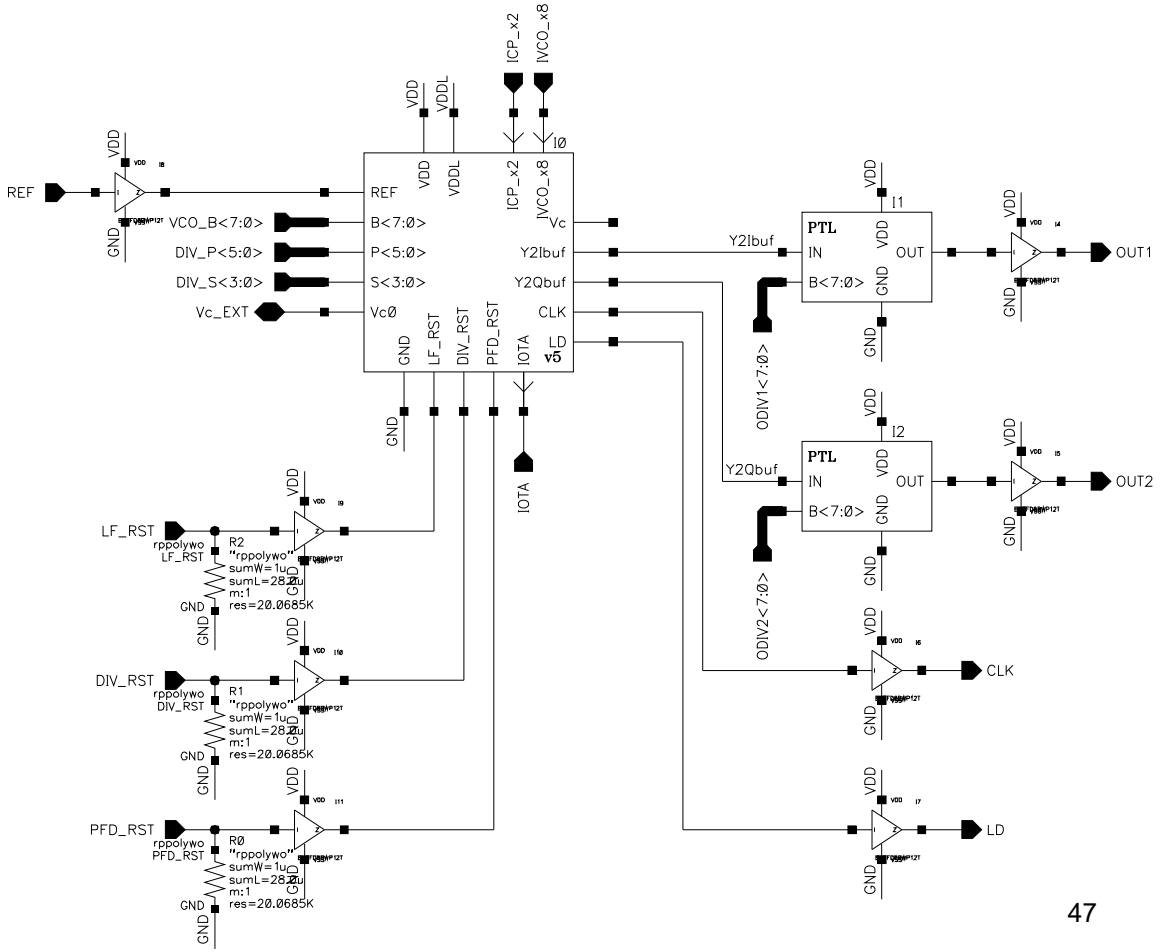
- Standard “textbook” design.
- The output of the SR latch goes high when the output of the 4-bit ripple counter matches the user-defined number *S*.



Complete frequency synthesizer block

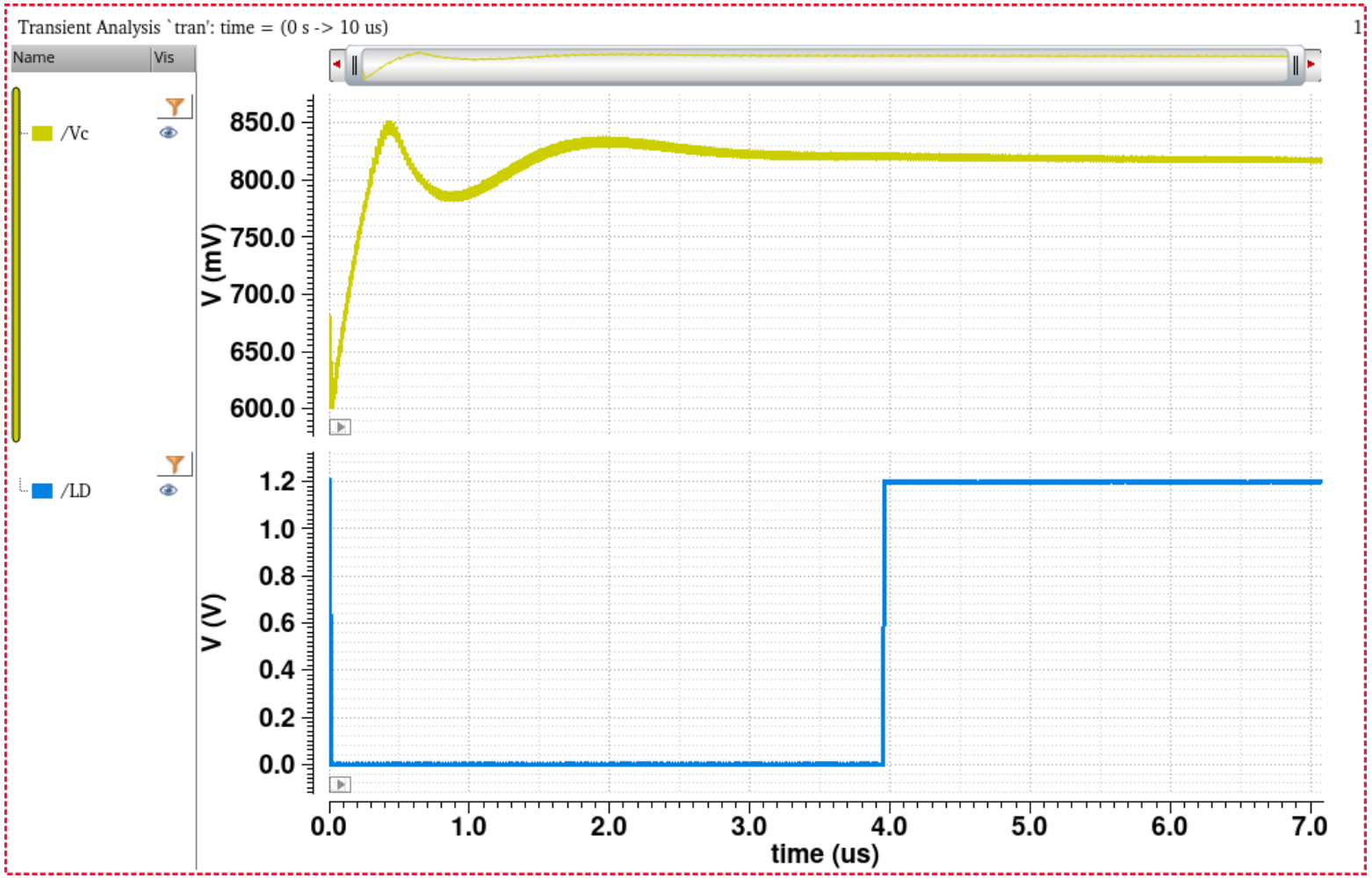
- Adds dual output dividers to the basic integer-*N* synthesizer to allow generation of two programmable output frequencies.
- Also includes input/output buffers.





Post-layout simulation of the PLL

- Transient simulation of the tt corner shows no major changes in the PLL settling response.



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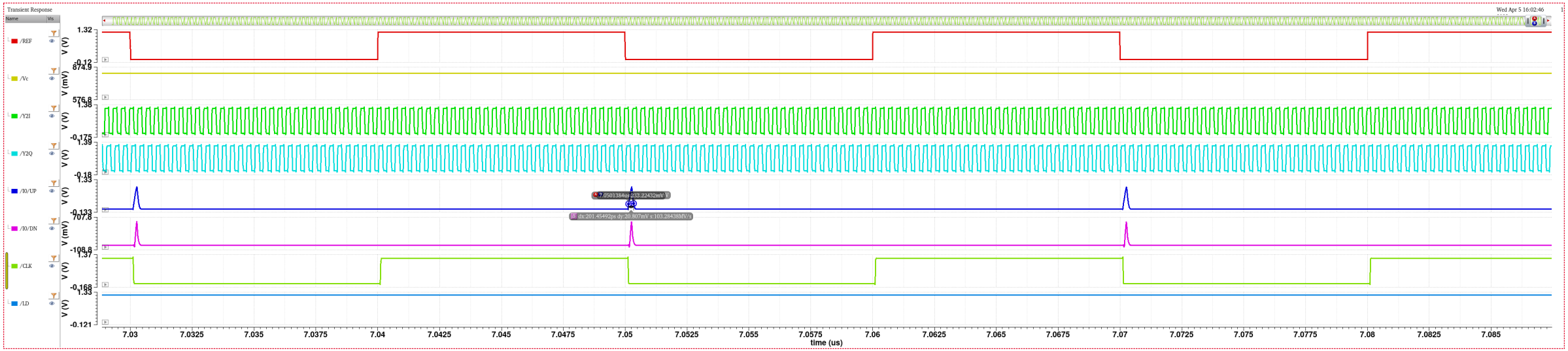
Post-layout simulation of the PLL (2)

- Transient simulation of the tt corner shows no major changes in the PLL settling response.



Zoomed-in view in steady-state conditions (after locking)

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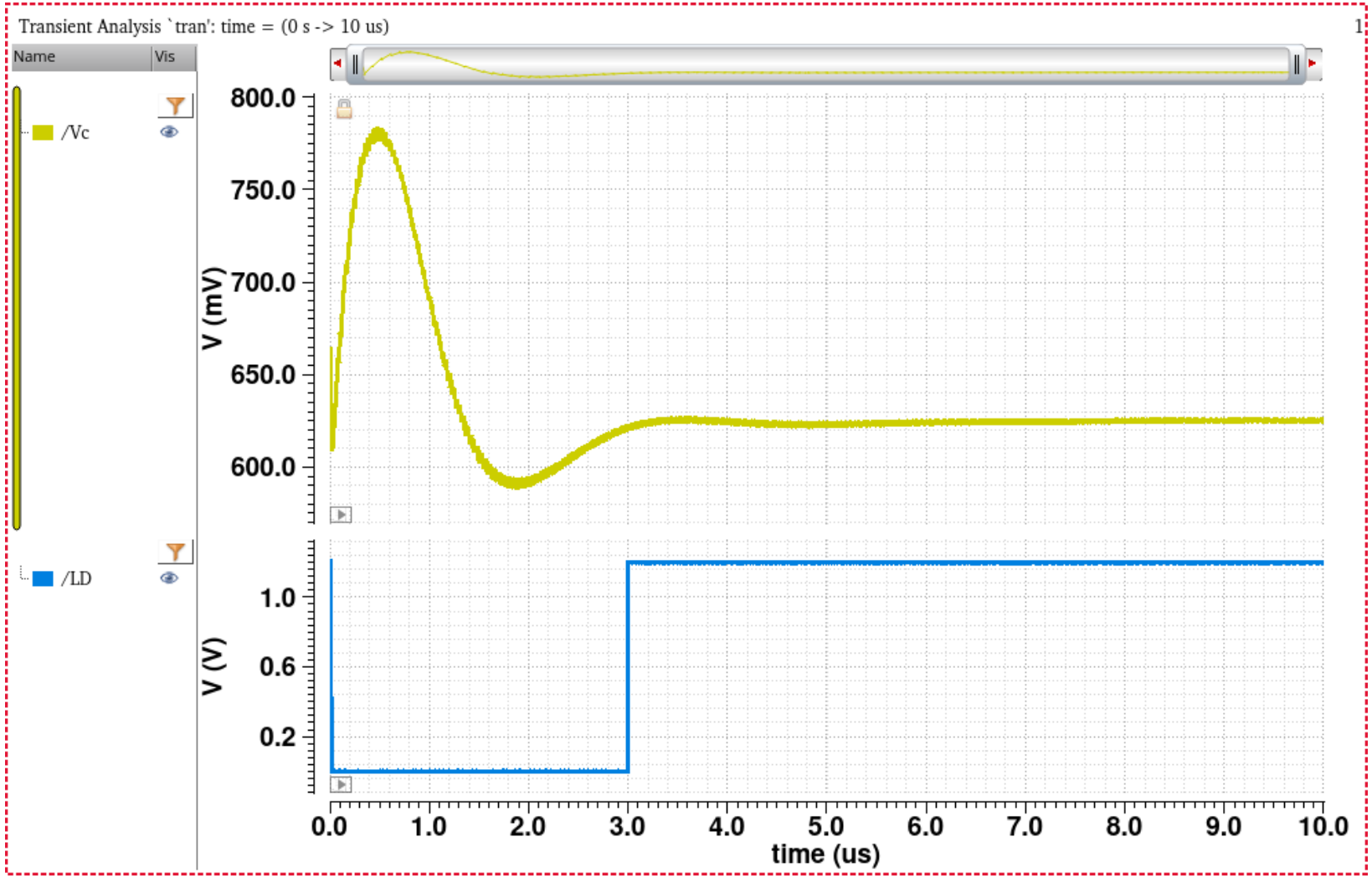
Post-layout simulation of the PLL

- Transient simulation of the ss corner shows no major changes in the PLL settling response.



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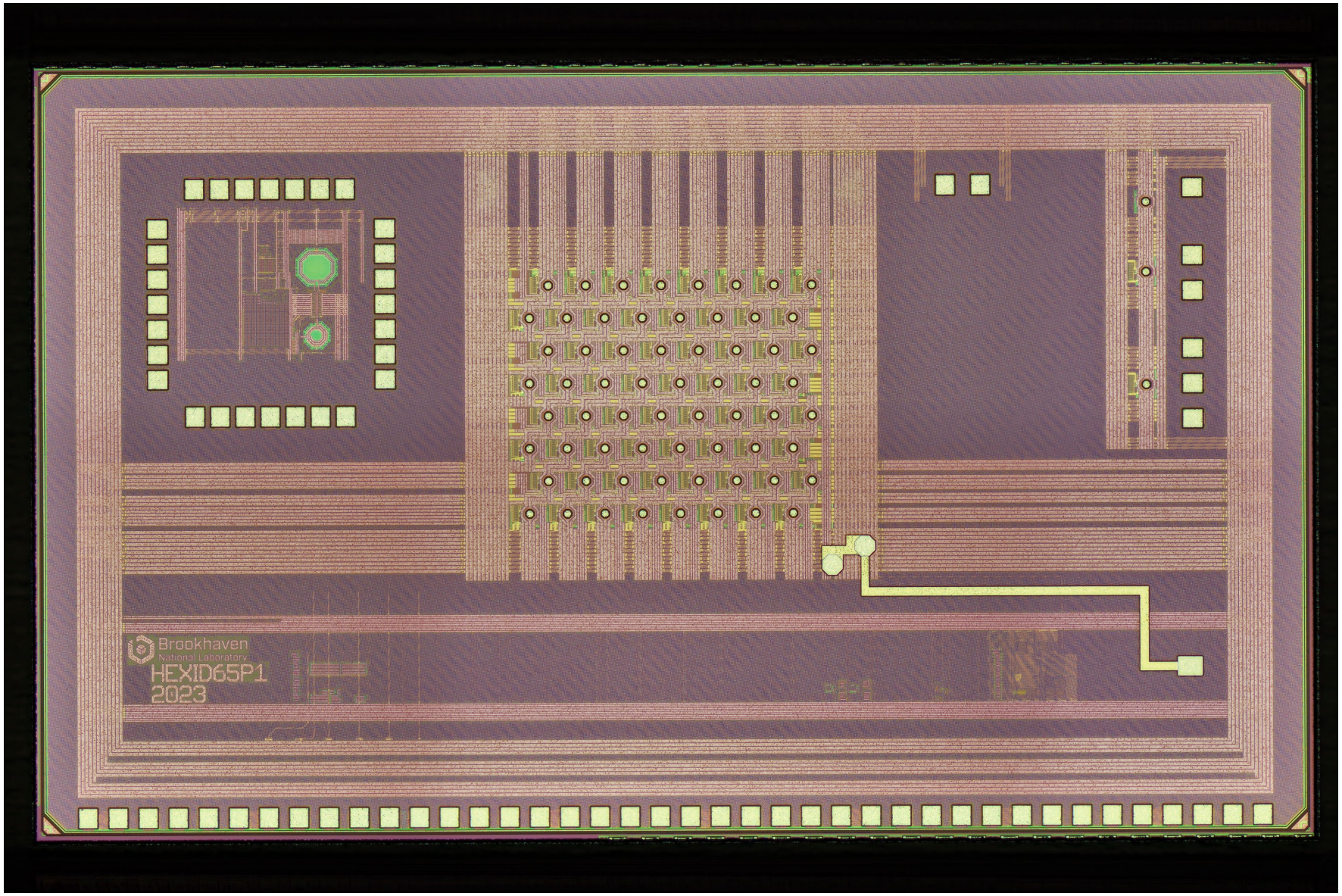
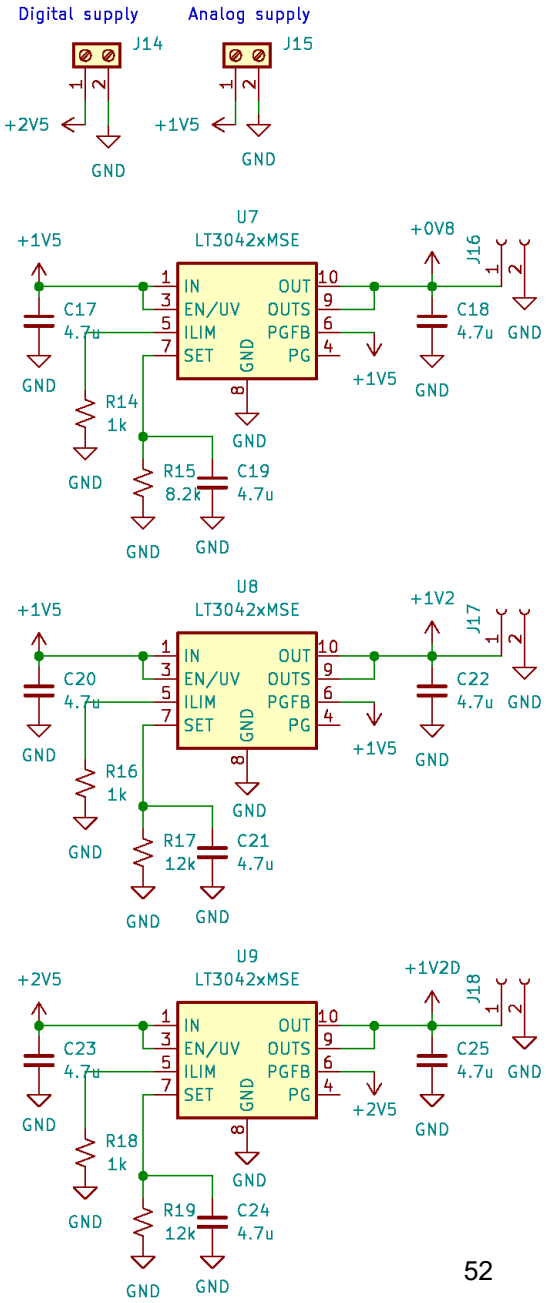
Die photograph



Design of the test board (4)

- The DC power supplies are split into analog (1.2V), digital (1.2V), and VCO (0.8V) paths
- All supplies use the same LDO (LT3042) to simplify the design



Typical waveforms (1)

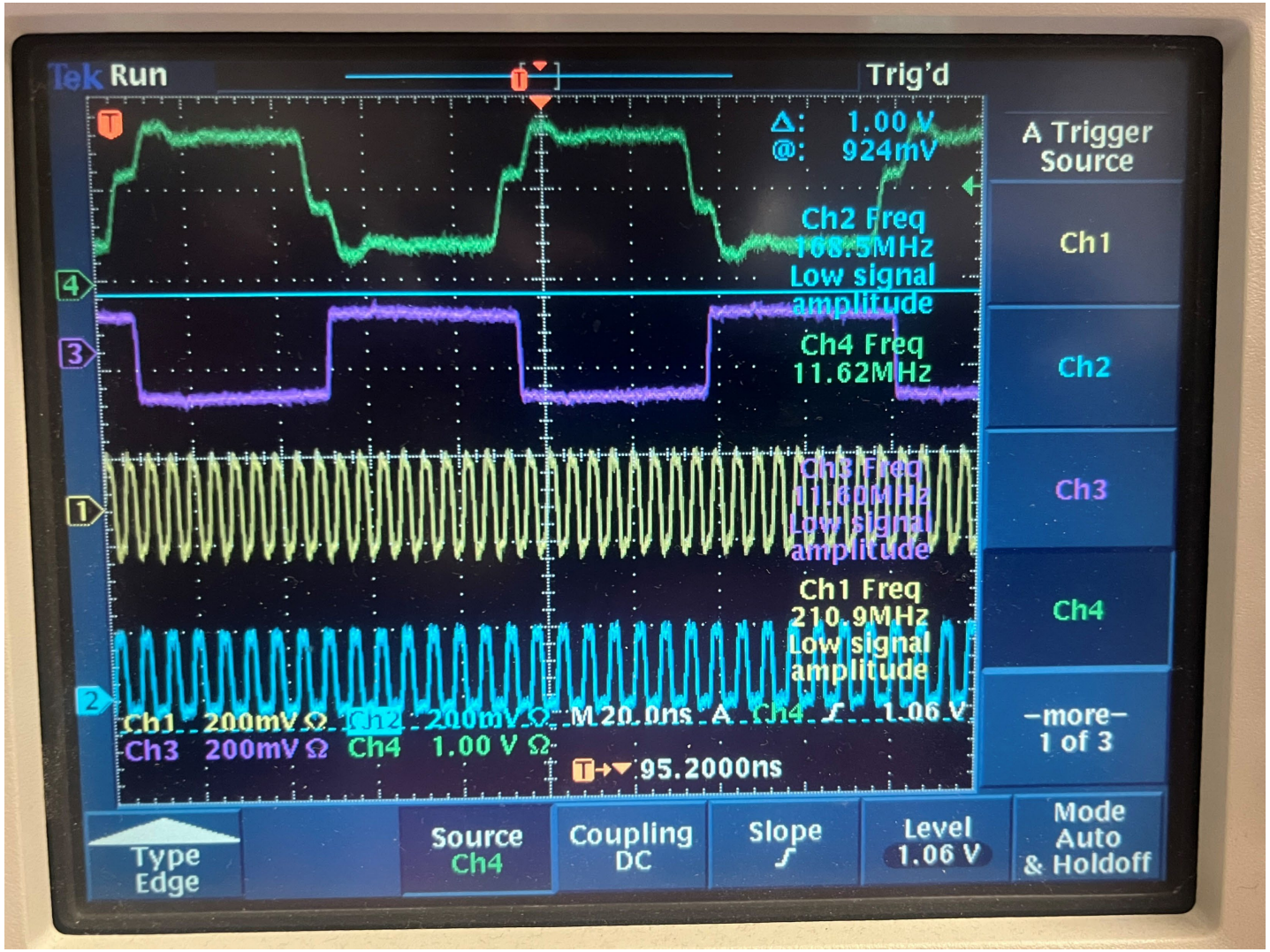
- Reference source: Tektronix AWG
- PLL locked
- Reference waveform is distorted due to lack of impedance matching on the test board

Reference

Recovered clock

Output 1

Output 2



Typical waveforms (2)

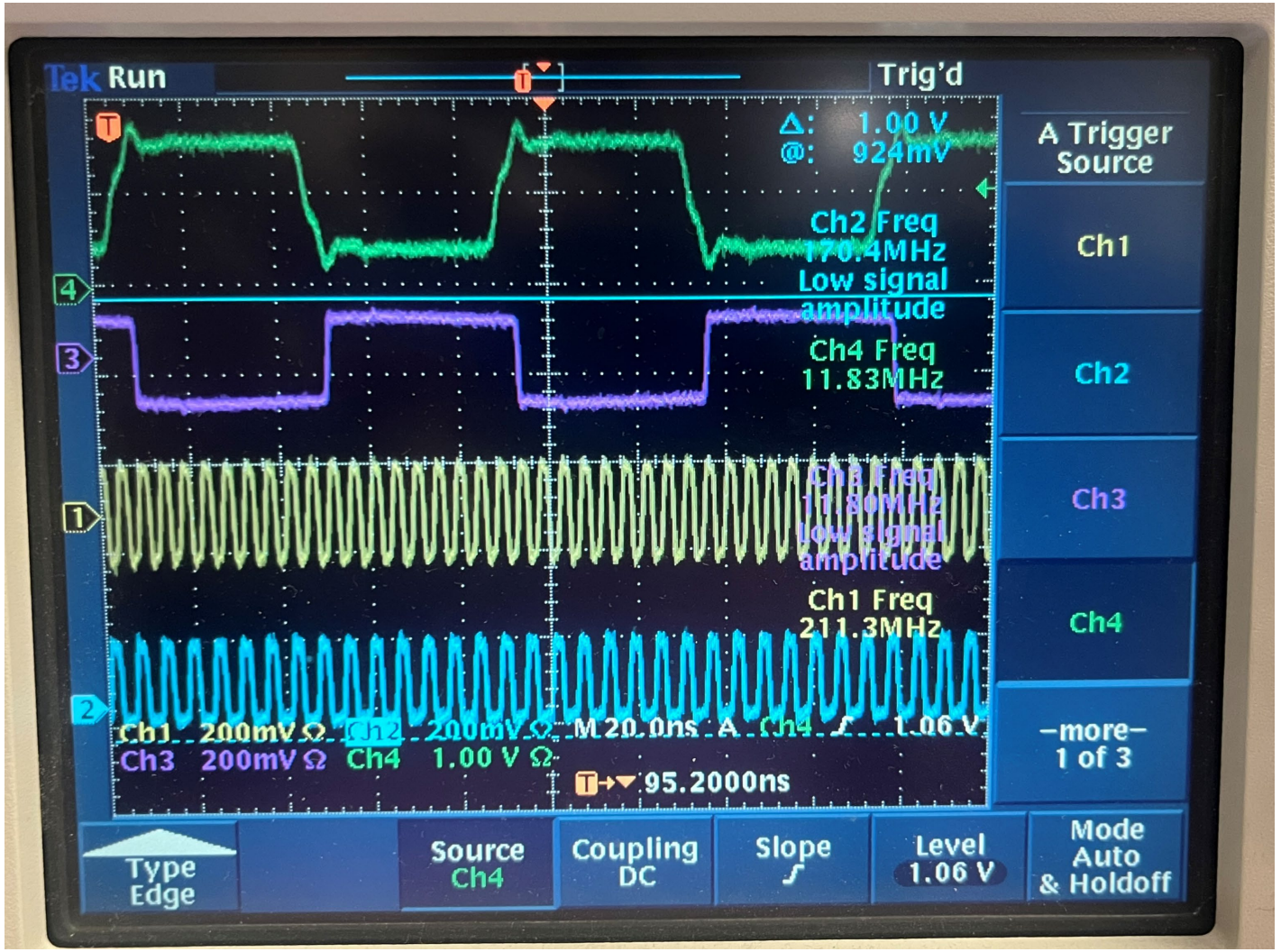
- Reference source: Tektronix AWG
- PLL locked
- Distortion of reference waveform decreased by using a shorter cable

Reference

Recovered clock

Output 1

Output 2



Typical waveforms (3)

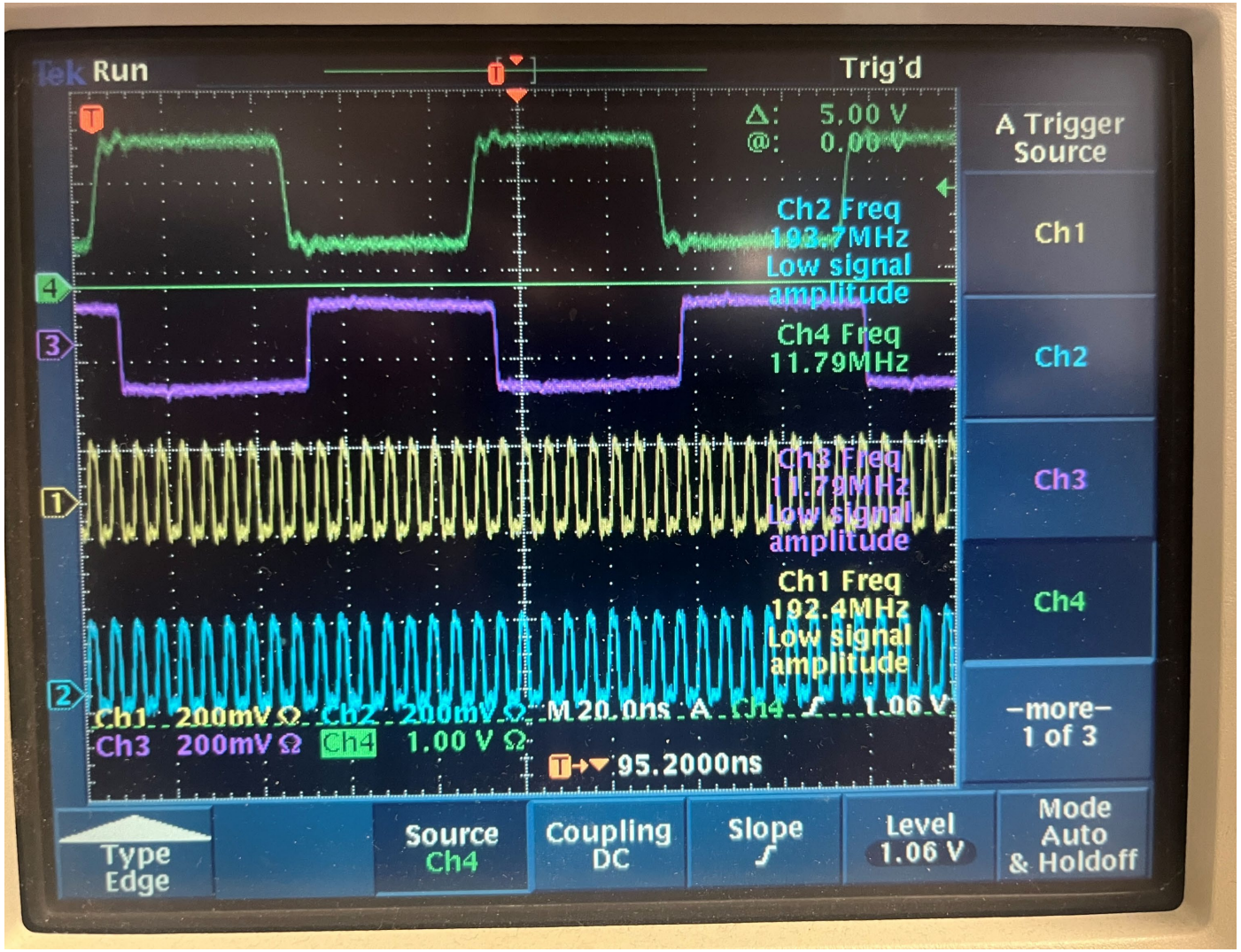
- Reference source: Tektronix AWG
- PLL locked
- Distortion of reference waveform greatly decreased by adding a 50Ω load (via a splitter) next to the test board

Reference

Recovered clock

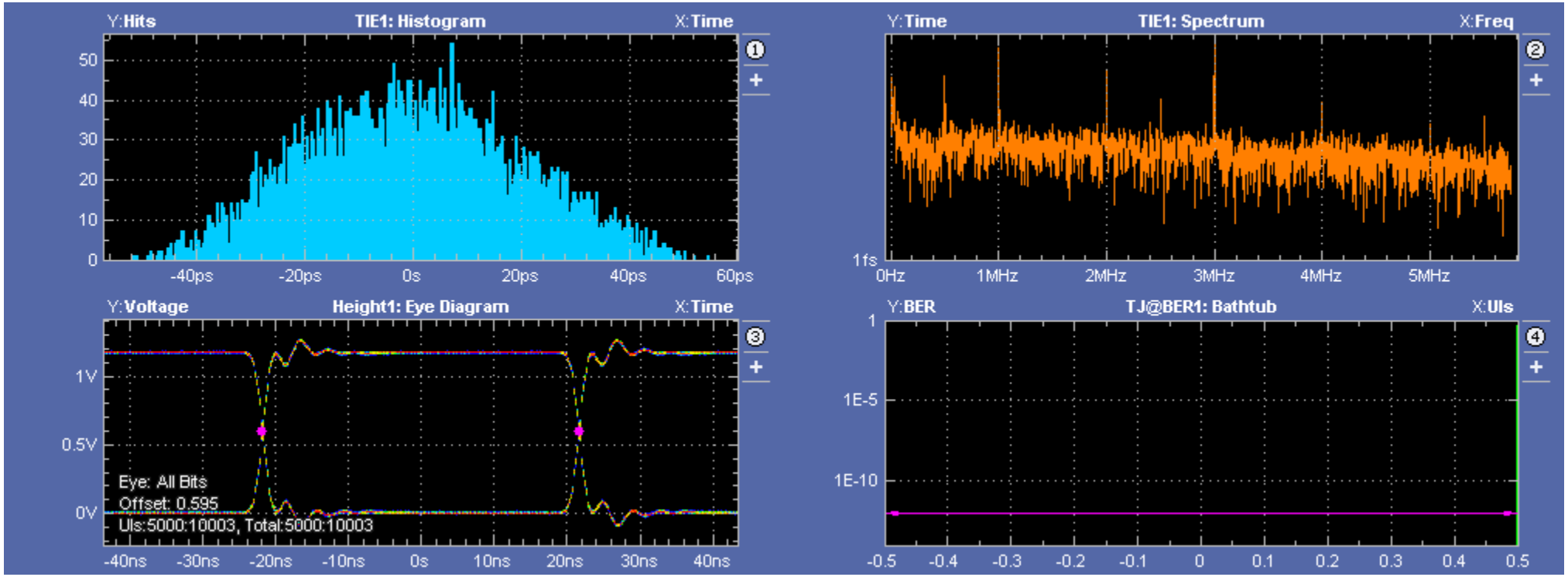
Output 1

Output 2



Jitter measurements: Reference input

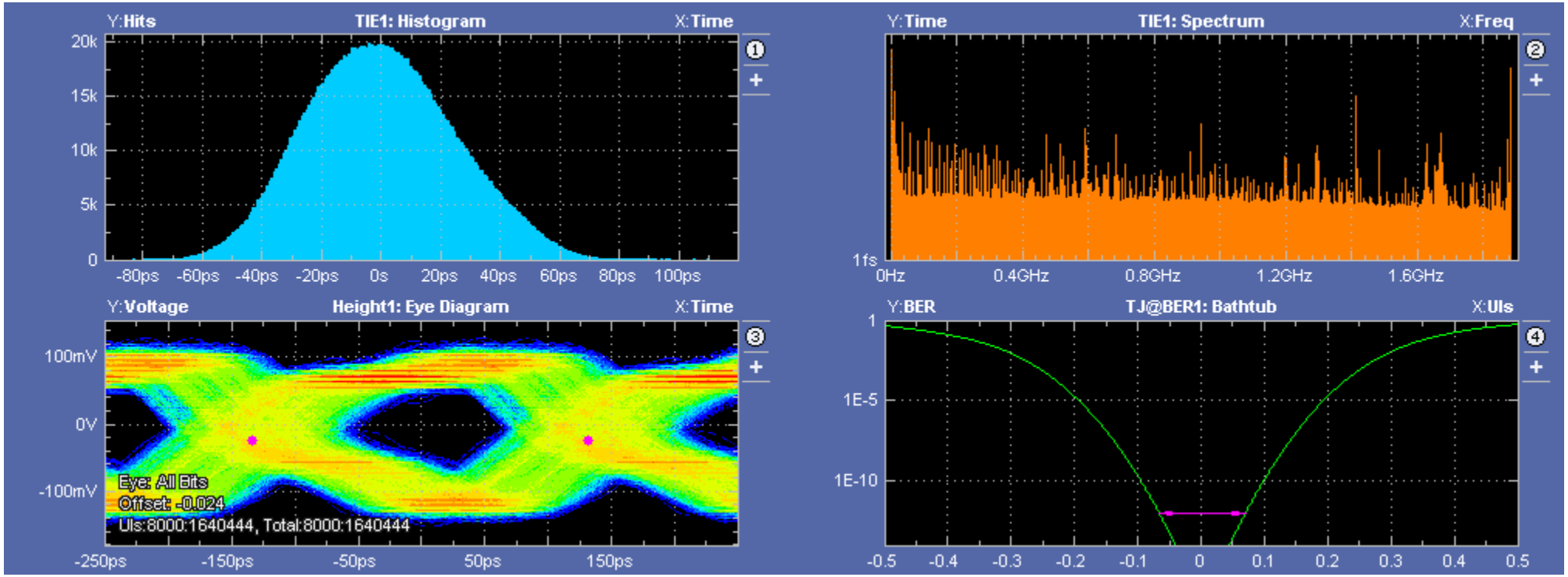
- Measured using the “one-shot jitter” mode on a Tektronix MSO 72004C high-speed oscilloscope (4 channels, 20 GHz, 100 GS/s)
- Highest observed output frequency ~1.9 GHz (corresponding to M = 2)
- Reference source: Tektronix AWG @11.5 MHz



RMS jitter = 19.8 ps, Peak-peak jitter = 106.5 ps

Jitter measurements: Output 1 (M = 2)

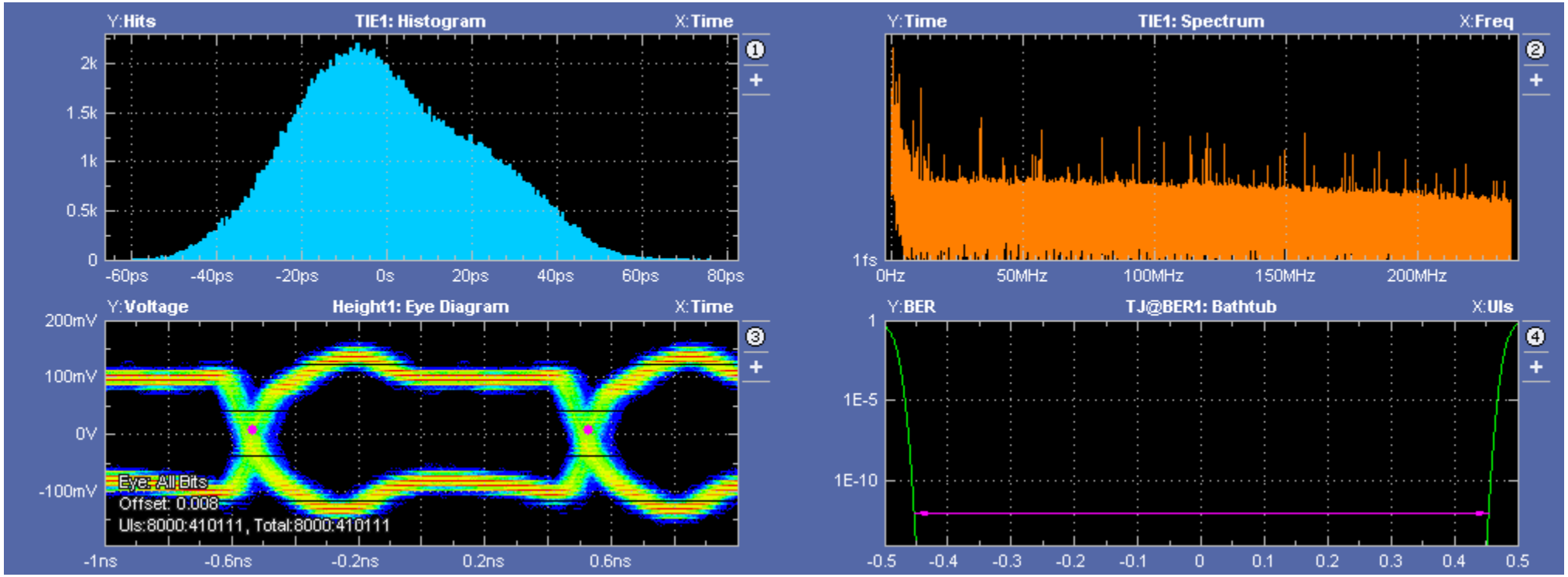
- Reference source: Tektronix AWG @11.5 MHz
- Little difference in jitter observed when the input voltage sources (3V batteries) were replaced by a benchtop power supply → confirms good PSRR of the on-board LDOs



RMS jitter = 24.4 ps, Peak-peak jitter = 193.4 ps

Jitter measurements: Output 2 (M = 8)

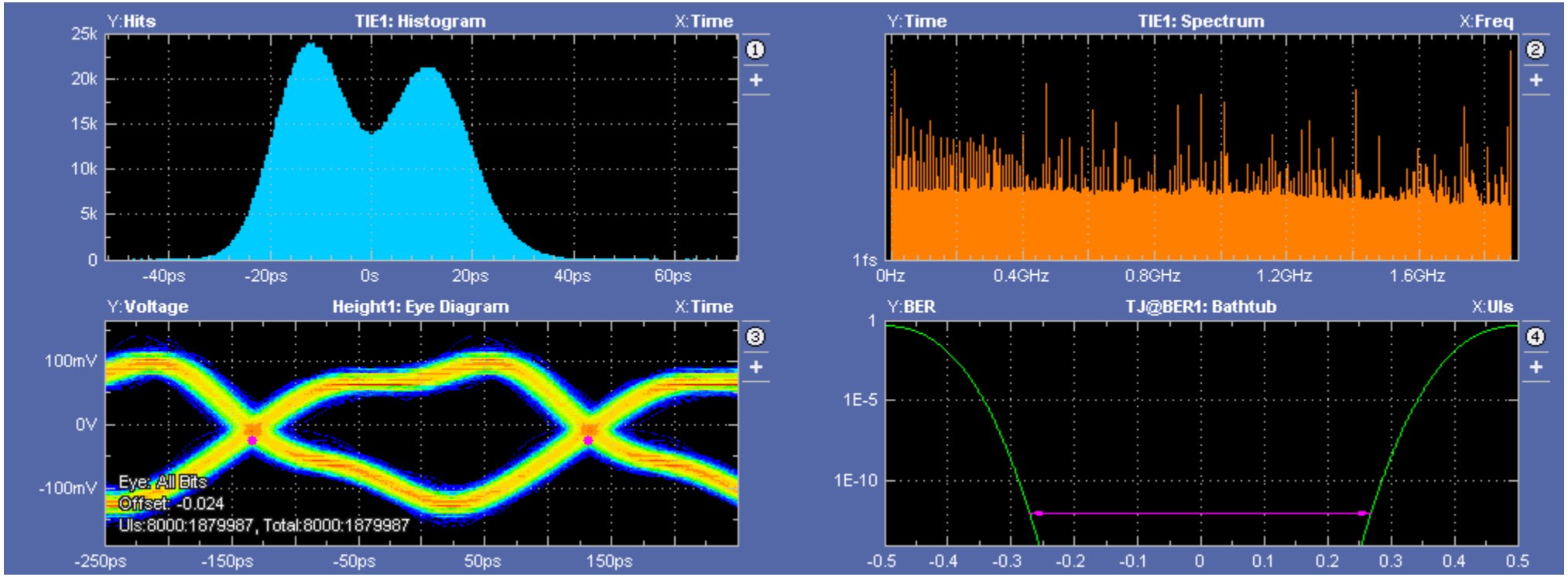
- Reference source: Tektronix AWG @11.5 MHz
- Little difference in jitter observed when the input voltage sources (3V batteries) were replaced by a benchtop power supply → confirms good PSRR of the on-board LDOs



RMS jitter = 20.9 ps, Peak-peak jitter = 130.1 ps

Jitter measurements: Output 1 (M = 2, 1.92 GHz)

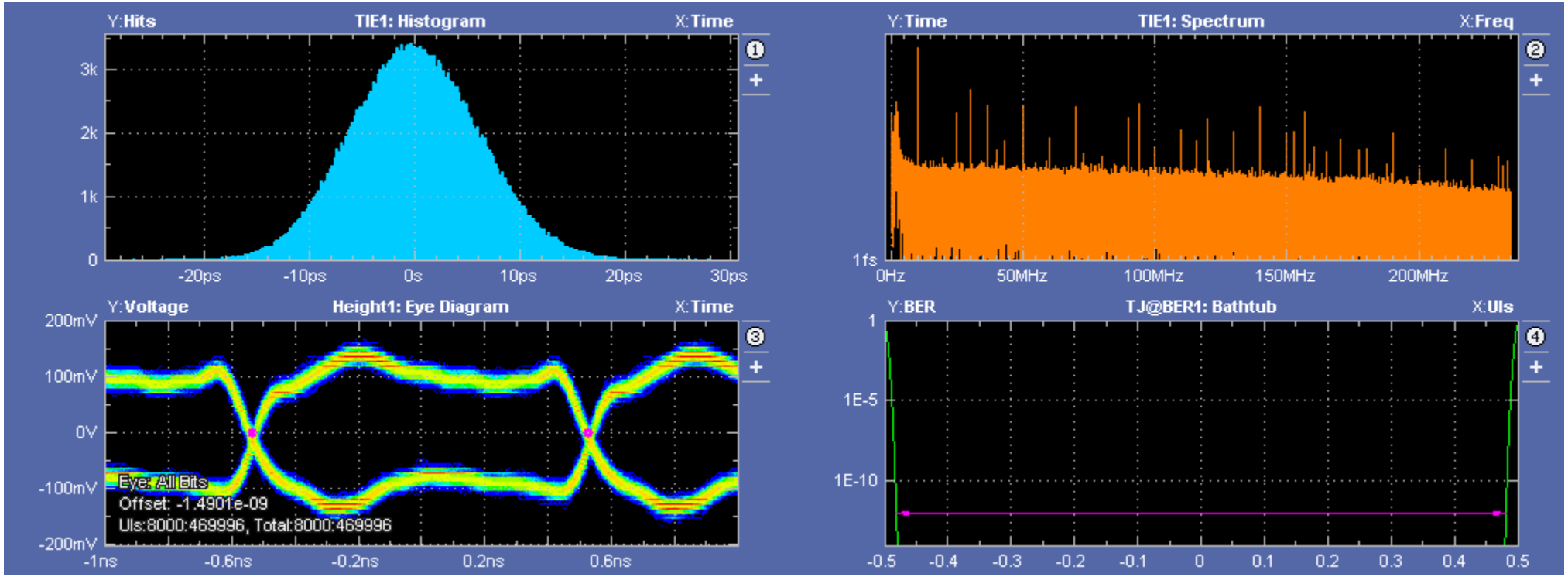
- Reference source: CTI OCXO @10 MHz
- Peak-to-peak jitter increases due to asymmetry between the rising and falling edges, which is determined by the on-board LVDS driver and not the PLL



RMS jitter = 14.0 ps, Peak-peak jitter = 113.6 ps

Jitter measurements: Output 2 (M = 8, 480 MHz)

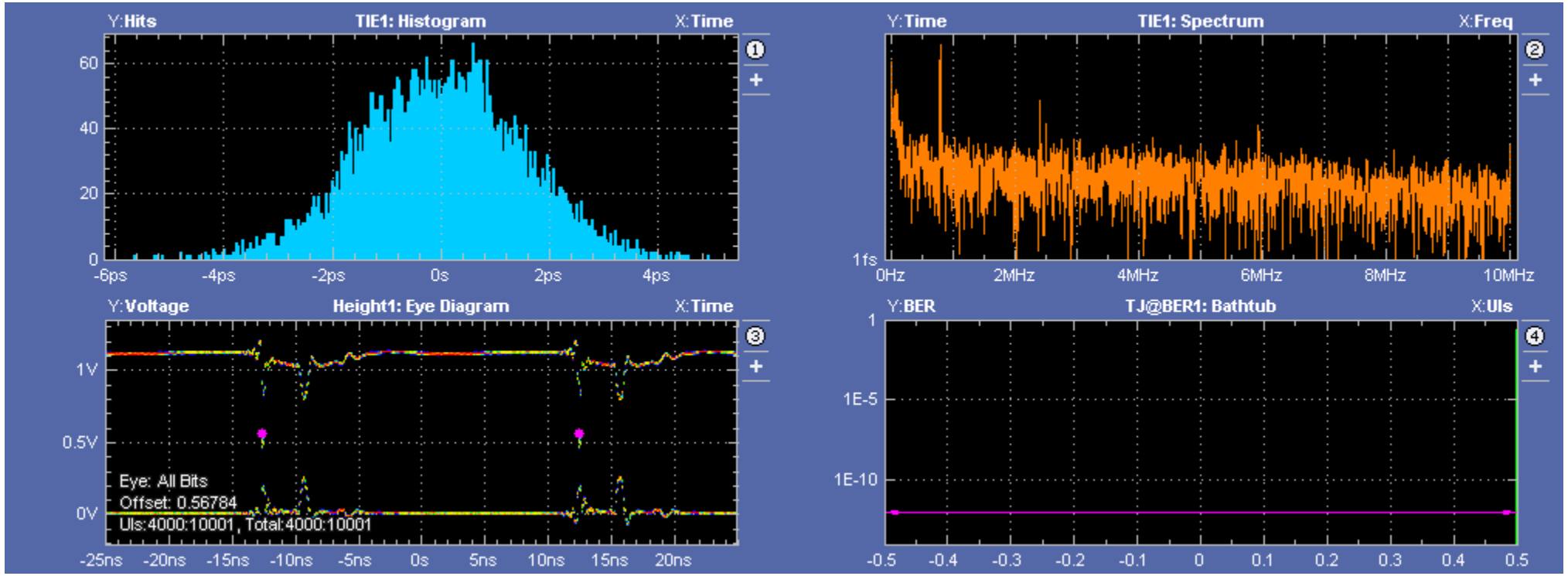
- Reference source: CTI OCXO @10 MHz



RMS jitter = 6.1 ps, Peak-peak jitter = 54.7 ps

Jitter measurements: Reference input

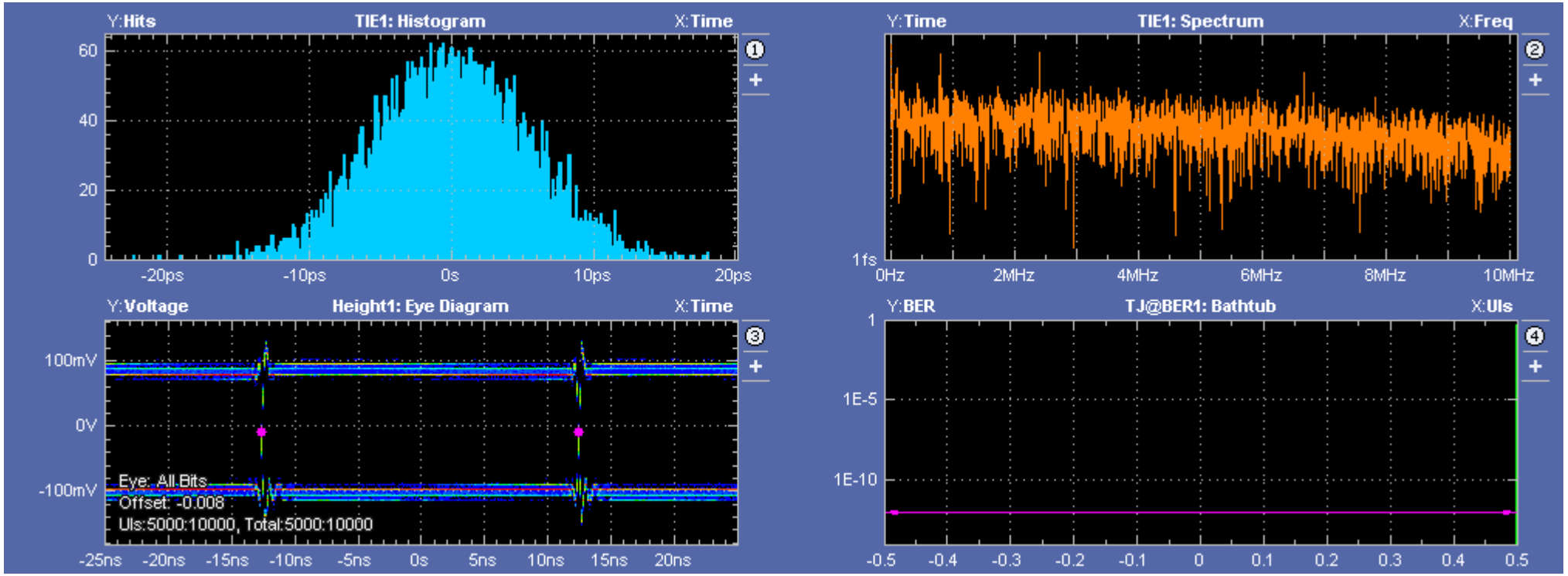
- Reference source: Leo Bodnar GPSDO @20 MHz
- Output jitter is ~1.4x larger than at 10 MHz



RMS jitter = 1.5 ps, Peak-peak jitter = 10.6 ps

Jitter measurements: Recovered clock

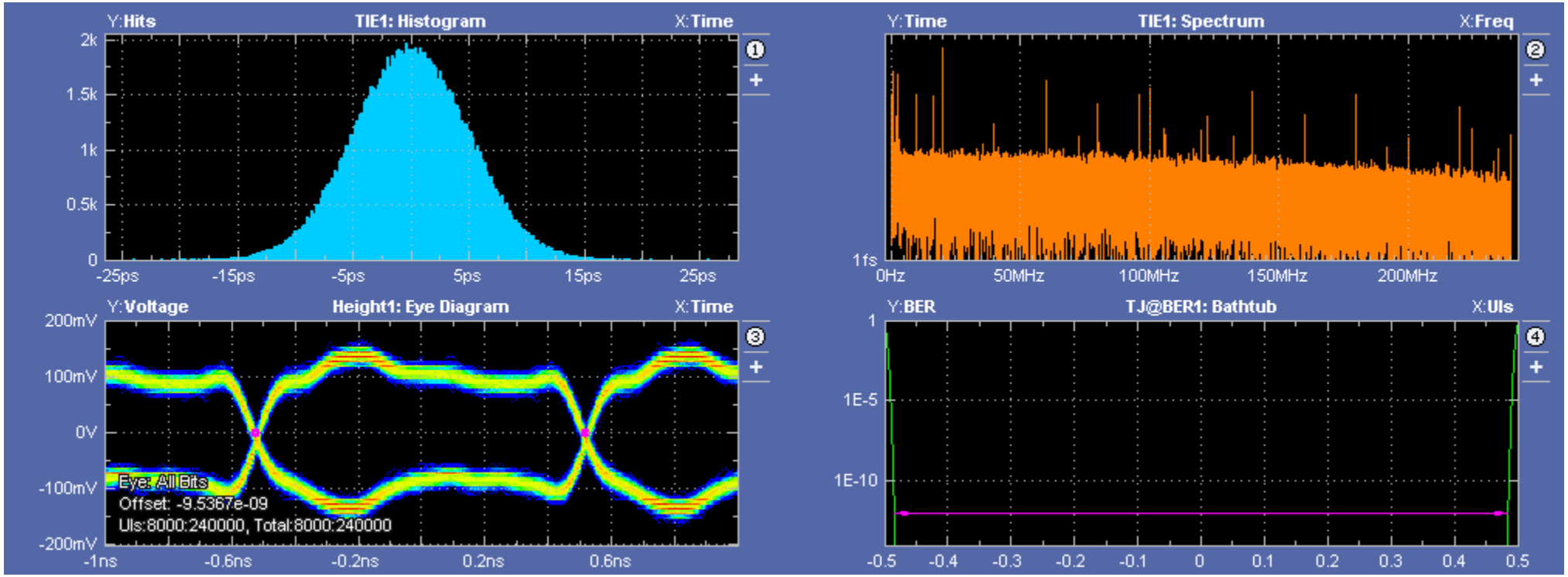
- Reference source: Leo Bodnar GPSDO @20 MHz
- Output jitter is ~3.5x larger than that of the reference



RMS jitter = 5.4 ps, Peak-peak jitter = 40.5 ps

Jitter measurements: Output 1 (M = 8)

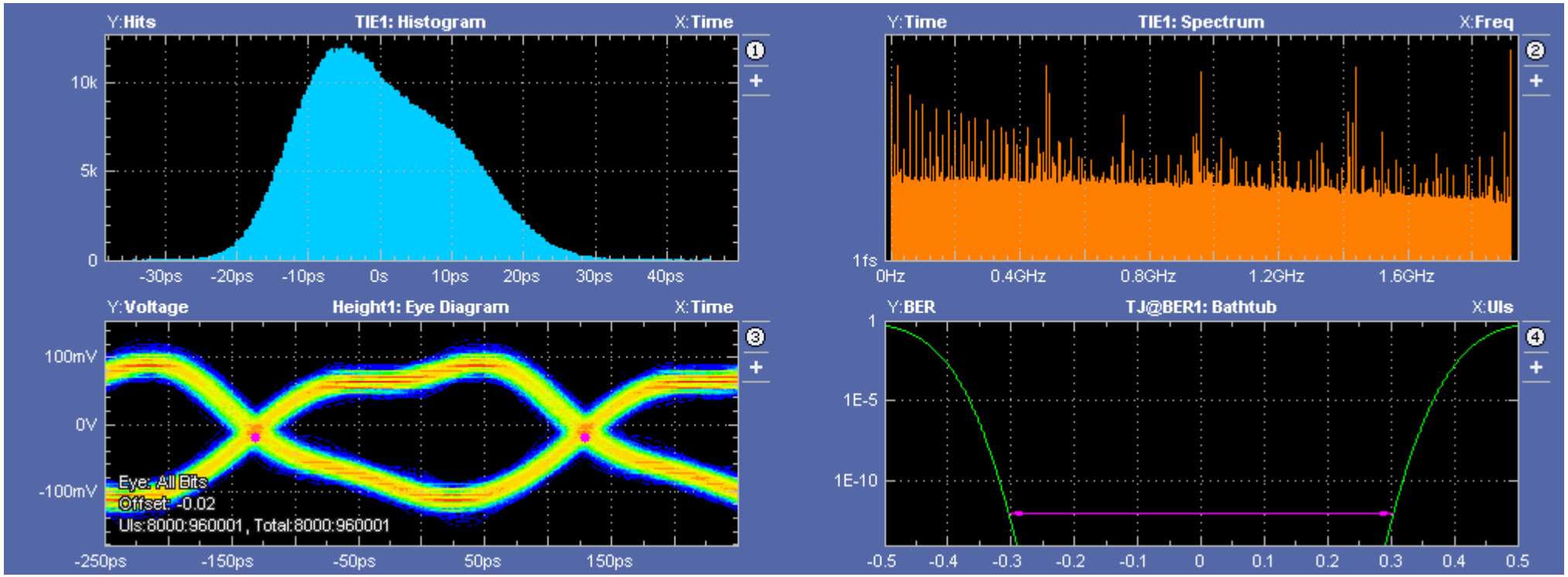
- Reference source: Leo Bodnar GPSDO @20 MHz



RMS jitter = 4.9 ps, Peak-peak jitter = 49.8 ps

Jitter measurements: Output 2 (M = 2)

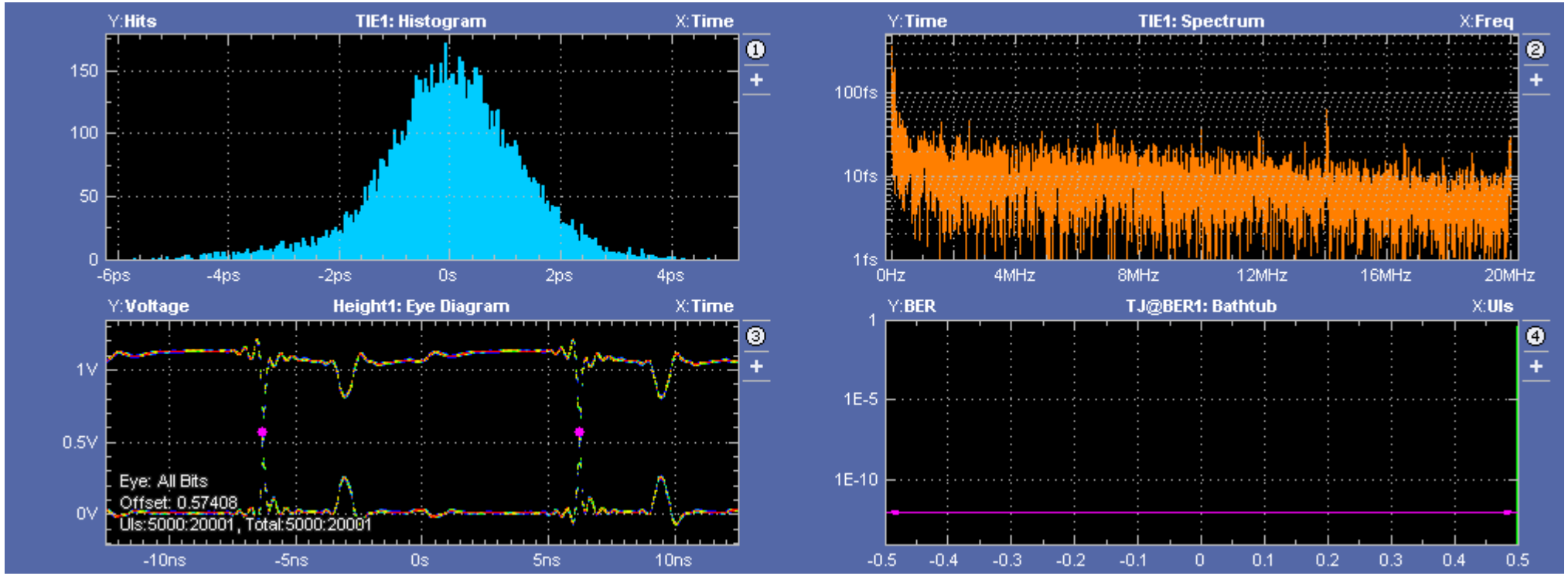
- Reference source: Leo Bodnar GPSDO @20 MHz
- Peak-to-peak jitter increases due to asymmetry between the rising and falling edges, which is determined by the on-board LVDS driver and not the PLL
- Overall jitter is significantly lower than that with the GPSDO at 10 MHz due to the smaller multiplication factor for input-reference noise sources (reference, divider, etc.).



RMS jitter = 10.0 ps, Peak-peak jitter = 80.3 ps

Jitter measurements: Reference input

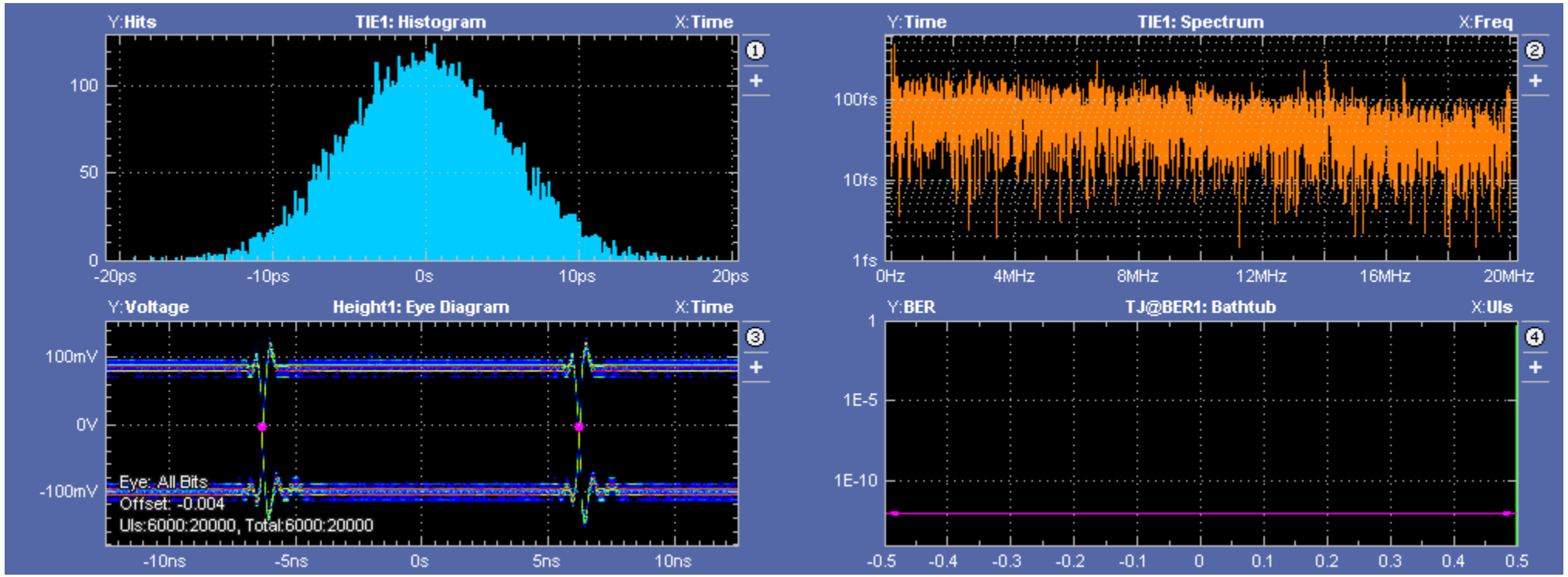
- Reference source: Leo Bodnar GPSDO @40 MHz
- Output jitter is slightly larger than at 10 MHz



RMS jitter = 1.25 ps, Peak-peak jitter = 10.4 ps

Jitter measurements: Recovered clock

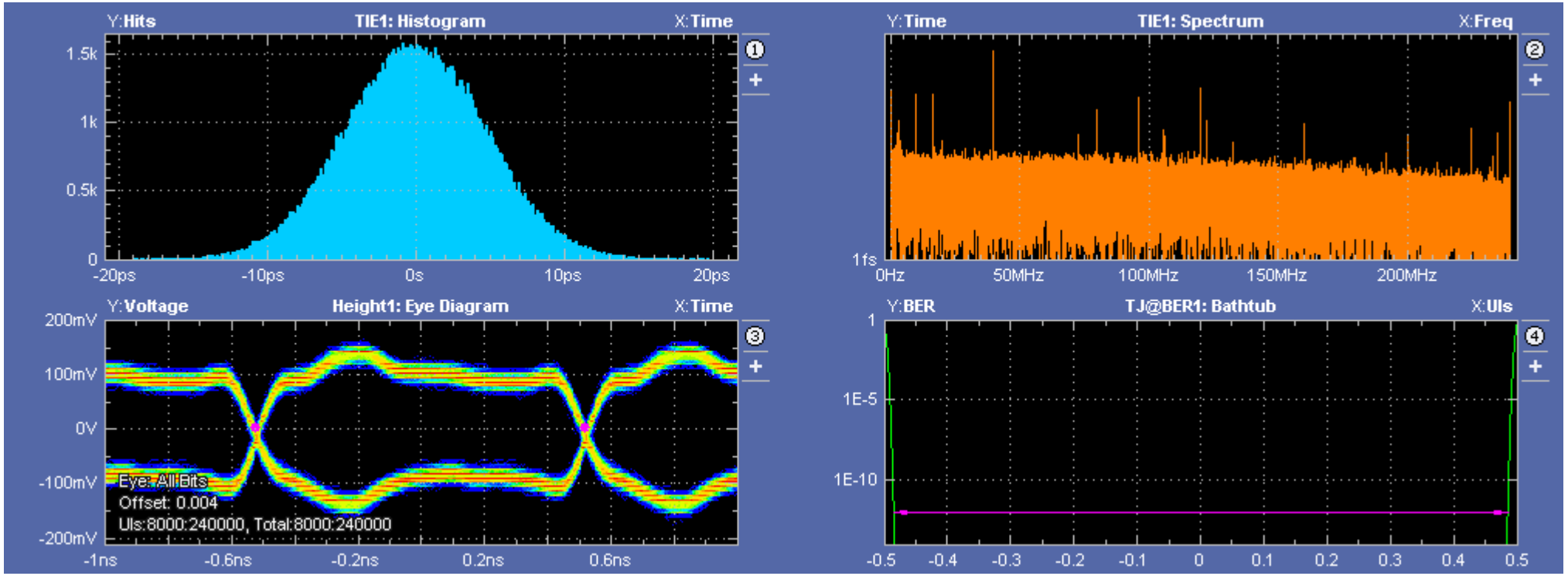
- Reference source: Leo Bodnar GPSDO @40 MHz
- Output jitter is ~4x larger than that of the reference



RMS jitter = 5.1 ps, Peak-peak jitter = 37.6 ps

Jitter measurements: Output 1 (M = 8, 480 MHz)

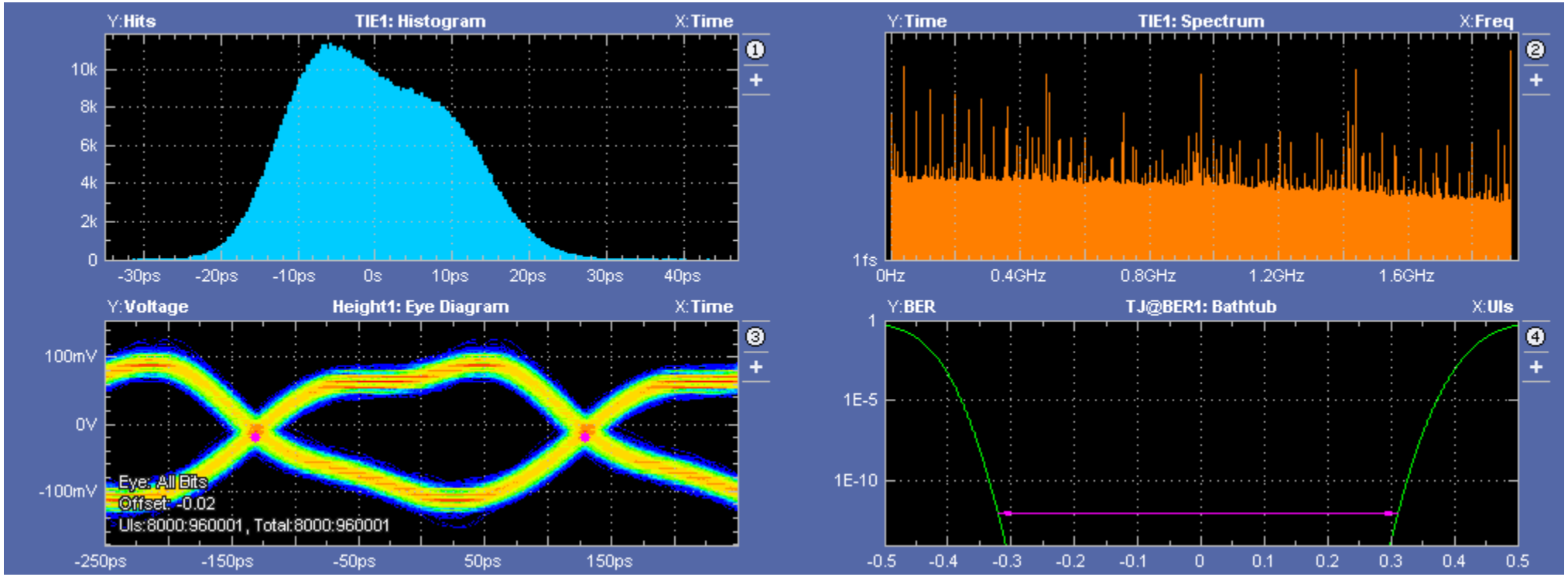
- Reference source: Leo Bodnar GPSDO @40 MHz



RMS jitter = 4.7 ps, Peak-peak jitter = 38.7 ps

Jitter measurements: Output 2 (M = 2, 1.92 GHz)

- Reference source: Leo Bodnar GPSDO @40 MHz
- Peak-to-peak jitter increases due to asymmetry between the rising and falling edges, which is determined by the on-board LVDS driver and not the PLL
- Overall jitter decreases compared to that for f_{REF} = 10 MHz due to the smaller multiplication factor for input-reference noise sources (reference, divider, etc.).



RMS jitter = 9.5 ps, Peak-peak jitter = 74.5 ps

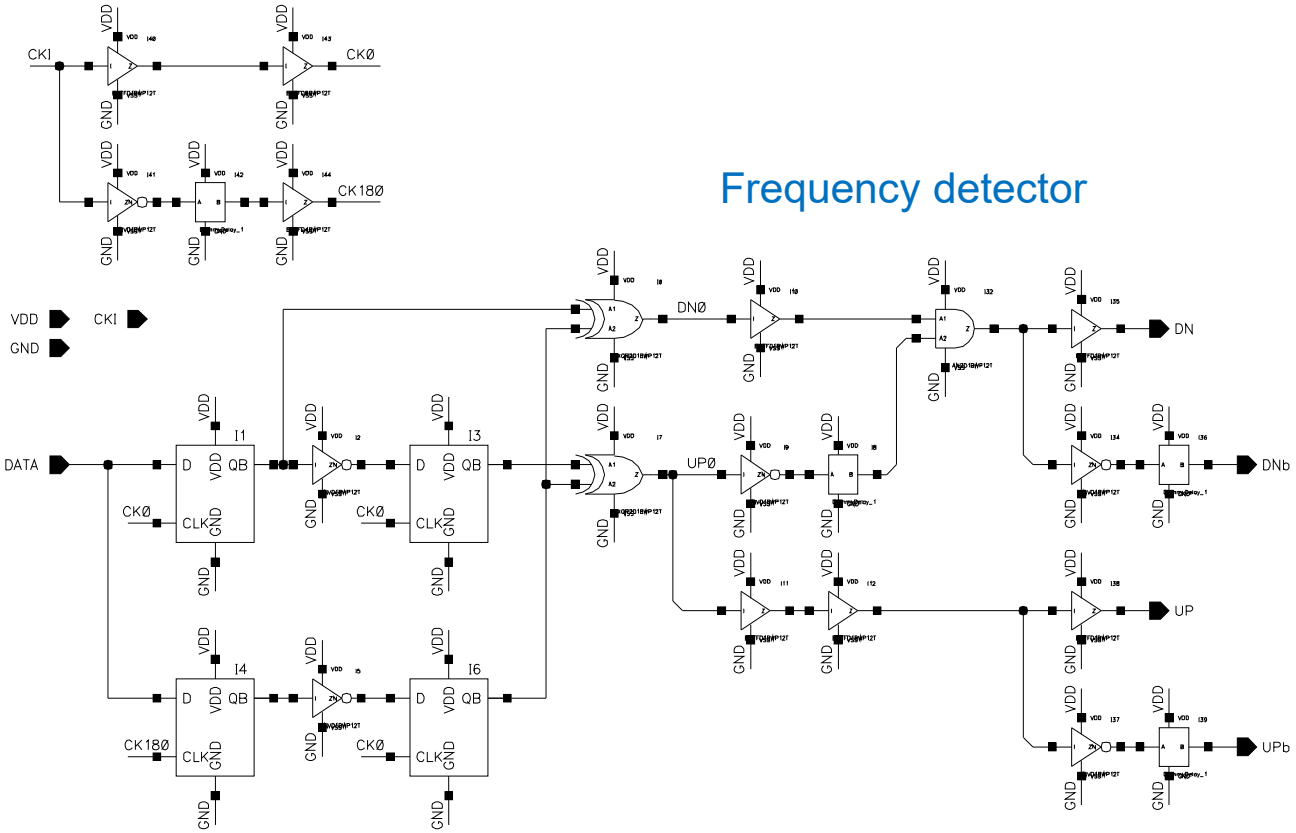
Typical waveforms

- Reference source: Leo Bodnar GPSDO @40 MHz
- Output divider 1: 2
- Output divider 2: 8
- Divider parameters:
  - N = 2, P = 11, S = 2
  - VCO frequency = 7.68 GHz
  - Output 1 frequency = 1.92 GHz
  - Output 2 frequency = 480 MHz

CDR design

Phase detector (PD)

- Used in the CDR loop.
- An Alexander or “bang-bang” PD is used to enable operation at high data rates.
  - Unlike a linear PD (such as the Hogge design), the output UP/DN pulse widths produced by a bang-bang PD are at least one clock cycle long.
- A simple modification (one additional AND gate) of the basic Alexander PD is used to provide frequency error information.
  - The resultant locking range is unbounded for negative frequency errors (f_{CLK} < 1/UI).
  - This eliminates the need for a separate frequency acquisition loop.

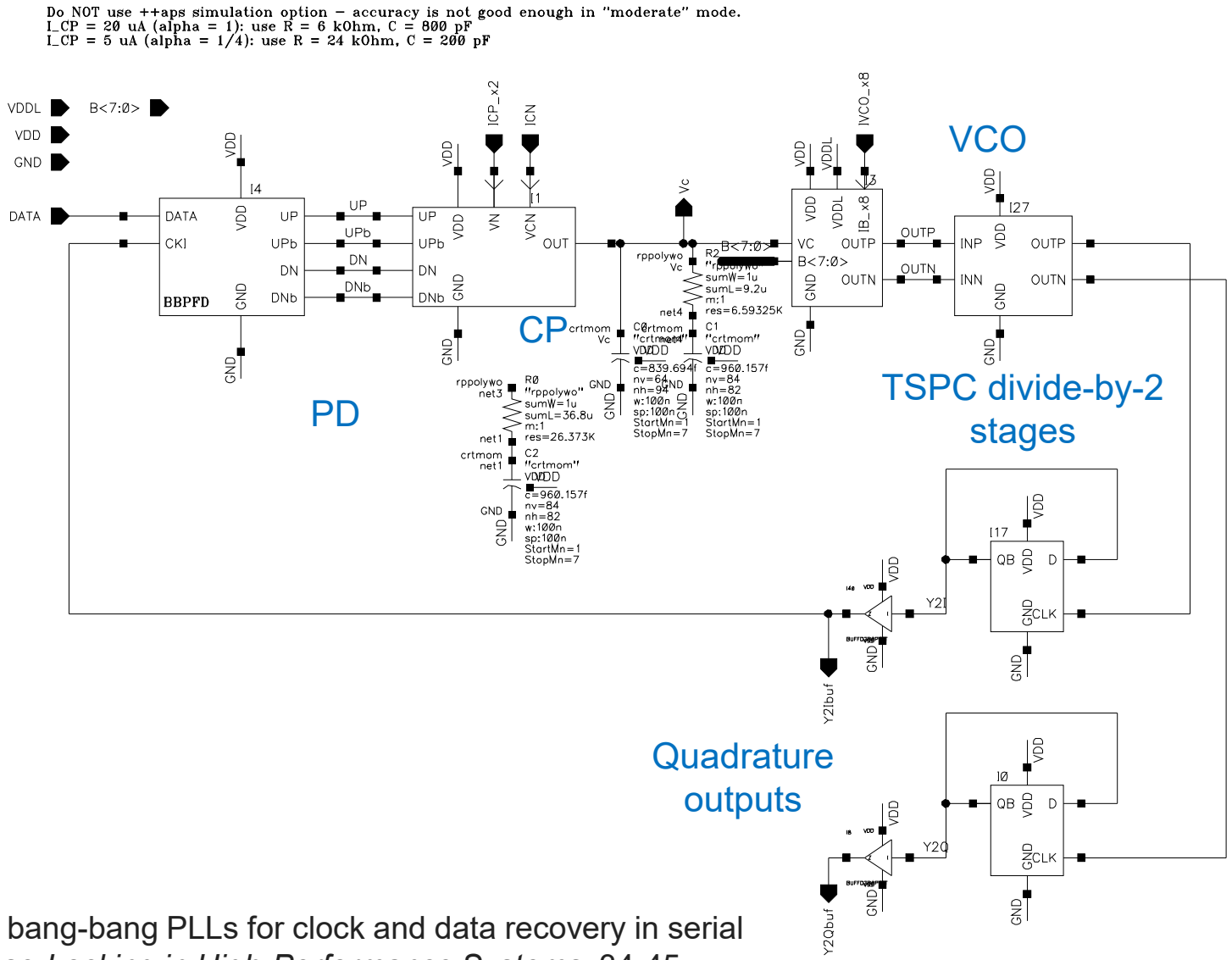


Basic Alexander PD
(using TSPC flip-flops)

Park, K., & Jeong, D. K. (2020). Analysis of frequency detection capability of Alexander phase detector. *Electronics Letters*, *56*(4), 180-182.

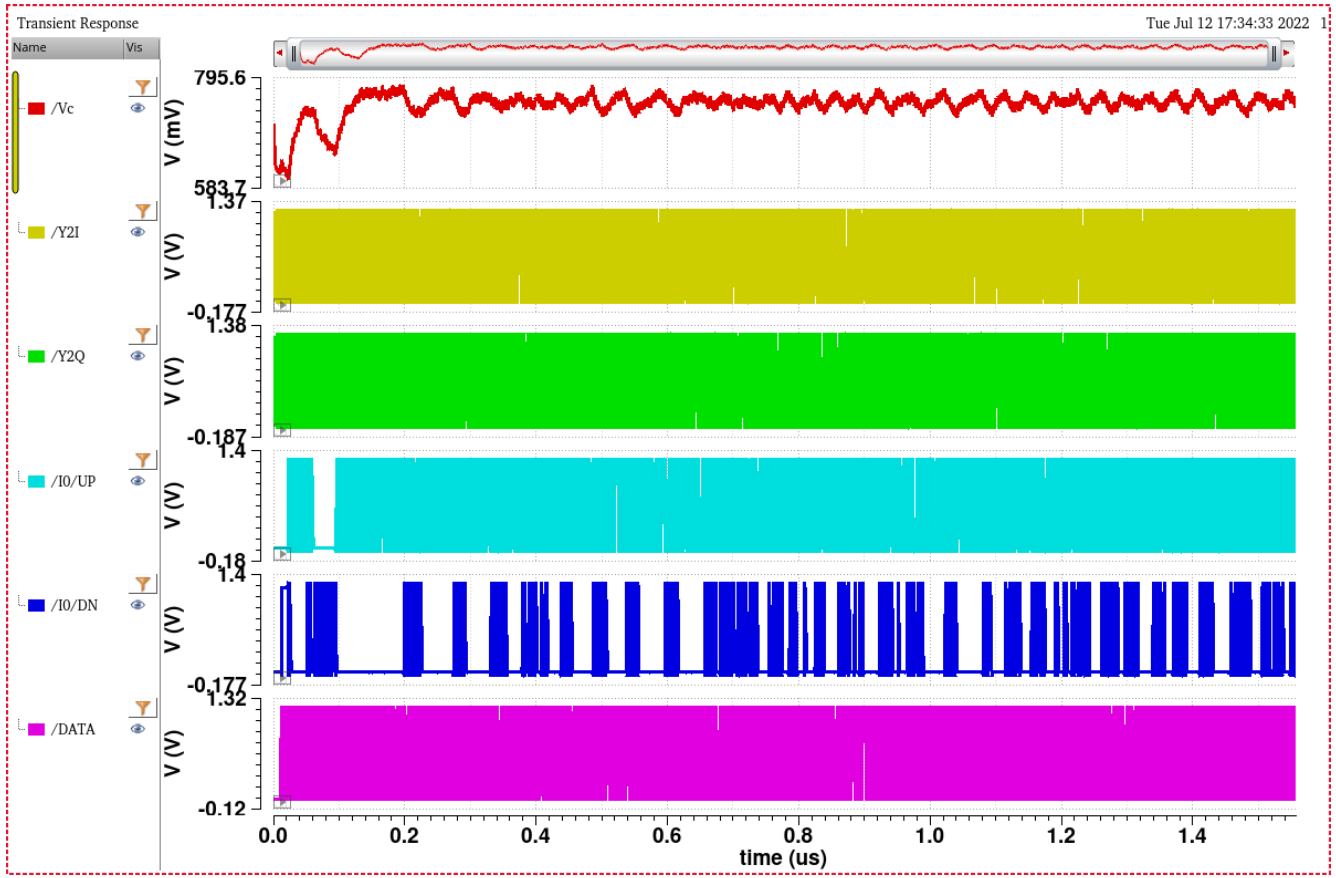
Complete CDR design

- Dynamics are fundamentally nonlinear due to the high gain of the bang-bang PD.
- Fixed passive second-order loop filter used for simplicity.
- The charge pump bias current I_{CP} acts as a free parameter for adjusting the CDR loop dynamics.
  - If I_{CP} is scaled by α, scaling the loop filter resistance and capacitance by 1/α and α, respectively, should result in similar stability properties.

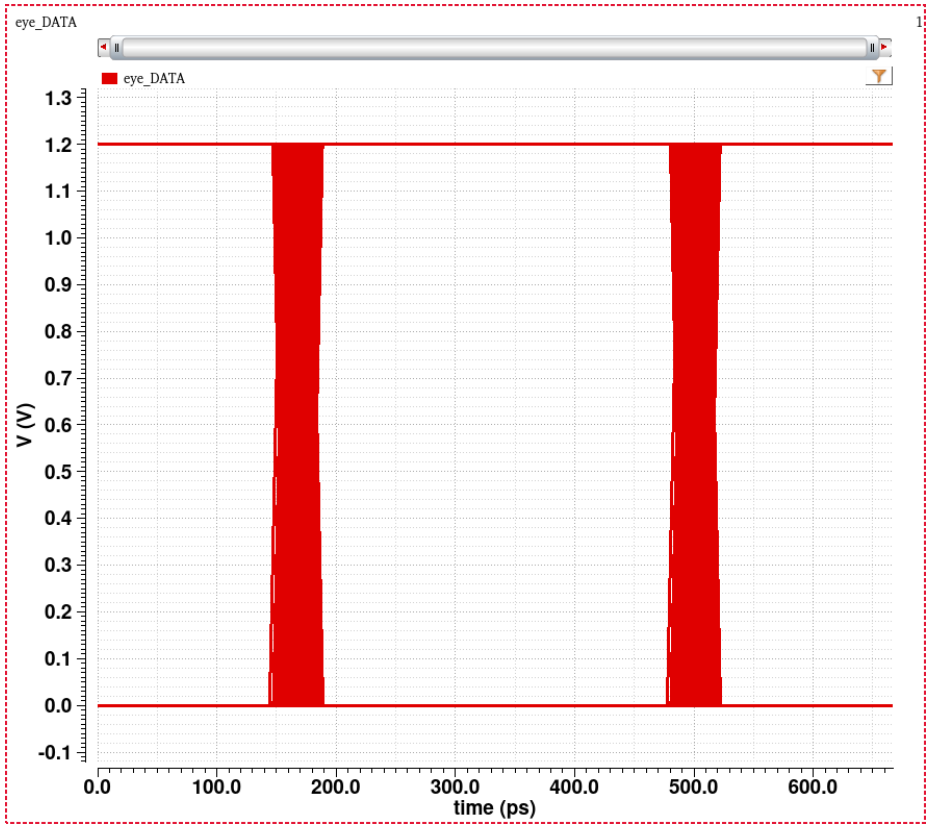


Walker, R. C. (2003). Designing bang-bang PLLs for clock and data recovery in serial data transmission systems. *Phase-Locking in High-Performance Systems*, 34-45.

Simulation of the CDR (I_{CP} = 20 µA, α = 1)



Main waveforms, data rate = 3 Gb/s (PRBS-31 input)



Eye diagram after locking (dominated by assumed input jitter of 20 ps_{rms})

- Initial loop filter voltage (V_c) set below the set point to ensure that the initial frequency error is negative.
- Lock time ~200 ns, little cycle slipping observed due to frequency detection within the PD.

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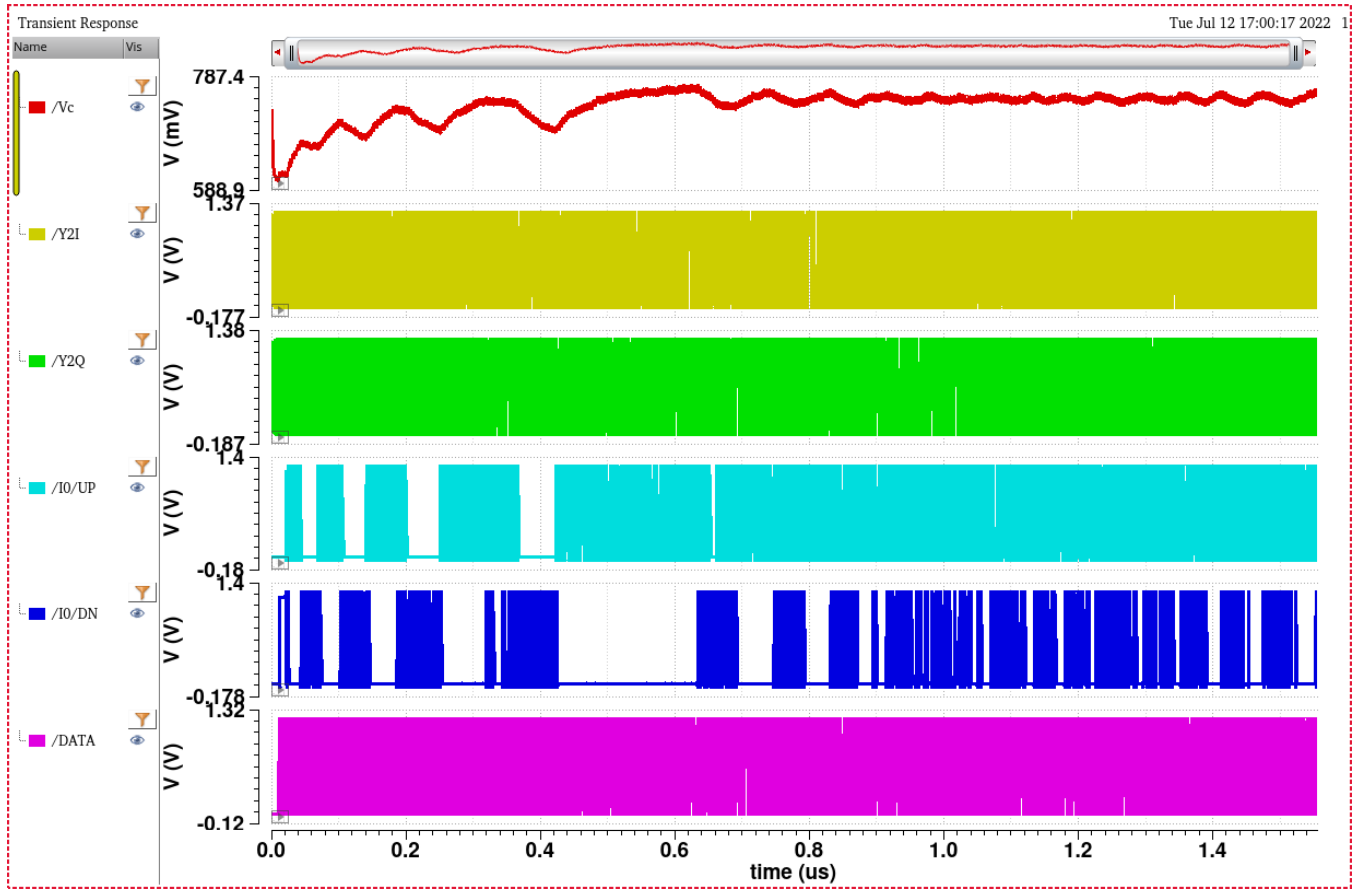
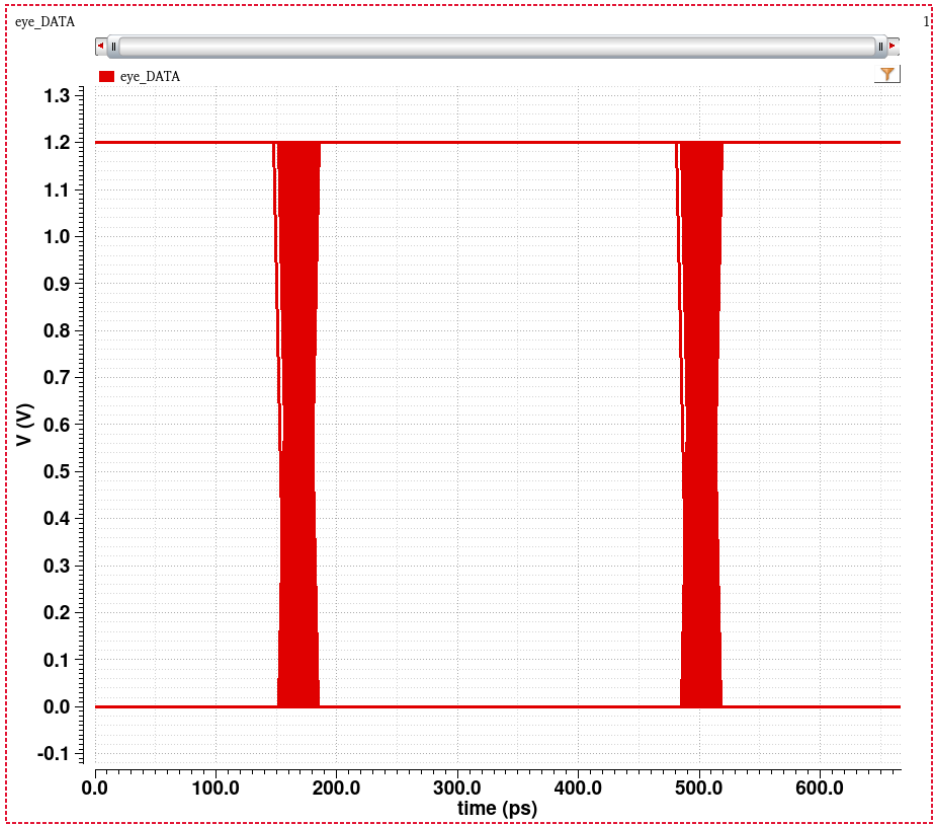
Simulation of the CDR (I_{CP} = 5 µA, α = 1/4)



Main waveforms, data rate = 3 Gb/s (PRBS-31 input)



Eye diagram after locking (dominated by assumed input jitter of 20 ps_{rms})

- Initial loop filter voltage (V_c) set below the set point to ensure that the initial frequency error is negative.
- Lock time ~700 ns, little cycle slipping observed due to frequency detection within the PD.

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On-chip LDO design

Effects of supply noise on oscillator stability

- All oscillators exhibit frequency “pulling” with respect to the power supply.
- Thus, supply noise (e.g., due to an LDO) will result in instantaneous frequency fluctuations that increase oscillator phase noise (PN), while supply ripples will generate output spurs.
- This effect can be analyzed by assuming that only white noise sources are significant; this is valid in the $1/f^2$ region of the PN spectrum.

IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS—I: REGULAR PAPERS, VOL. 67, NO. 12, DECEMBER 2020

Analysis and Design of Power Supply Circuits for RF Oscillators

Alessandro Urso, *Student Member, IEEE*, Yue Chen, *Student Member, IEEE*, Johan F. Dijkhuis, *Member, IEEE*, Yao-Hong Liu, *Senior Member, IEEE*, Masoud Babaie, *Member, IEEE*, and Wouter A. Serdijn, *Fellow, IEEE*

Example:

- For I_L = 1 mA, C_{fly} = 0.01 µF, and f_{clk} = 10 MHz, we get V_{ripple} = 10 mV.
- Assume K_v = 0.38 GHz/V.
- Prediction: Need PSRR > 36 dB @ 10 MHz to keep S_{spur} < -60 dBc.

Sinusoidal ripple, $v(t) = V_m \sin(2\pi f_m t)$:

$$S_{spur} = 10\log_{10}\left(\frac{K_V V_m}{2 f_m}\right)^2$$

Typical switched-capacitor DC-DC converter:

$$V_{ripple} = \frac{I_L}{C_{fly} f_{clk}} \text{ (sawtooth)} \Rightarrow V_{ripple}(f_{clk}) = \frac{V_{ripple}}{\pi}$$

Required PSRR for LDO:

$$PSRR = \frac{V_{ripple}(f_{clk})}{V_m} = \frac{I_L K_V}{2\pi C_{fly} f_{clk}^2 10^{(S_{spur}/20)}}.$$

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Effects of supply noise on oscillator stability

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- Thus, supply noise (e.g., due to an LDO) will result in instantaneous frequency fluctuations that increase oscillator phase noise (PN), while supply ripples will generate output spurs.
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Example:

- For FOM = 190 dBc/Hz and P_{DC} = 1 mW, we get L(Δf) = -114 dBc/Hz @ 1 MHz offset.
- Assume K_v = 0.38 GHz/V.
- Prediction: Need v_n < 5.0 nV/Hz$^{1/2}$ @ 1 MHz to keep $L_{sup}(\Delta f) < L(\Delta f)$, i.e., avoid PN degradation.

Leeson's phase noise model ($1/f^2$ region):

$$\mathcal{L}(\Delta f) = 10\log_{10}\left(\frac{10^{-FOM/10}}{10^3 P_{DC}}\left(\frac{f_0}{\Delta f}\right)^2\right)$$

$FOM \approx 190 - 195$ dBc/Hz for CMOS LC VCOs

PN induced by power supply noise:

$$\mathcal{L}_{sup}(\Delta f) = 10\log_{10}\left(\overline{v_{n,sup}^2(\Delta f)}\left(\frac{K_V}{\Delta f}\right)^2\right)$$

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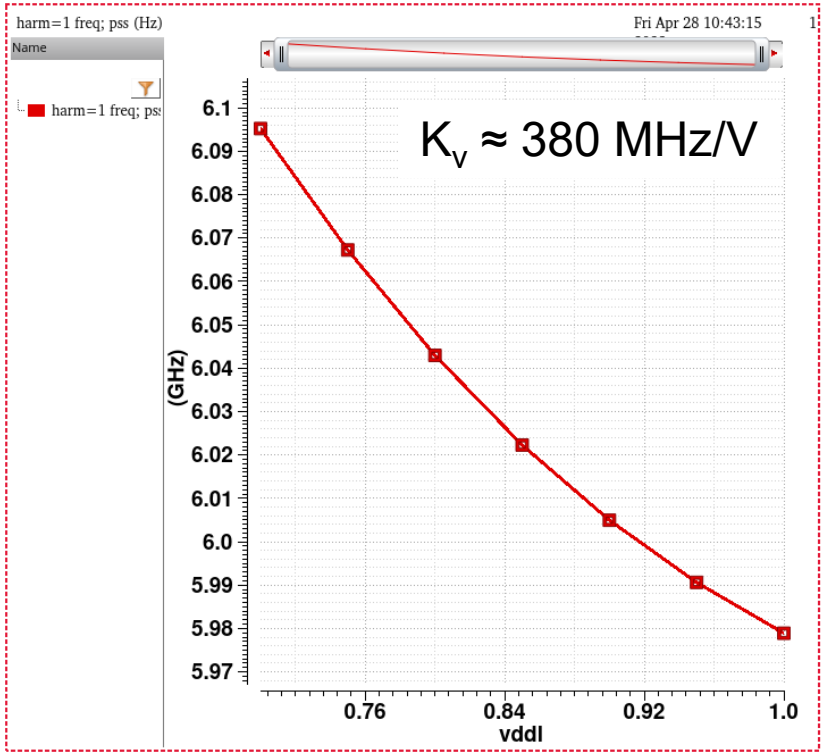
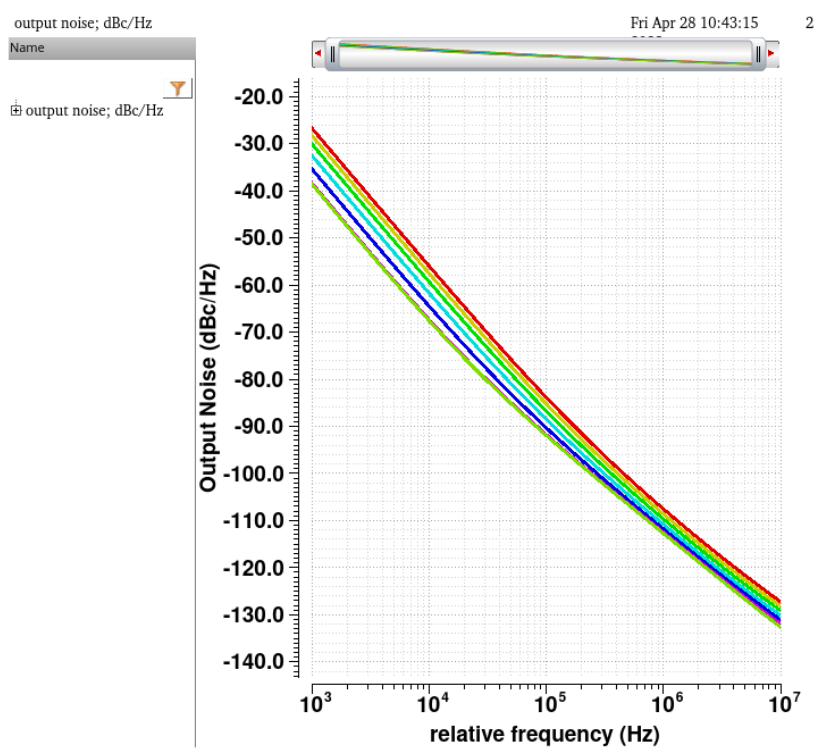
Example: LC VCO at 6 GHz (2)

- Multi-band LC VCO design for use in an integer-*N* frequency synthesizer. Two power supplies:
  - Main V_{DD} (V_{DDL} ≈ 0.8V) fed into the VCO core through the center-tap of a symmetric inductor.
  - Auxiliary V_{DD} (V_{DD} ≈ 1.2V) used by 1) the CMOS inverter-based output buffers, 2) the control signals for the band-adjust switches.
- PSS, PAC, and PNOISE simulations were used to estimate supply pulling and the PN power spectrum versus changes in both V_{DDL} and V_{DD}.

V_{DDL} sweep
(0.7 – 1.0 V)

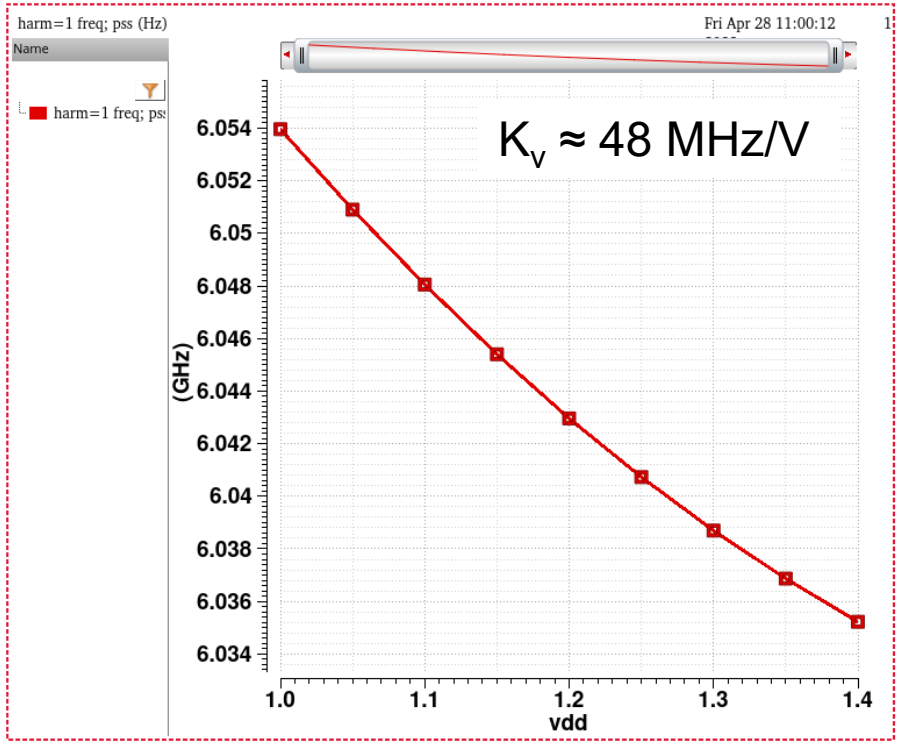


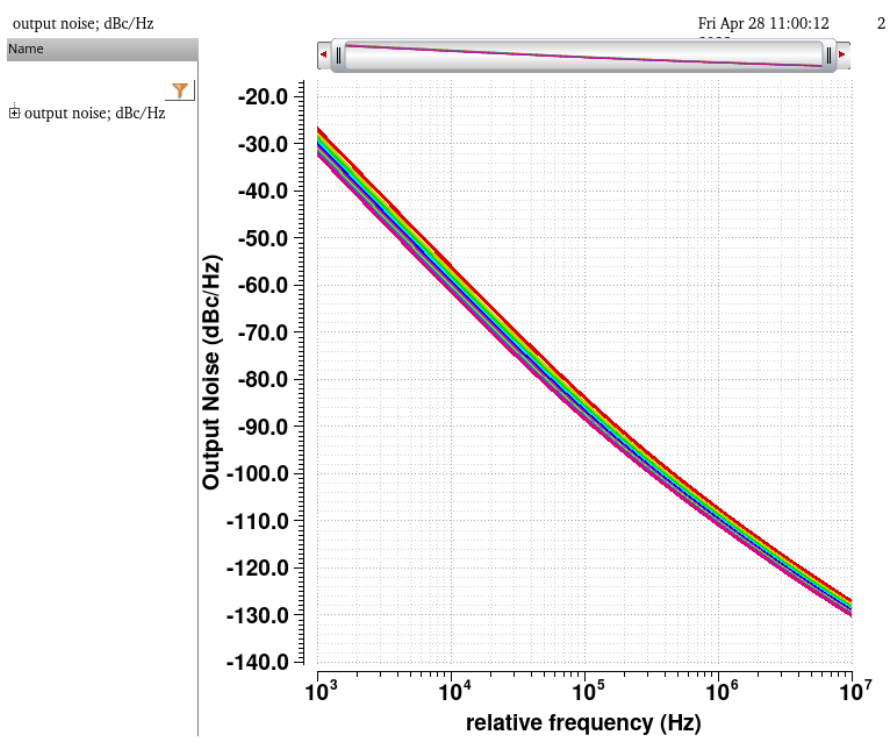


Example: LC VCO at 6 GHz

- Multi-band LC VCO design for use in an integer-*N* frequency synthesizer. Two power supplies:
  - Main V_{DD} (V_{DDL} ≈ 0.8V) fed into the VCO core through the center-tap of a symmetric inductor.
  - Auxiliary V_{DD} (V_{DD} ≈ 1.2V) used by 1) the CMOS inverter-based output buffers, 2) the control signals for the band-adjust switches.
- PSS, PAC, and PNOISE simulations were used to estimate supply pulling and the PN power spectrum versus changes in both V_{DDL} and V_{DD}.

V_{DD} sweep
(1.0 – 1.4 V)





High-PSRR on-chip LDO design

- The supply sensitivity of *LC* oscillators, while much lower than that of ring oscillators, can still result in significant phase noise degradation due to power supply noise and/or ripple.
- The preferred solution is to run the VCO (and possibly also the VCO buffer) off its own high-PSRR regulated power supply, i.e., a low-dropout (LDO) on-chip voltage regulator.
  - The PSRR of the proposed LDO is improved over a broad frequency range via an auxiliary (AUX) amplifier for adaptive feed-forward ripple cancellation (FFRC).
  - In addition, an NMOS power transistor is used to ensure low dropout voltage (< 100 mV at 100 mA load) and low overshoot/undershoot during transients.

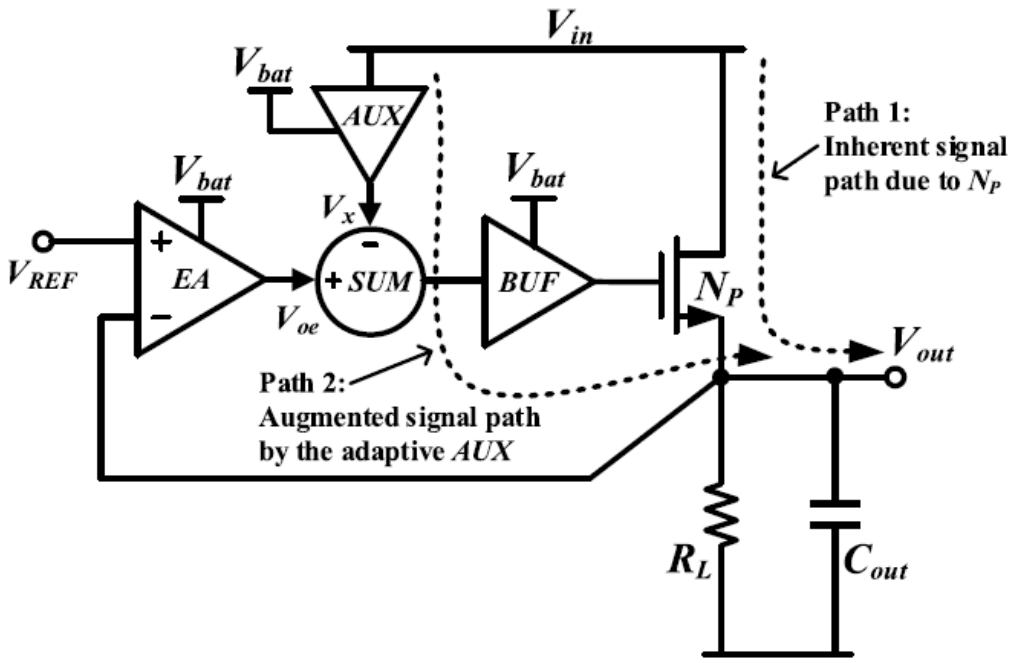
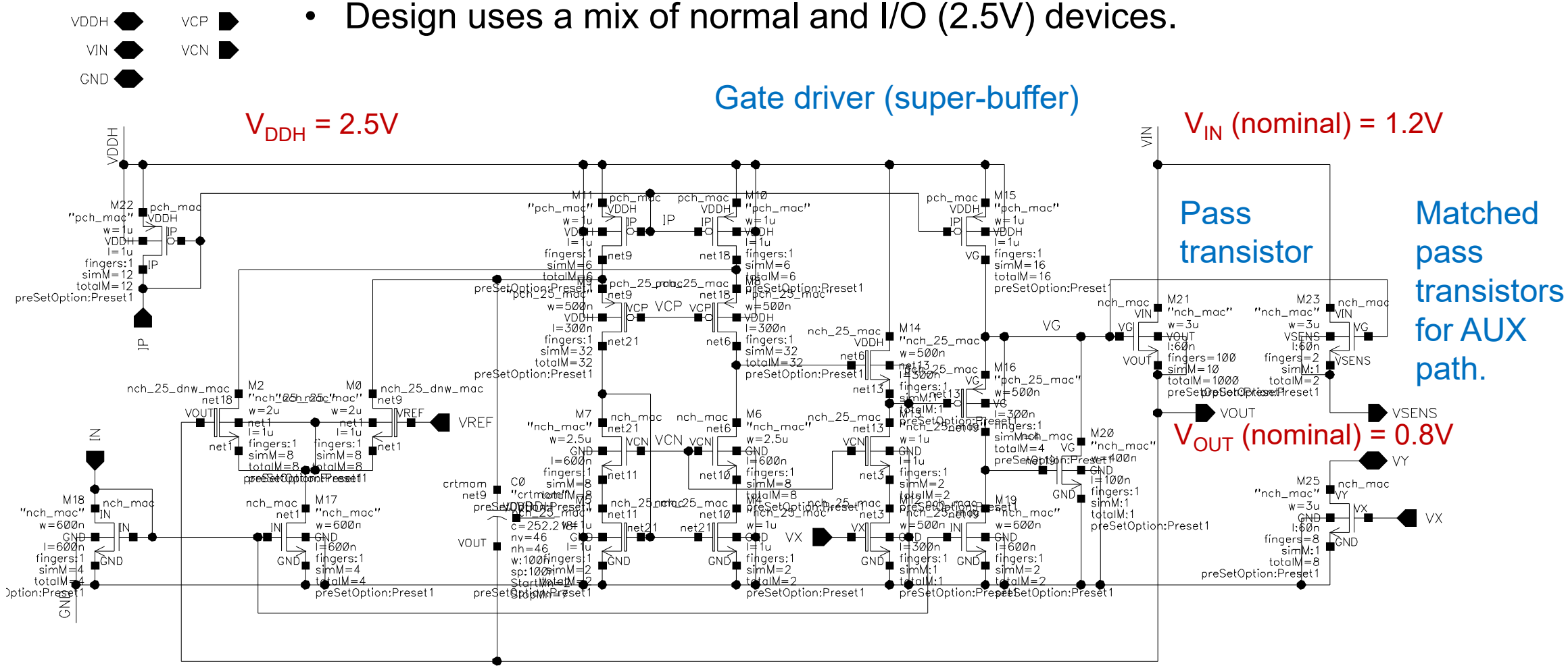


Fig. 2. Conceptual block diagram of the LDO.

Jiang, J., Shu, W., & Chang, J. S. (2018). A 65-nm CMOS low dropout regulator featuring> 60-dB PSRR over 10-MHz frequency range and 100-mA load current range. *IEEE Journal of Solid-State Circuits*, *53*(8), 2331-2342.

LDO schematic: main amplifier

- Design uses a mix of normal and I/O (2.5V) devices.



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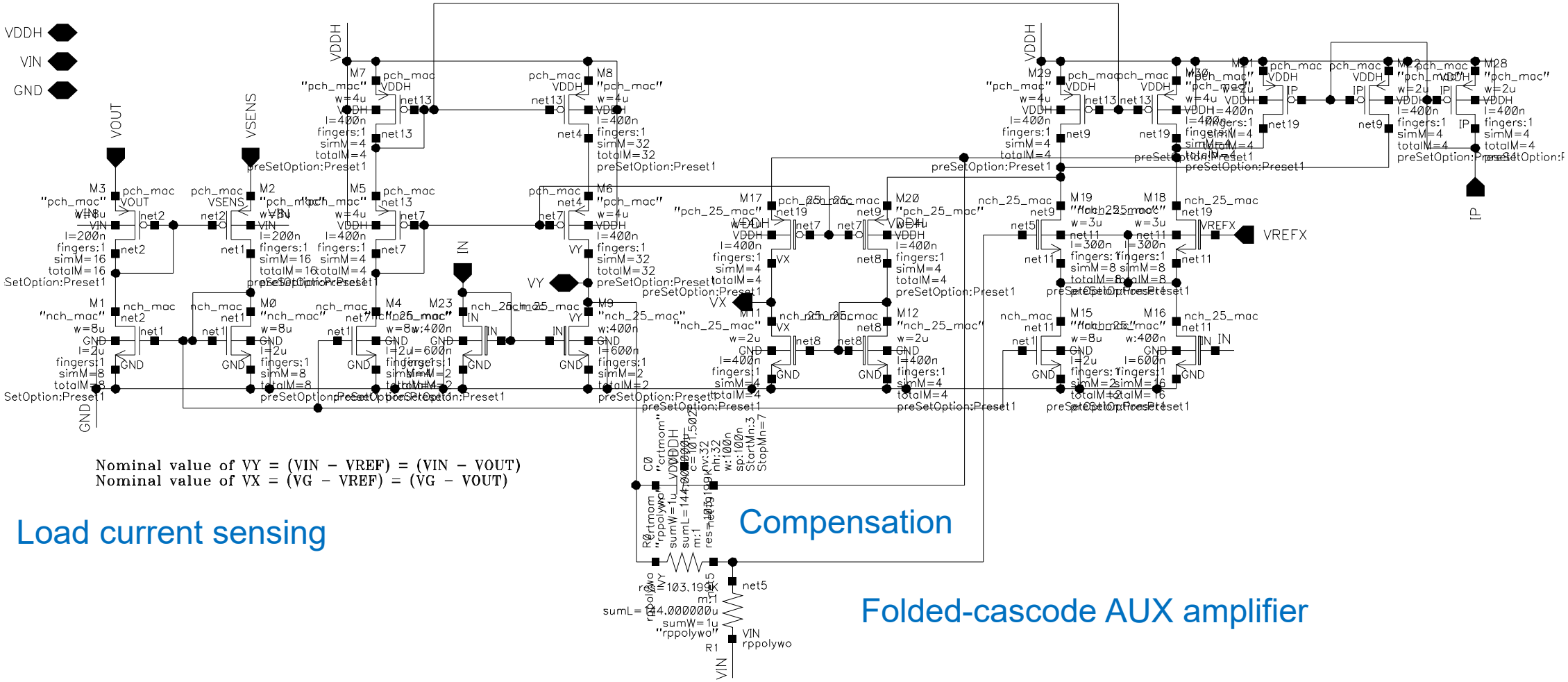
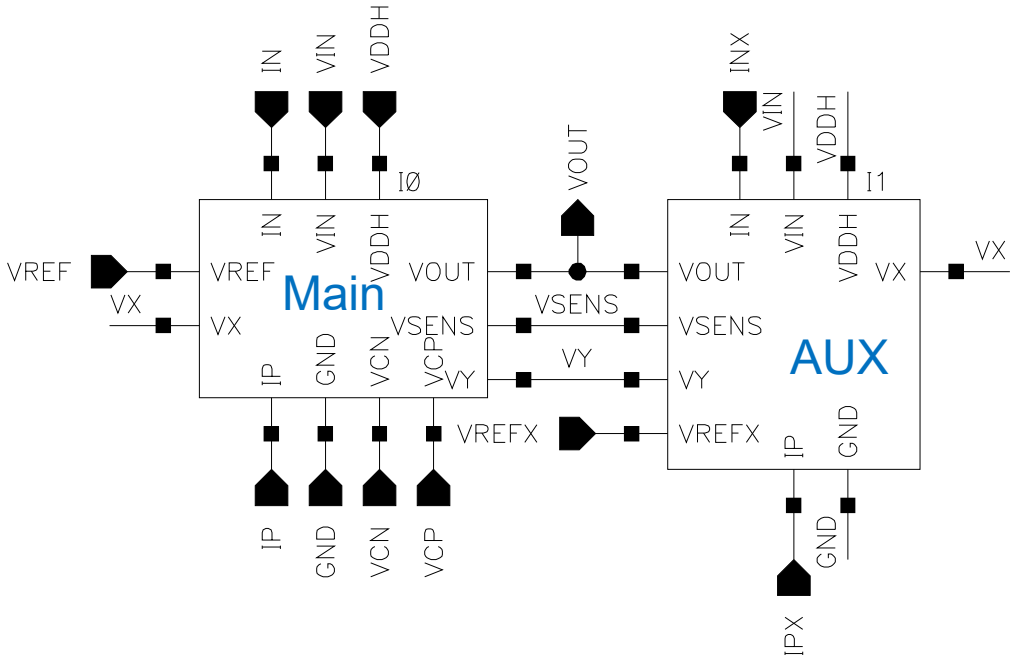
LDO schematic: auxiliary (AUX) amplifier

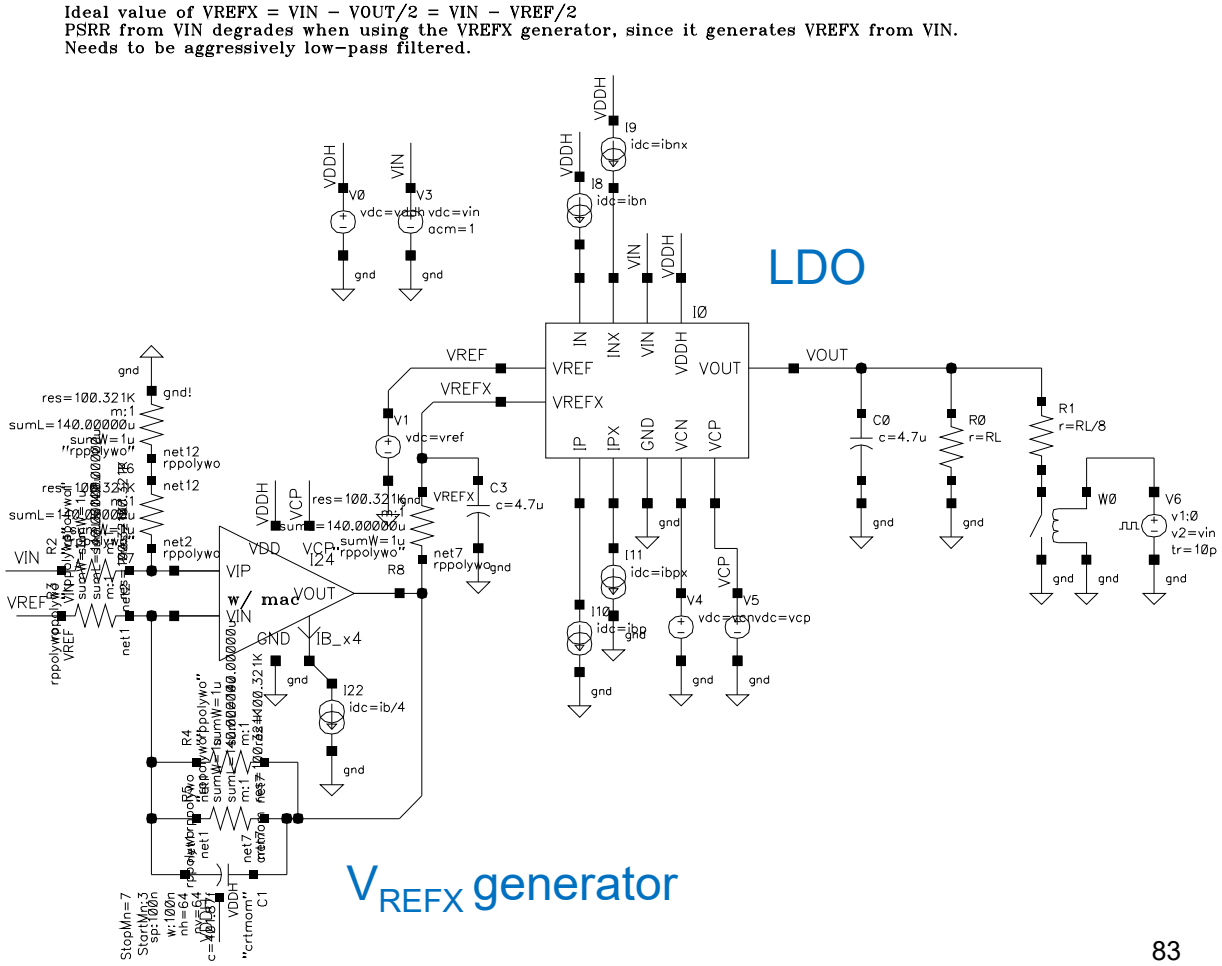


Complete LDO design and test bench

- An additional op-amp is used to generate the reference voltage for the AUX amplifier, which should be $V_{REFX} = V_{IN} - V_{OUT}/2$ for optimal feed-forward cancellation.

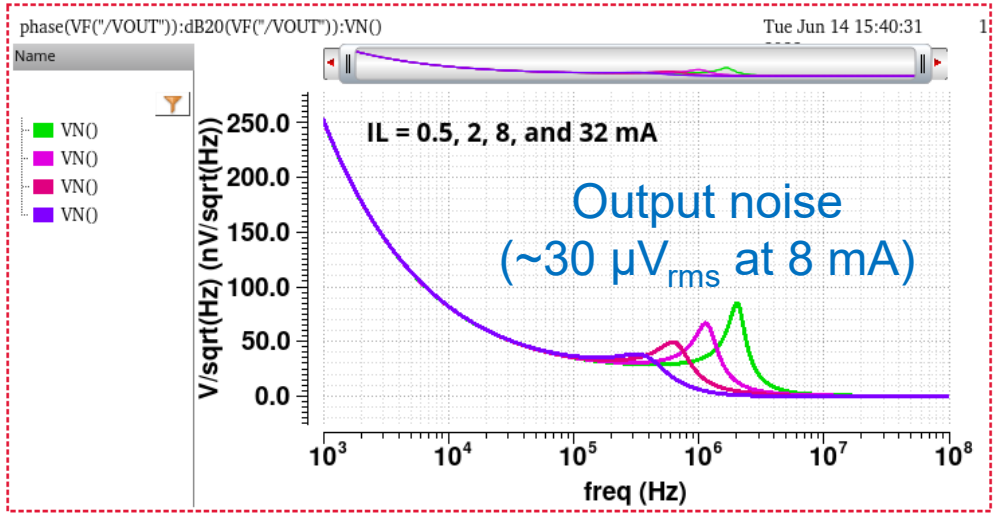


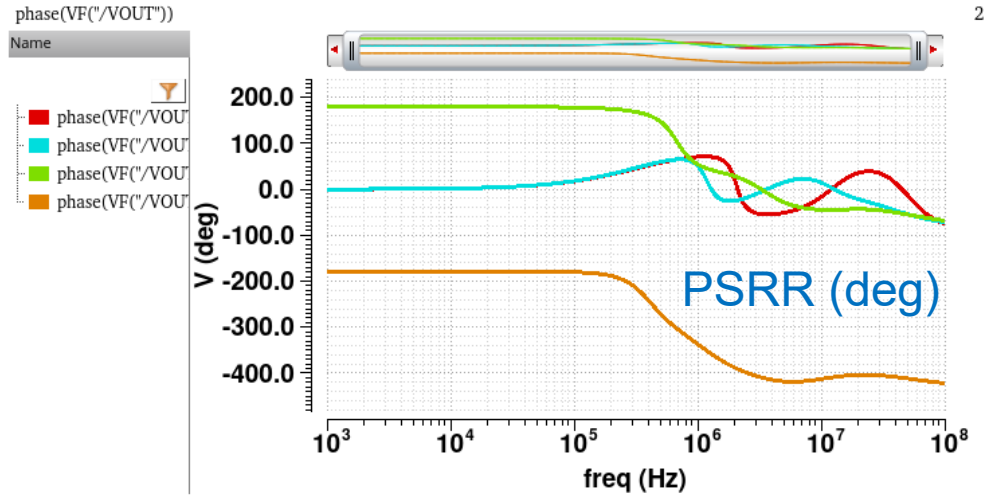
Top-level LDO schematic

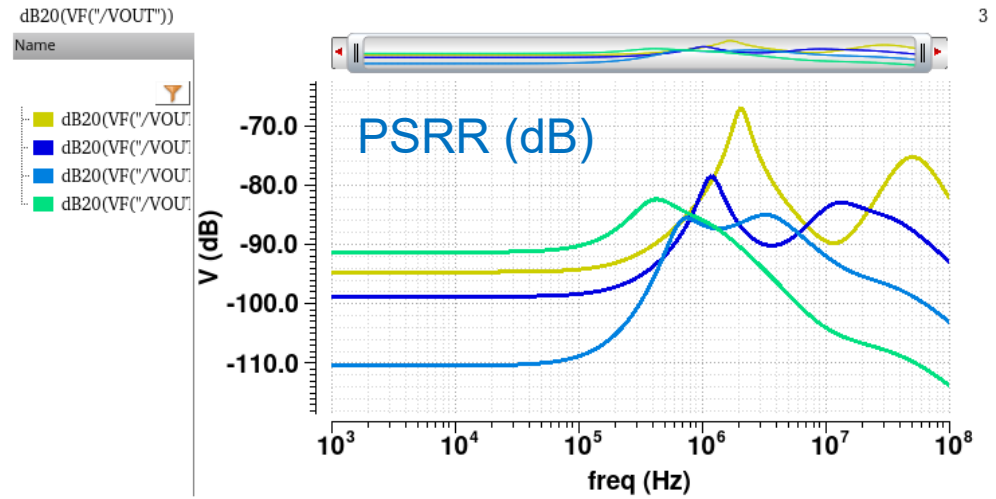


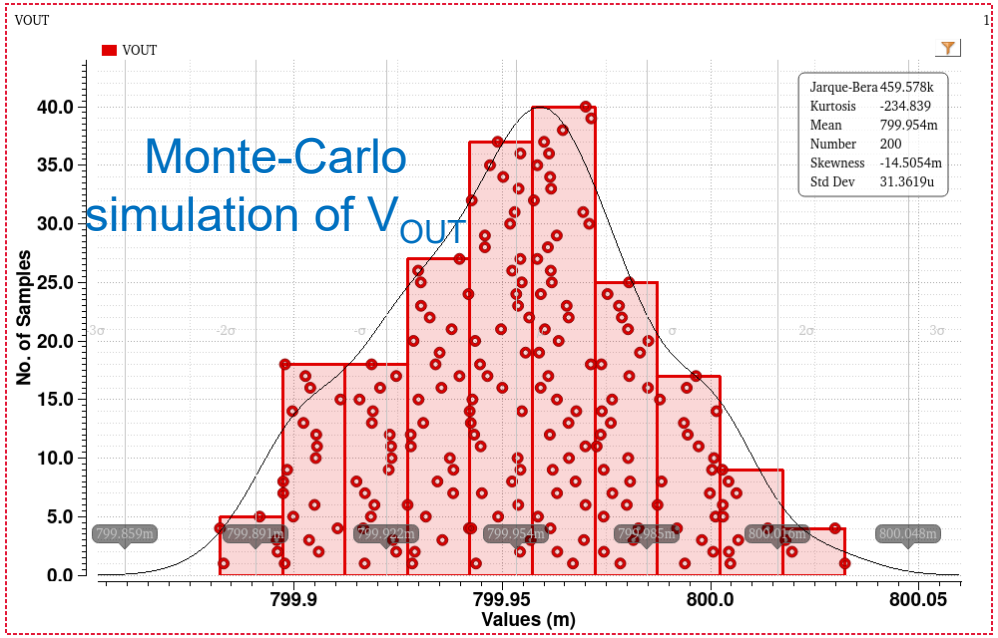
V_{REFX} generator

LDO simulation results (V_{OUT} = 0.8V)









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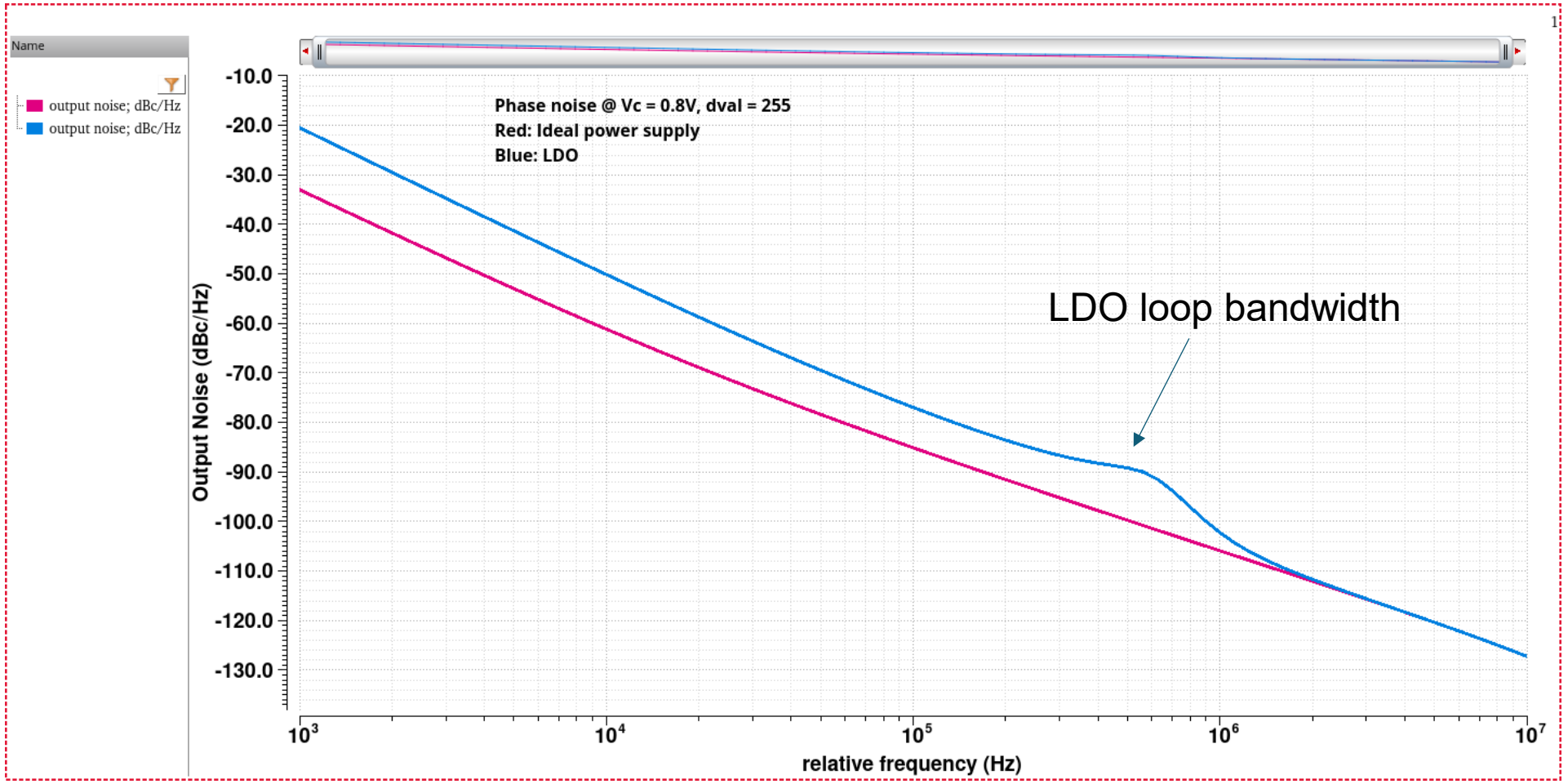
PSRR >70 dB up to 100MHz
for all load currents

Effect of the LDO on VCO phase noise

- We observe ~10 dB degradation in close-in phase noise due to the output noise of the LDO.



Potential design improvements

- Using a PFD with increased linear range.
  - Provides improved settling time (e.g., for large frequency steps) by eliminating cycle slips.
- Using a dual-path loop filter (LF).
  - Enables the proportional (P) and integral (I) terms in the LF transfer function to be independently set.
  - However, adding together the outputs of these paths generally requires use of the current domain, which in turn imposes additional I-V and V-I conversions.
- Modifying the PLL architecture to improve its radiation hardness.
  - The lpGBT group has performed extensive research in this area. TMR has been used for the digital blocks, while the VCO design has been modified to minimize its LET cross-section.
  - Nevertheless, large and slowly-decaying phase transients after each radiation event are inevitable due to the limited PLL loop bandwidth.
  - Our idea: Instead of hardening individual components within a single PLL, use multiple PLLs scattered across the chip and perform majority voting on their outputs. This novel approach has the potential to completely eliminate radiation-induced phase transients.

Next steps

- Implement and verify the proposed design improvements, in particular the use of redundant PLLs to eliminate phase transients due to SEUs.
- Simulate performance at cryogenic temperatures (using 77K device models).
  - Cryogenic models for 2.5V transistors are not available, so simulations of certain blocks (e.g., the LDO) may not be possible.