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An Integer-N Frequency Synthesizer for Flexible On-Chip Clock Generation

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Many high-energy physics experiments require high-data-rate links between readout ASICs and digital back-end processors over lossy channels, such as radio-pure cables. The preferred solution uses a forwarded clock architecture in which the back-end transfers a low-frequency reference clock (e.g., from a crystal oscillator) to the readout system over a low-speed cable, which is then used by a frequency synthesizer to generate the high-frequency data-rate clock. Here we describe an integer-N synthesizer in 65nm CMOS technology suitable for such applications. The circuit can be programmed to generate low-jitter clocks between 30MHz and 4GHz that are locked a 10-50 MHz reference input.

Summary (500 words)

Fig. 1 shows a top-level block diagram of the proposed synthesizer. The design uses a phase-locked loop (PLL) with programmable feedback and output dividers. The PLL has a classical structure with an edge-triggered sequential phase-frequency detector (PFD), differential charge pump (CP), passive RC loop filter, voltage-controlled oscillator (VCO), feedback frequency divider, and lock detector (LD). The CP uses an adaptive replica-bias loop to improve matching between the P- and N-sides, i.e., reduce offset.

The VCO, which is shown in Fig. 2, uses an on-chip LC resonator and cross-coupled NMOS pair. Coarse tuning (band switching) is provided by 8 equal-valued switched capacitors, while fine tuning is provided by accumulation-mode MOS varactors. Phase noise is minimized by using 1) an RC low-pass filter to remove bias current noise, and 2) an LC tail current filter (tuned to the second harmonic) to reduce 1/f noise up-conversion. Power consumption is minimized by operating the VCO at a reduced supply voltage, VDDL. The total tuning range is 5.6-8.6 GHz with a control gain of ~0.6GHz/V and a typical phase noise of −110 dBc/Hz at 1MHz offset. The differential VCO outputs are converted to logic-level signals by self-biased buffers (consisting of AC-coupled CMOS inverters with resistive feedback), thus ensuring insensitivity to the common-mode level.

The feedback divider uses a standard pulse-swallow counter topology with a total division ratio of (NP+S), where N=2 is fixed while P and S are adjustable over the ranges 1-63 and 0-15, respectively. Propagation delays are minimized by using dynamic (TSPC) flip-flops within the N/(N + 1) dual-modulus prescaler and a one-level carry select adder within the programmable counter. The divider output is further divided by 2 to ensure that the recovered clock signal, CLK, has a 50% duty cycle.

Fig. 3 shows a schematic of the LD circuit, which detects when total time-averaged duty cycle of the PFD UP and DN outputs, D, is less than a fixed threshold value, Dmin. The value of Dmin is determined by two dimensionless quantities, namely the normalized threshold voltage of the Schmitt trigger and the ratio R1/R2, and is thus robust to changes in process, voltage, and temperature.

Fig. 4 shows a block diagram of the programmable output divider. It uses a cascade of stages with smaller division ratios, as shown in the figure. The design allows a wide range of divide values from 1-160 (including most composite numbers <32) to be generated while maintaining an output duty cycle close to 50%. Note that individual stages are bypassed by transmission gate multiplexers when in “divide by 1”mode.

The complete synthesizer uses dual output dividers to allow generation of two programmable output frequencies from the quadrature outputs of the PLL and a standard two-wire I2C serial interface for programming. The overall die area is 450µm×500µm, of which ~50% and ~25% are occupied by the VCO and main loop filter

capacitor, respectively. The nominal power consumption (VDD=1.2V, VDDL=0.8V) is 4.0mW. Fig. 5 shows a die photograph of the fabricated synthesizer, which is currently being tested.

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