The Energy Measurement ASIC for the Upgrade II in the LHCb Calorimeter Detector

Abstract (max 100 words):

This work presents the design of a 4-channel ASIC developed in a 65 nm CMOS technology specifically designed to measure the energy captured by the PMTs in the LHCb Upgrade II Calorimeter. The processing chain stands on rail-to-rail fully differential blocks that improve the common noise rejection and maximize the voltage range. A dual gain structure is adopted to extend the dynamic range up to 12 bits. Each gain path is based on two time-interleaved subchannels that remove the dead time of the switched integrators. A dedicated phase-lock loop (PLL) generates the necessary clock signals to synchronize each channel independently.

Summary (max 500 words):

The Front-End Board (FEB) is expected to measure the photoelectrons' energy and arrival time using two different ASICs. The radiation level inside the detector binds the design to a high-radiation resilient technology, such as TSMC65, in addition to its advantages regarding matching the analog and digital internal blocks of the FEB. This work summarizes the ASIC for the energy measurement.

The low voltage supply in this technology (1.2V) imposes a stringent noise specification in order to achieve a 12-bit precision required at the channel output. For that purpose, a two-gain scheme has been adopted. It consists of a Low-Gain (LG) path, using a unity gain preamplifier that achieves 11 bits at the chain's output, and a High-Gain (HG) that increases the measured resolution against low-amplitude input signals. Following the design in the ICECAL ASIC already installed in the Upgrade I of the LHCb calorimeter, both paths are based on two time-interleaved subchannels that grant the signal integration to reset between input events and the removal of dead time to prevent sample losses. It is accurately synchronized by adding a Phase Locked Loop (PLL) that generates the 40 MHz integrator clocks individually per channel with a phase calibration resolution below 1 ns.

Each of these subchannels is based on a processing chain comprised of (1) a voltage preamplifier, (2) a configurable pole-zero cancellation circuit to mitigate the effect of the spillover generated by the different detector technologies (Shaslink, SPACAL-W, and SPACAL-Pb), (3) an integrator with a tunable time constant τ, and (4) a high-slew-rate track-and-hold based on the bottom plate sampling technique. All these blocks are built with a fully-differential rail-to-rail (RTR) amplifier with high-performance specifications which has been particularly designed for this ASIC with: (1) an equalized RTR input stage loaded with a folded cascode to achieve constant GBW along the whole common-mode (CM) input range (~ 500 MHz) and a high open-loop gain (A_{v0} ~ 85 dB); (2) a class-AB output to maintain the RTR swing at the output; (3) a common-mode feedback amplifier (CMFB) that ensures a minimum deviation from the CM output level. This amplifier has a power consumption below 3 mW, achieving a slew rate above 500 V/µs and an integrated noise in the range of operation ~300 μV_{rms}.

The circuit simulations of the full analog channel report power consumption of ~ 40mW/channel, complying with the requirements regarding: (1) an output noise that grants a 12-bit equivalent precision; (2) a linearity error below 1LSB against input signals with amplitude up to 1.1V in the LG path; (3) an integrator output stable for 4 ns with less than 1% variation; (4) and a minimum spillover of ~ 2.5% with the simulated detector.

Finally, the output signal from both LG and HG paths is driven to two fully-differential drivers with a capacitance drive capability up to 10 pF to output the analog signal to be digitized off-chip with an external 12 bits Analog-To-Digital Converter (ADC).

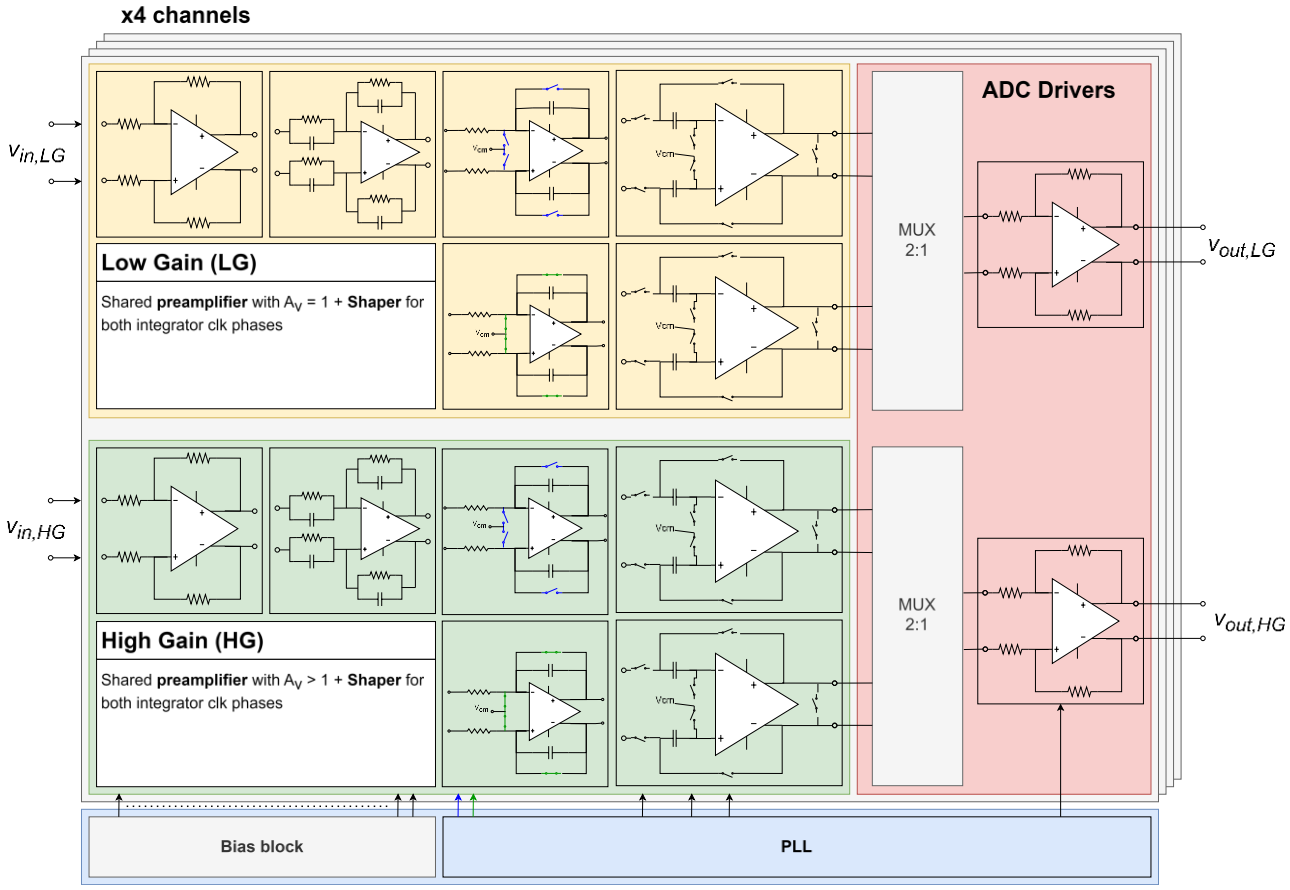

Figure 1. Block diagram of the energy measurement ASIC for LHCb Calorimeter Upgrade II