The Energy measurement ASIC for the Upgrade II in the LHCb Calorimeter Detector

TWEPP 2024 workshop on electronics for Particle Physics

University of Glasgow

Sept 30th-Oct 4th, 2024

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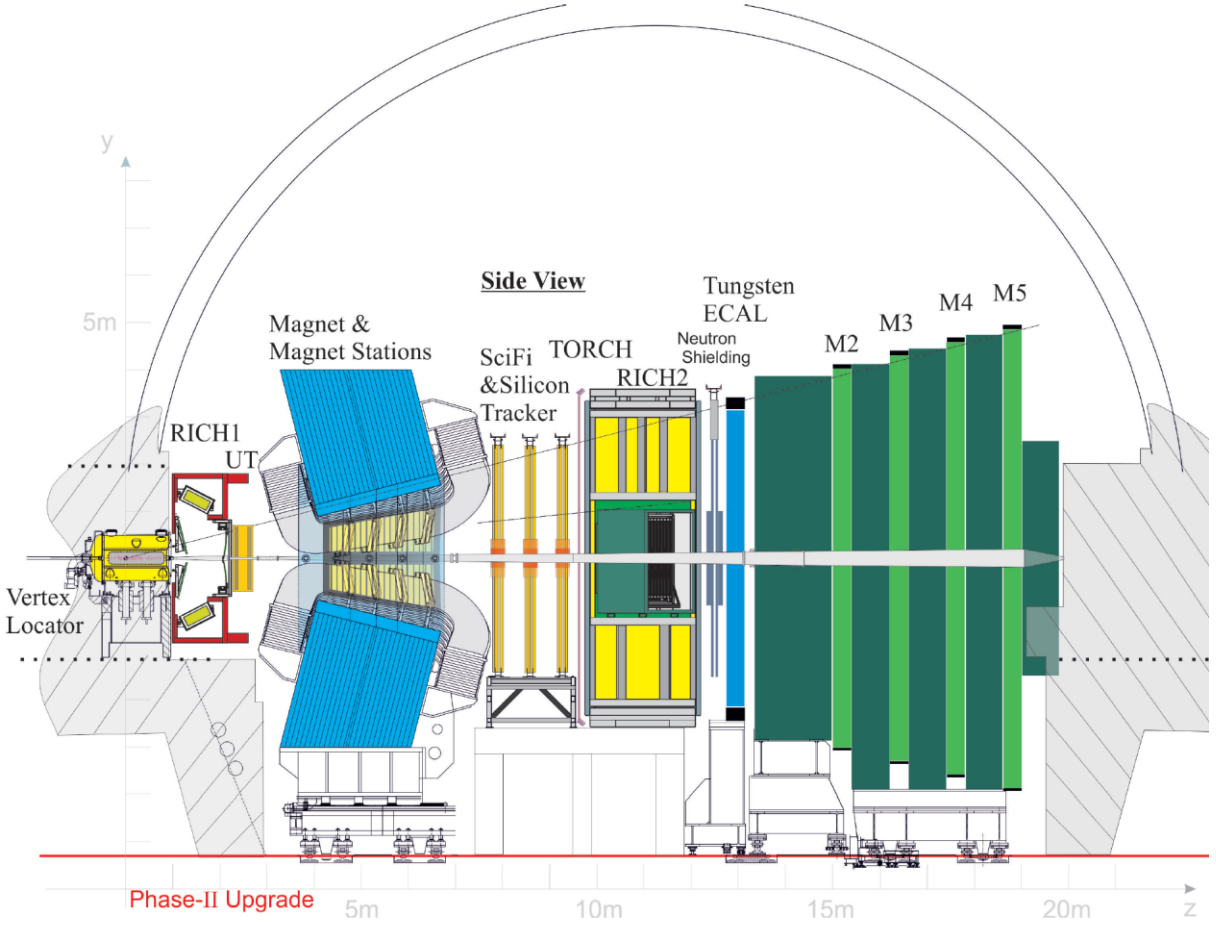
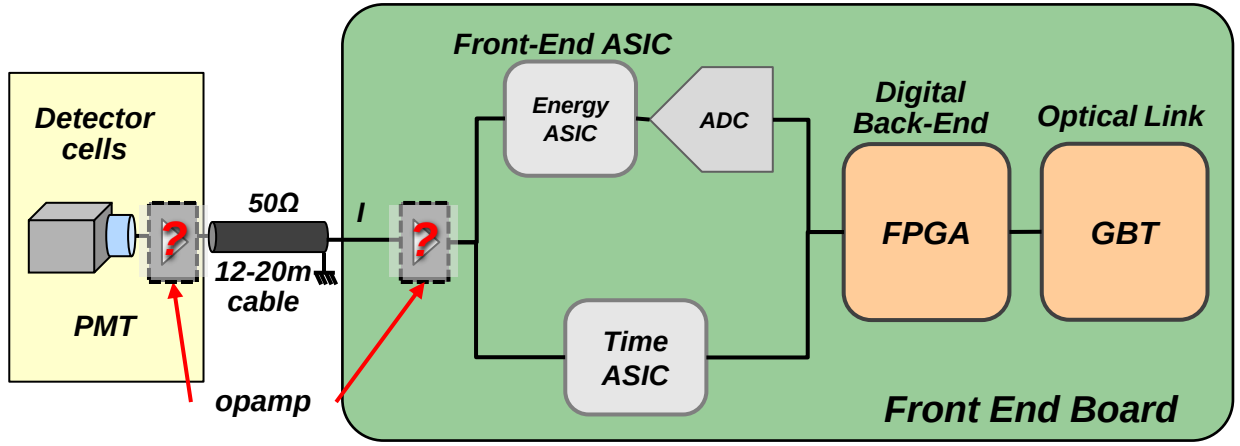


LHCb calorimeter detector

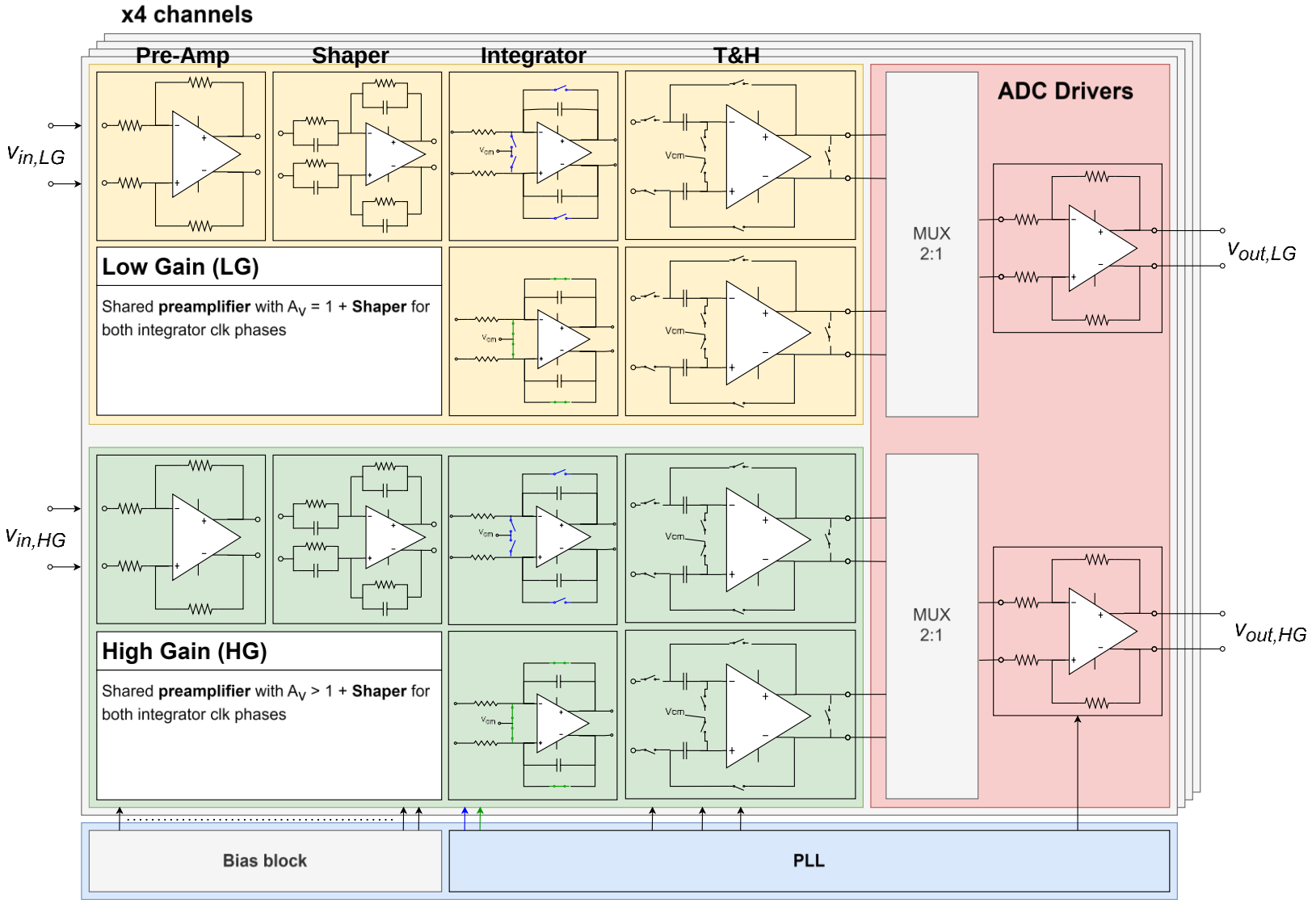
1. Introduction
1.1. ECAL Electronics Upgrade II



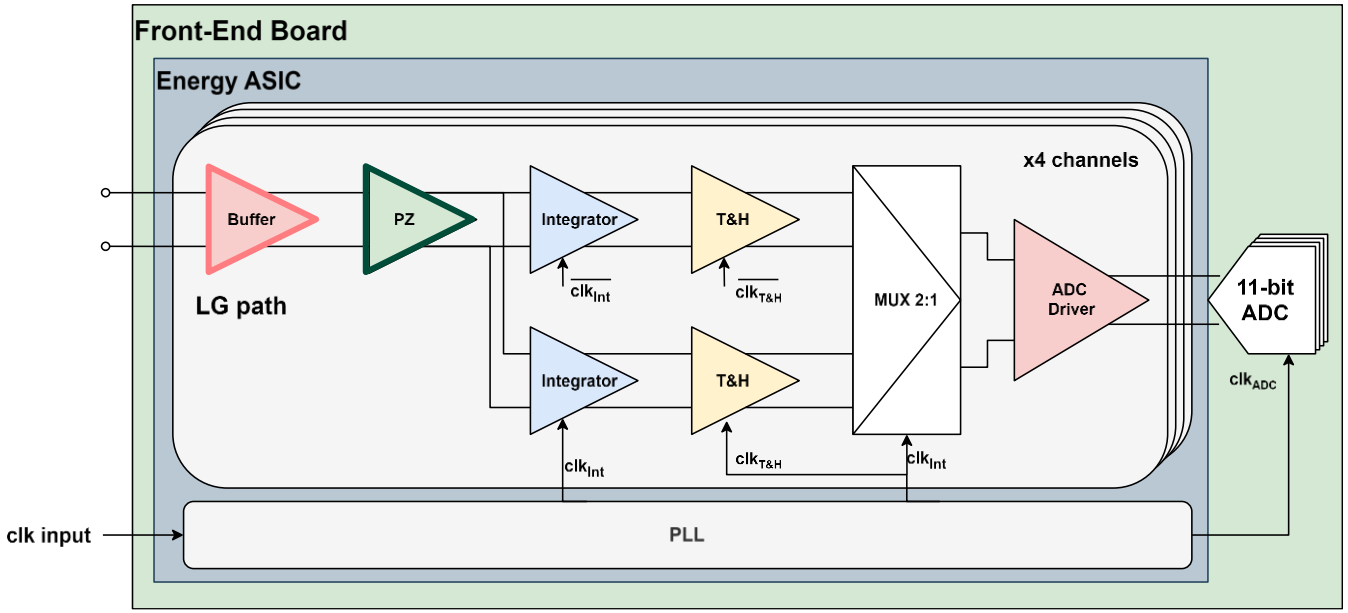
- Photodetectors readout solution follows the same scheme as in current ECAL:
  - PMT sensors near modules
- Signal conditioner circuit (COTS) to compensate cable attenuation, improve SNR, and reduce spill-over effort designed by IFIC
- ASIC/chipset in TSMC 65 nm with separate energy and timing paths.
  - Energy ASIC (ICECAL65) designed by UB, UPC and IFIC.
  - Timing ASIC (SPIDER) designed by IJC, LPC and IP2I.

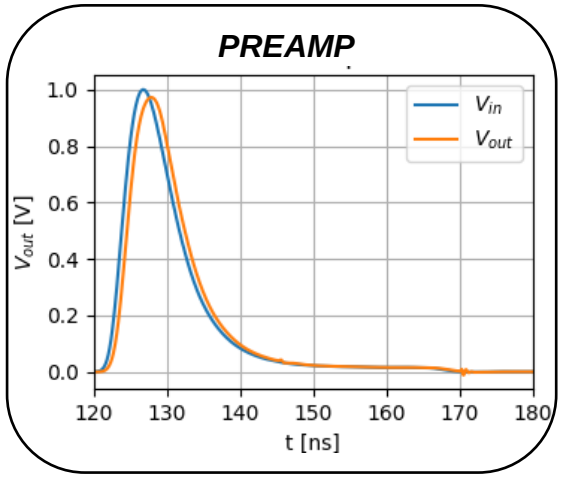
1. Introduction
1.2. Energy ASIC overview

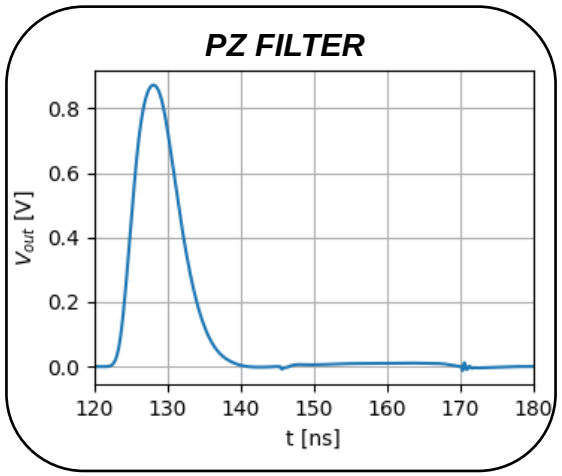
- TSMC 65nm **8-channel ASIC**
- Dynamic range 1 V with **two-gain system and 11-bit resolution** for optimal SNR
  - Noise/1LSB at ~ 500 µV
- **Time-interleaved double channel** scheme for integrator recovery
  - Data transmission at 40 MHz, continuous readout with no deadtime
- **Fully differential** to improve noise rejection.
- **Clocks** individually generated per channel using a **PLL**.
- Power consumption < 50 mW/channel.
- Measure digitized with an **external ADC**. **On-chip ADC is under development** for the second run.



2. Energy ASIC architecture
2.1. Preamplifier and Pole-Zero filter

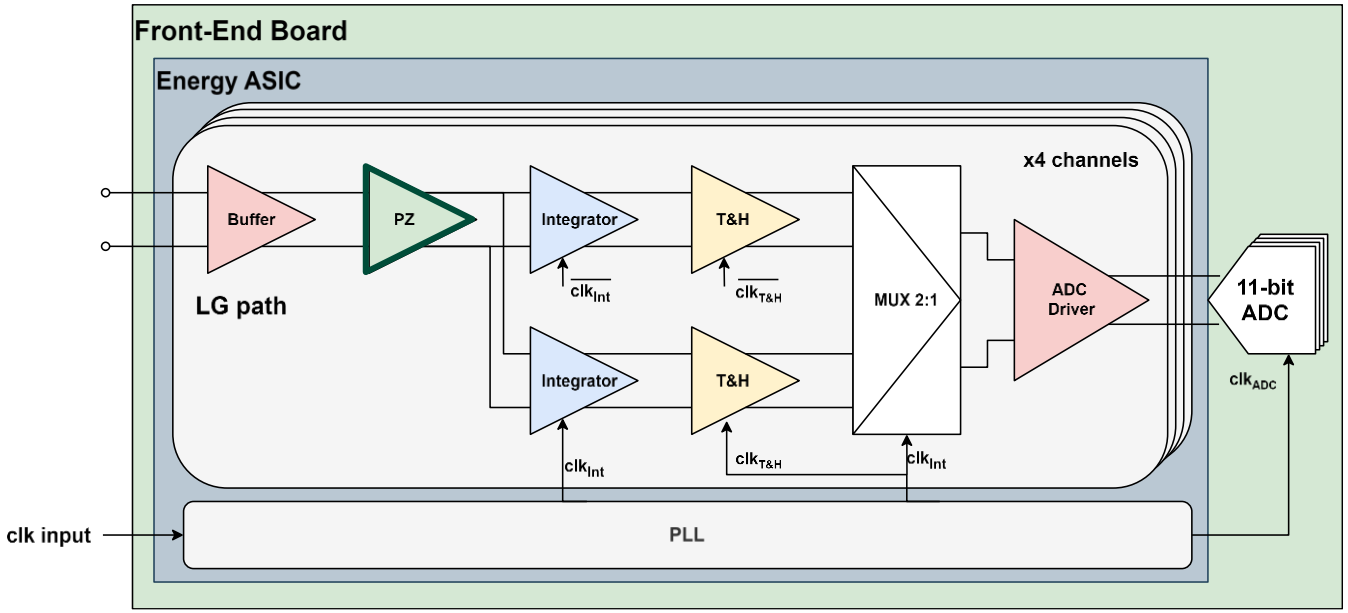


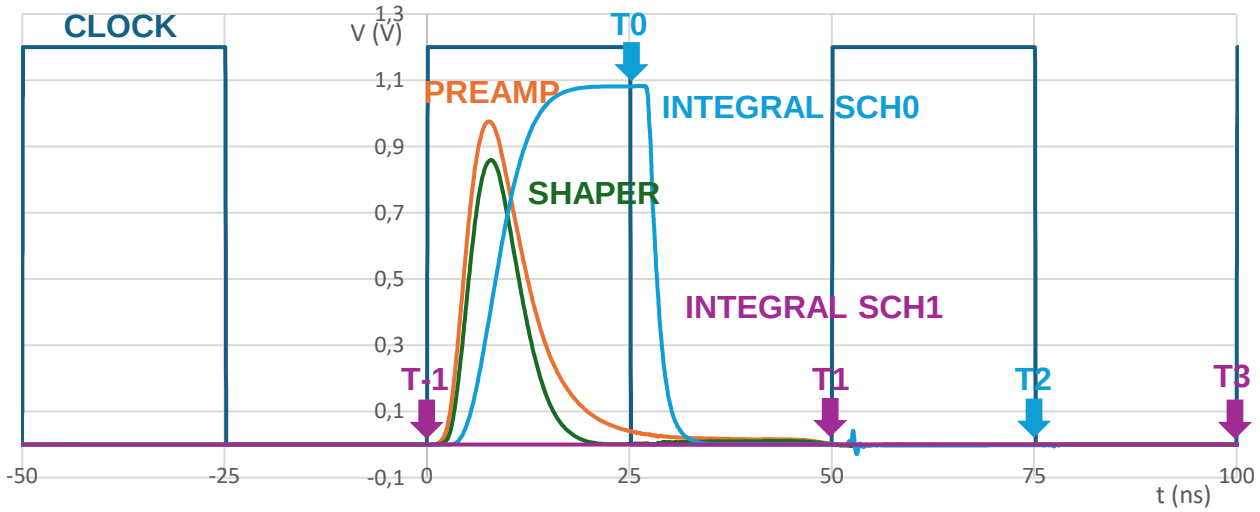




- Input buffer (Preamp)
- Pole-zero filter
  - Shape the input signal to fit it **within the 25 ns** clock window.
  - Input signal with different **shapes** depending on:
    - **Channel technology** (SpaCal, W+Crystal, Pb+poly, Shashlik).
    - PMT
    - Cables
  - Adjustable RC for both pole and zero frequencies to:
    - Adapt the shape against the different technologies
    - Compensate the PVT corners.

2. Energy ASIC architecture
2.1. Preamplifier and Pole-Zero filter



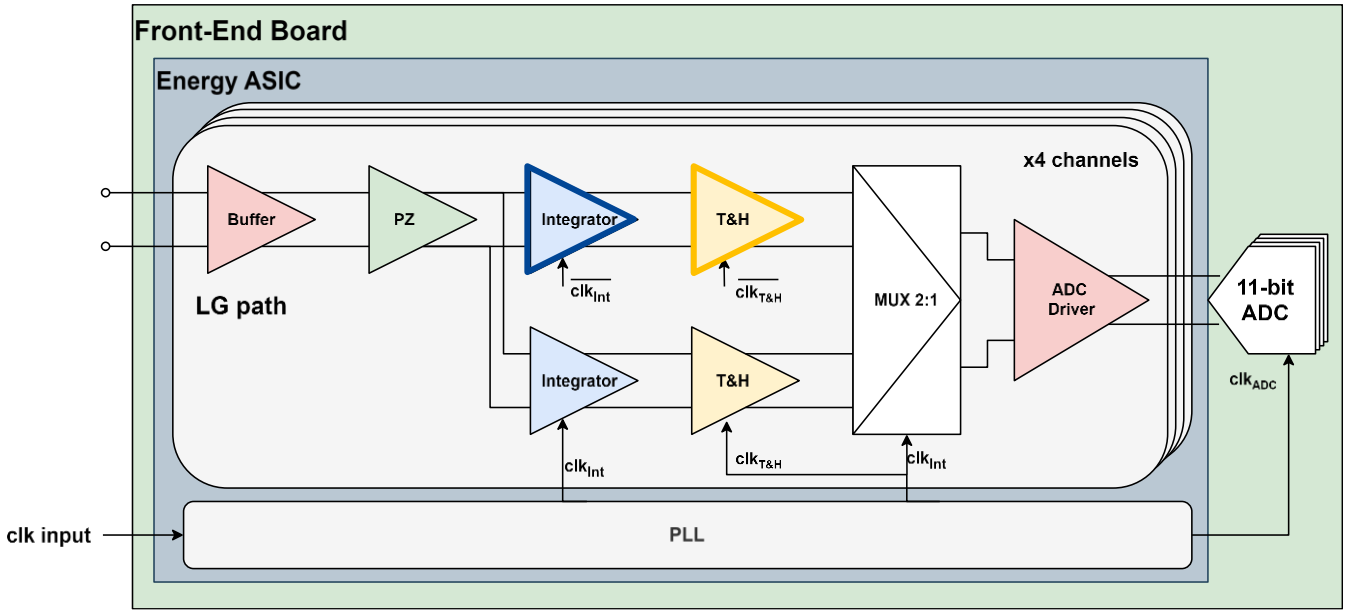


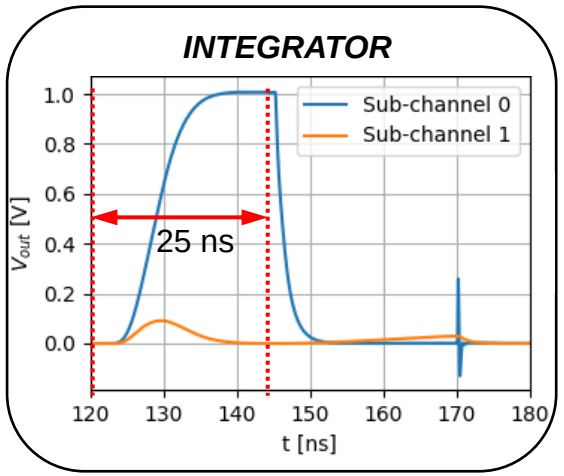
- Specification:
  - **Plateau**: output stable at 1% for > ±2 ns
    - Stability of the integrator output to accept different arrival times
  - **Spill over** ≲ 1%
    - Amount of signal of the present event that appears on the previous/next events.

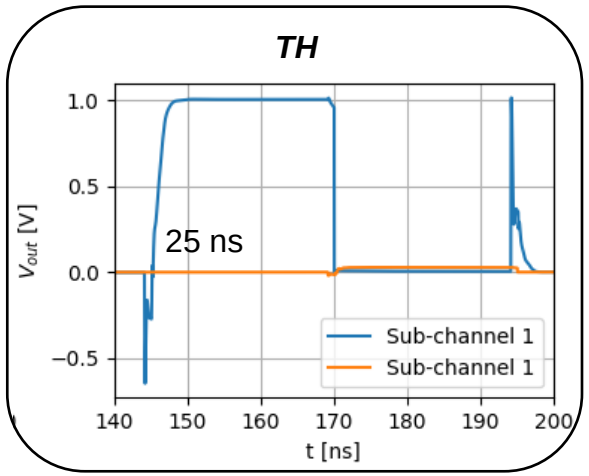
Techno	Plateau (ns)	T-1 (%)	T1 (%)	T2 (%)	T3 (%)	T4 (%)	T5 (%)
WGAGG	3.7	0.93	0.01	0.60	0.61	0.84	0.83
PbPoly	9.3	0.05	0.78	0.31	0.01	0.06	0.14
Shashlik	5.1	0.34	0.19	0.84	0.38	0.32	0.30

TB pulse shapes and nominal case preliminary results

2. Energy ASIC architecture
2.2. Integrator and Track-and-Hold

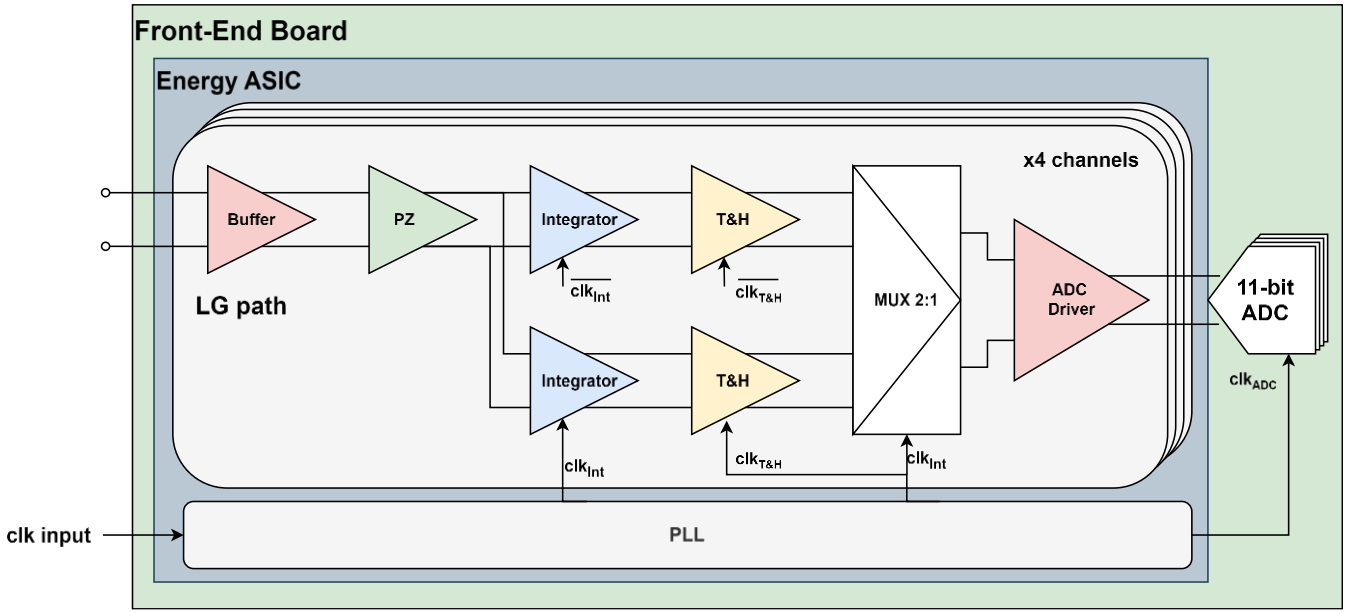


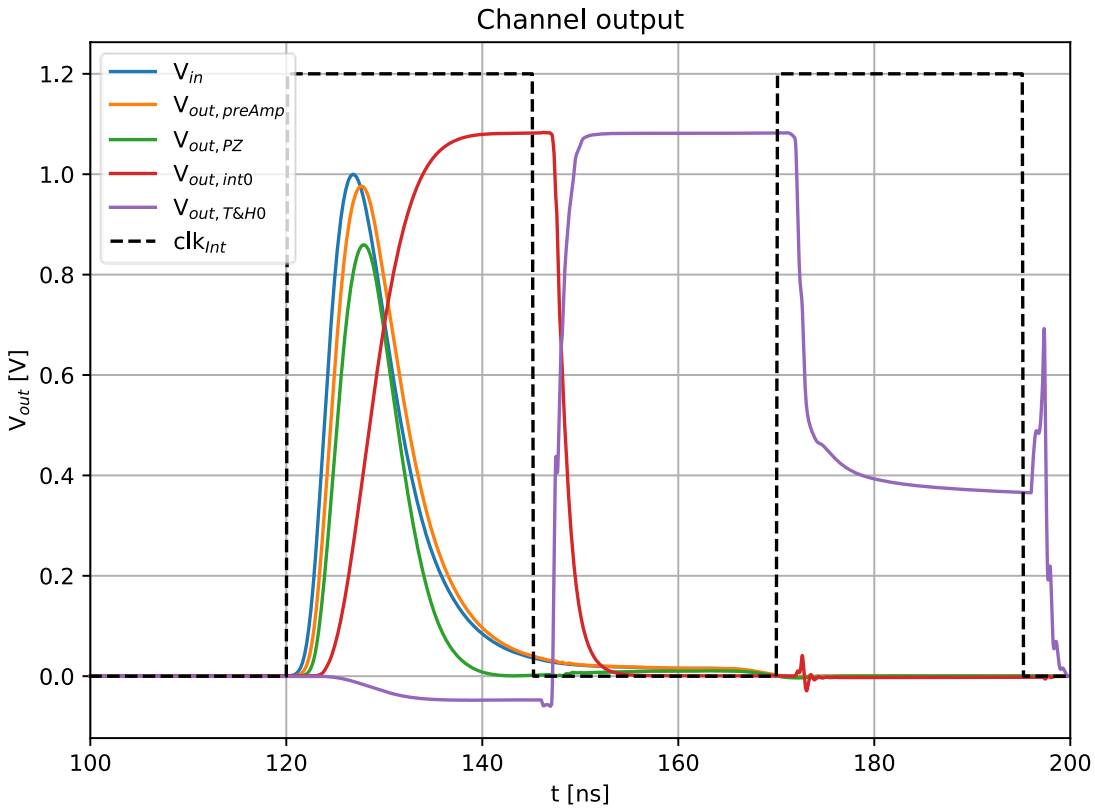




- Integrator
  - **Time-interleaved** integrators → no dead time
  - Variable capacitor for **gain adjustment.**
- Track&Hold
  - Based on bottom plate sampling technique → 3 non-overlapped 20 MHz clocks.
  - Precision for **11 bits**.
  - High slew-rate to hold the measure for > **15 ns**.
- PLL
  - **20 MHz** clocks: integrator + TH + MUX + ADC
  - **Calibrate** the clocks with **< 1 ns** resolution.
- Output buffer
  - Drive capability up to **10 pF** to cope with **IO+pack+ADC parasitics.**

2. Energy ASIC architecture
2.3. Schematic simulations results



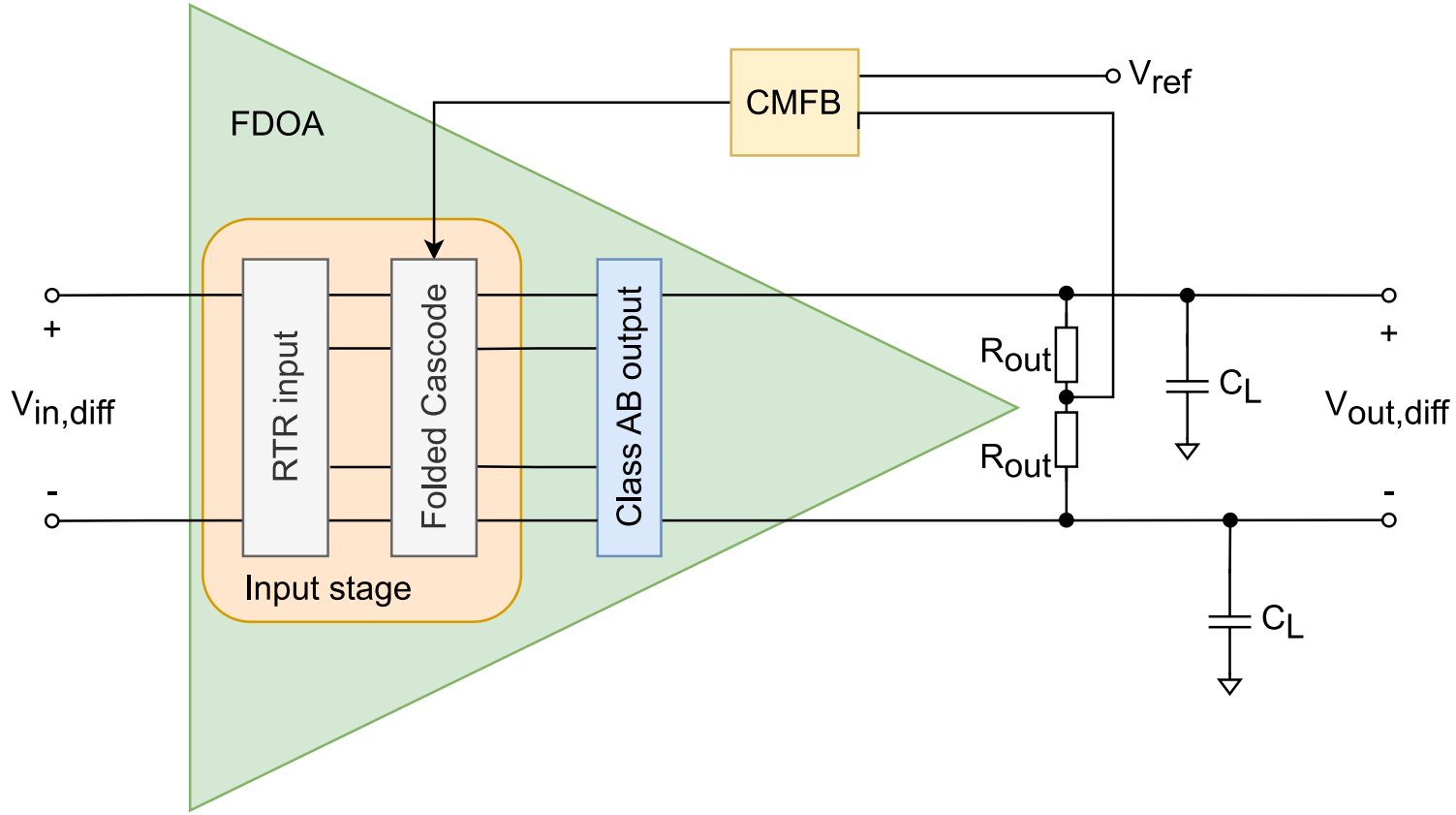


- Schematic simulation results:
  - Preamplifier **integration error < 1%** for $|v_{IN}(t)| = 1$ V
  - Pulse **tail mostly filtered** by shaper.
  - T&H output value **held for > 15 ns**.
  - Transient noise at T&H output **~ 500 µV**. Maximum allowed for **11-bit precision**.
  - **Linearity** error < **1LSB** for $|v_{IN}(t)| < 1.1$V in the LG gain path.

3. Fully-differential operational amplifier (FDOA).
3.1. FDOA specification

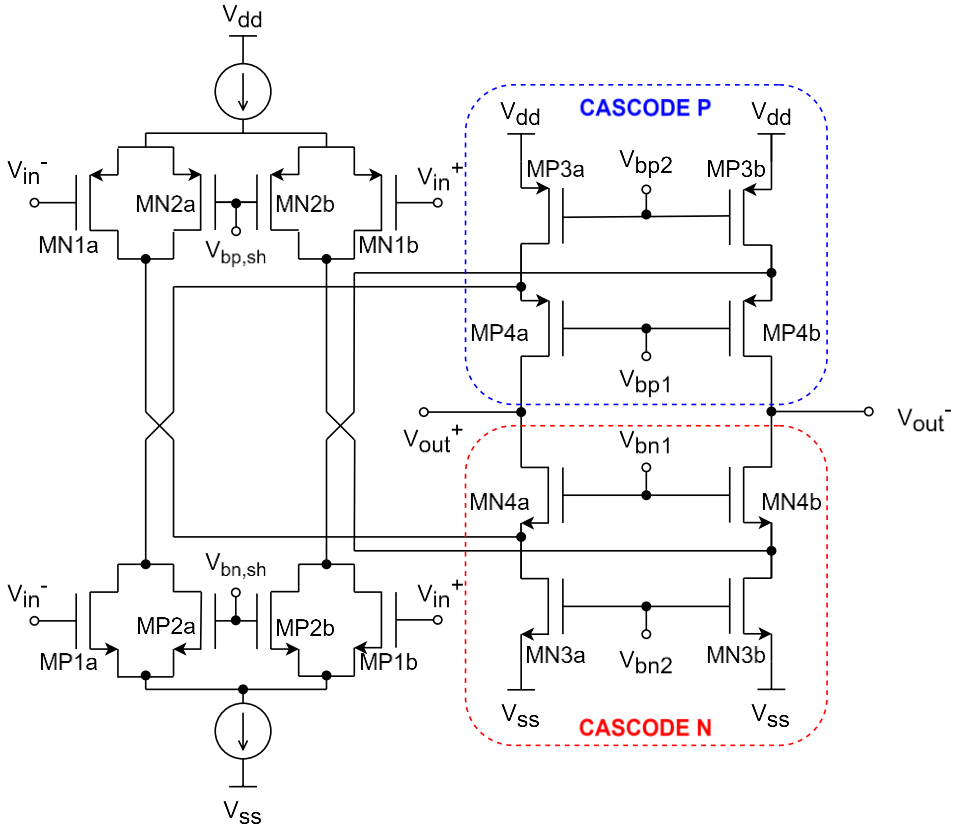
- Development of a rail-to-rail fully differential amplifier in TSMC 65 nm technology.
- The FDOA must achieve the following specifications:

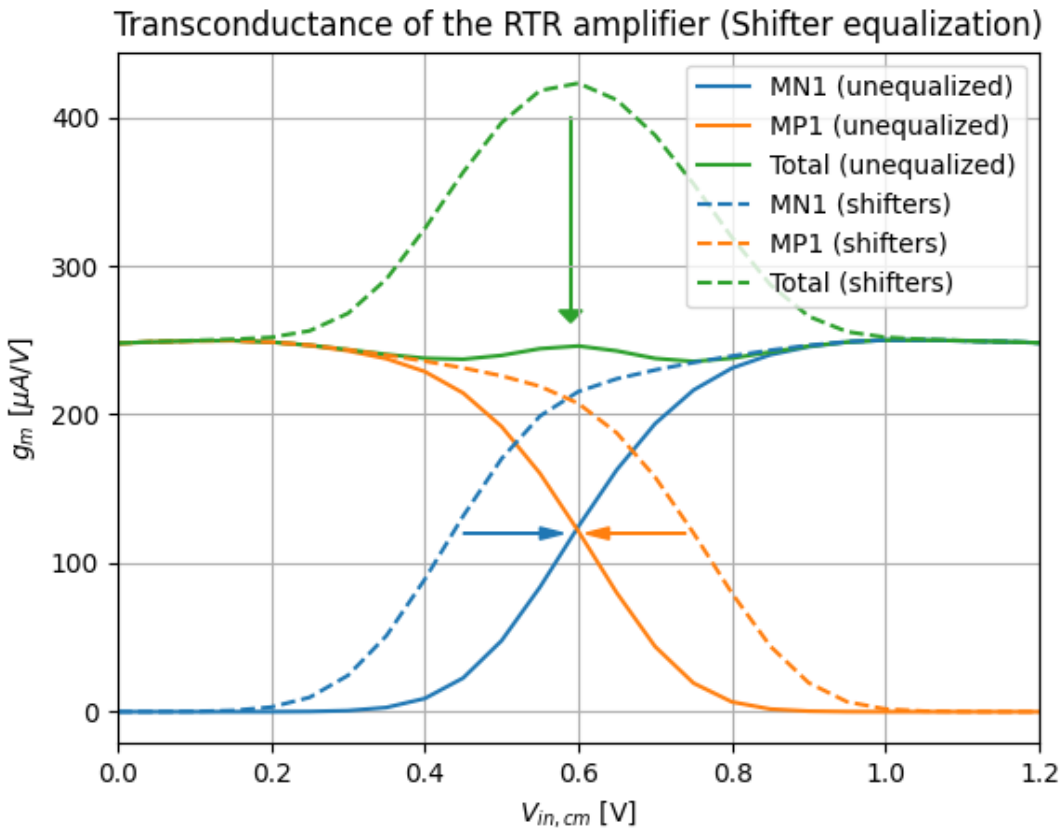
- TSMC 65nm technology
- Fully differential
- Rail-to-Rail (0-1.2 V)
- Low frequency gain > 70 dB
- GBW > 500 MHz
- PM > 65º
- SR > 0.5 V/ns
- VCM ~0.6V
- Power optimization
- Output noise optimization



3. Fully-differential operational amplifier (FDOA).
3.2. Rail-to-rail input stage

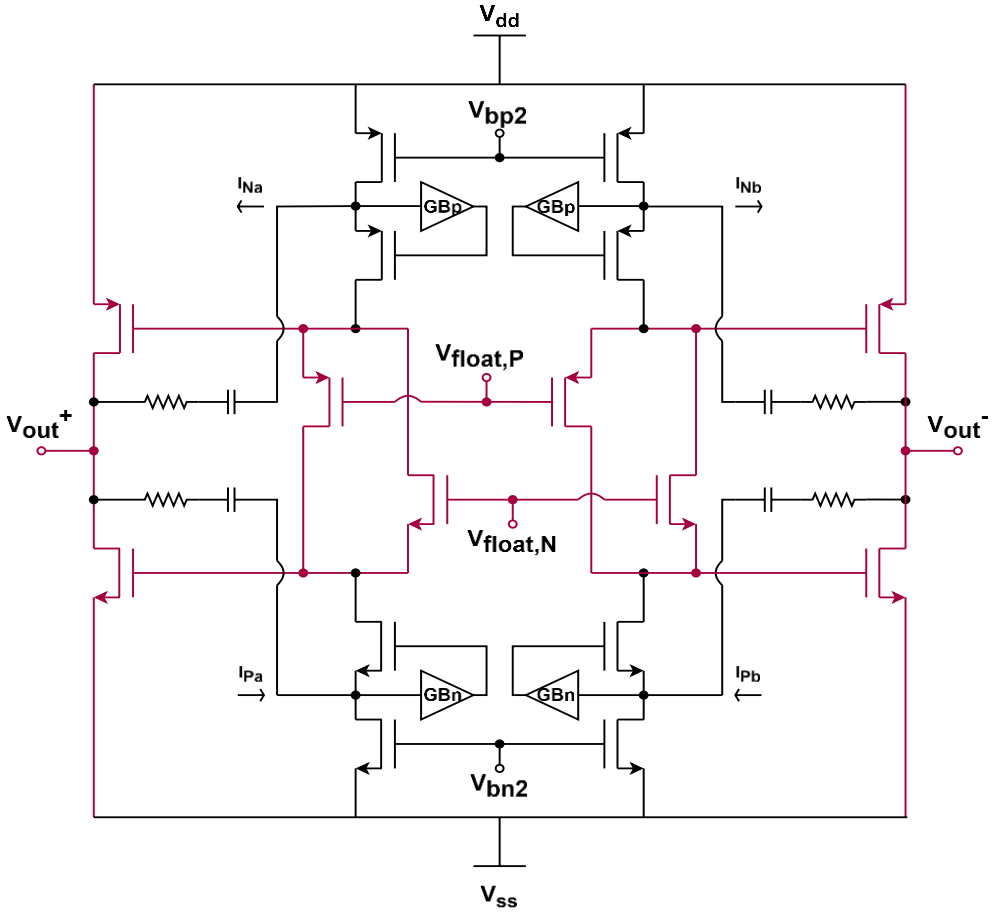
- Rail-to-rail input stage equalized using “shifter” transistors for constant GBW.
  - Need a common bias with 2 current DACs to cope with the PVT corners and 2 voltage DACs to adjust the displacement.
- RTR loaded with cascodes for high gain.

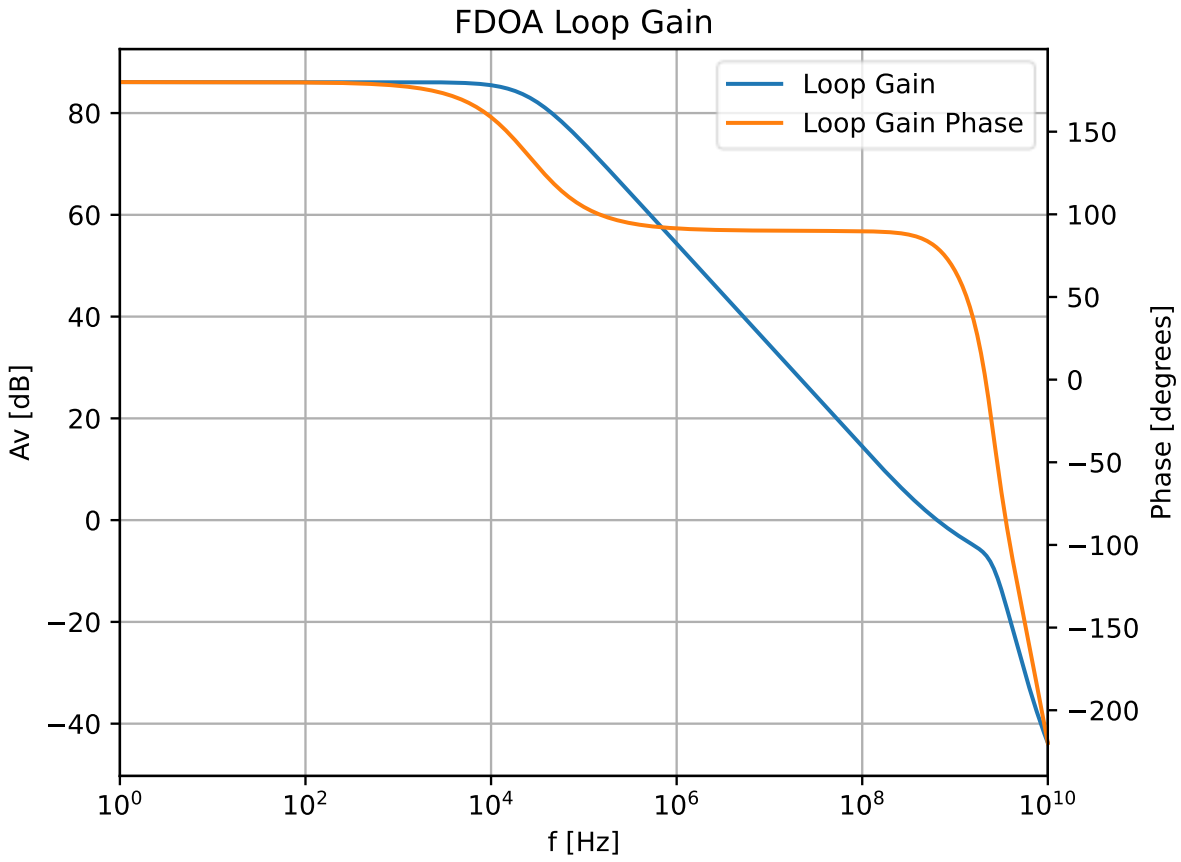




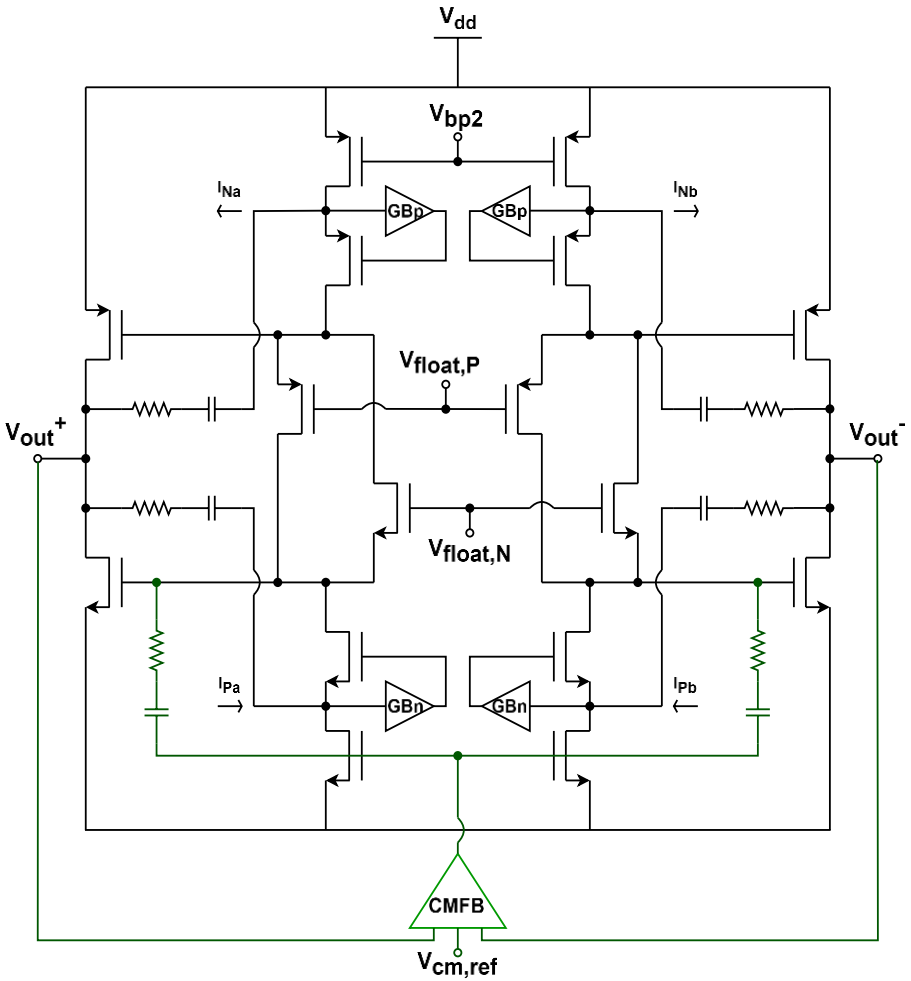
3. Fully-differential operational amplifier (FDOA).
3.3. Class AB output stage

- Class AB output stage for rail-to-rail output swing.
- Floating transistors to generate the voltage drop for biasing the class AB transistors.
- Gain-boosting amplifiers to achieve gain specification.



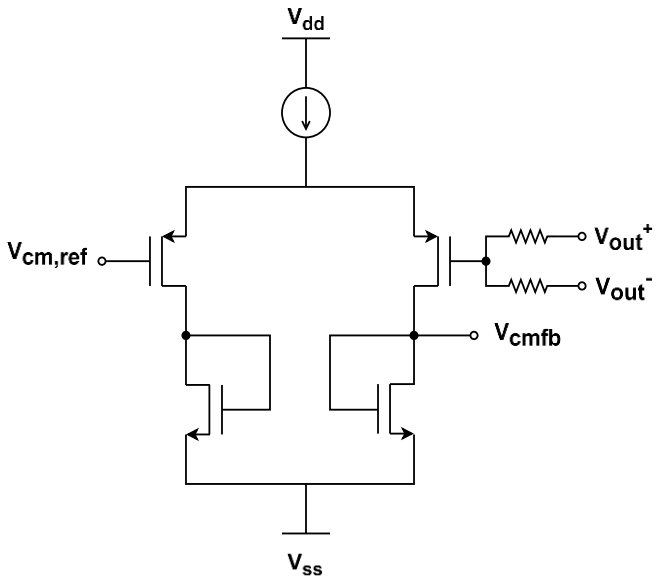


3. Fully-differential operational amplifier (FDOA).
3.4. Common-mode feedback (CMFB)

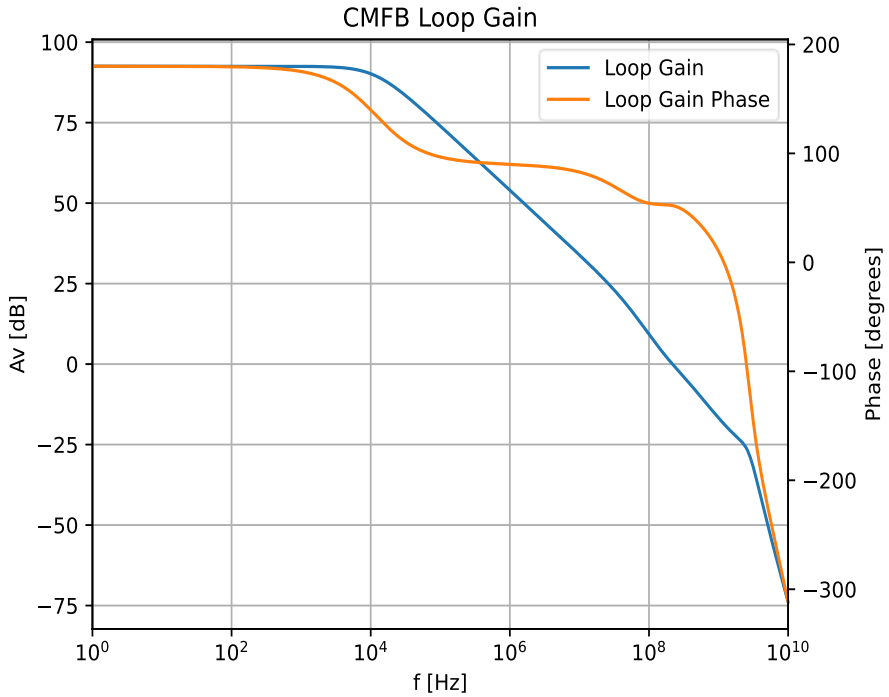


FDOA outputs stage + CMFB

- CMFB to control the DC output level.
  - Common-mode reference set to $V_{DD}/2$ to optimize dynamic range.
- Two-stage feedback generates a 3rd pole.
  - Need to compensate with an additional RC network.

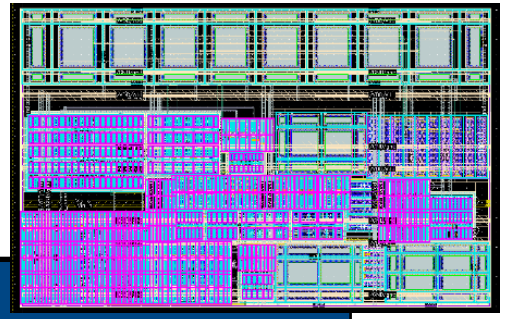


CMFB amplifier



3. Fully-differential operational amplifier (FDOA).
3.5. Simulation results

- PVT corners have been compensated using 2 current DACs to fulfill specifications.
- The DACs range is not wide enough to compensate for the post-layout parasitics of the PVT extreme cases.



Simulation	Schematic			Post-layout		
PVT corner	TT, 1.2Vdd, 27ºC	SS, 1.14Vdd, 80ºC	FF, 1.26Vdd, -20ºC	TT, 1.2Vdd, 27ºC	SS, 1.14Vdd, 80ºC	FF, 1.26Vdd, -20ºC
GBW (MHz)	519.7	511.2	623.9	475.3	412.1	490.2
DC gain (dB)	86.09	84.32	85.17	85.85	84.33	85.27
Phase Margin (º)	79.7	79.01	69.08	71.29	72.52	64.08
Vout + DC (mV)	599.4	600.7	601.8	601.3	599.1	601.5
Vout - DC (mV)	599.4	600.7	601.8	601.3	599.1	601.5
SR+ (V/µs)	583.4	860.3	657.4	654.9	917.4	657.4
SR- (V/µs)	-581.4	-861.6	-648.7	-650	-918.2	-648.7
I (mA)	1.94	2.448	1.875	2.16	2.361	1.772
Power (mW)	2.32	2.939	2.25	2.592	2.834	2.127

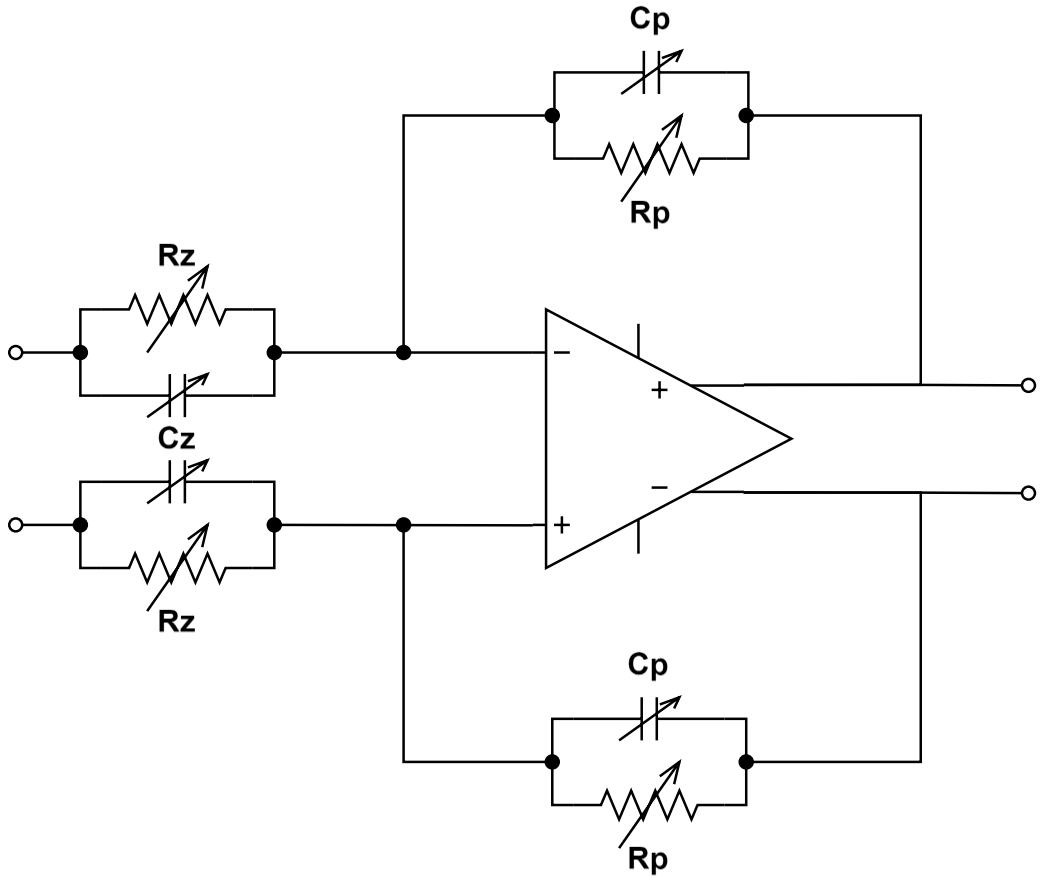
4. Summary

- Upgrade II ASIC developed in TSMC 65 nm technology based on proved U-I design.
  - Time-interleaved double channel guarantees the continuous readout.
  - Add a second gain path to cover the 12-bit resolution due to the reduced voltage supply.
  - The design of the fully-differential amplifier and the performance of the processing chain satisfies all channel requirements.
- FDOA layout finished
  - Postlayout simulations are promising even though current DACs need to be adjusted.
  - Dimensions fit the complete channel specification.
  - Layout of analog blocks ongoing.
- Next steps:
  - Complete the analog channel layout.
  - Integration of the analog chain with PLL and I2C block.

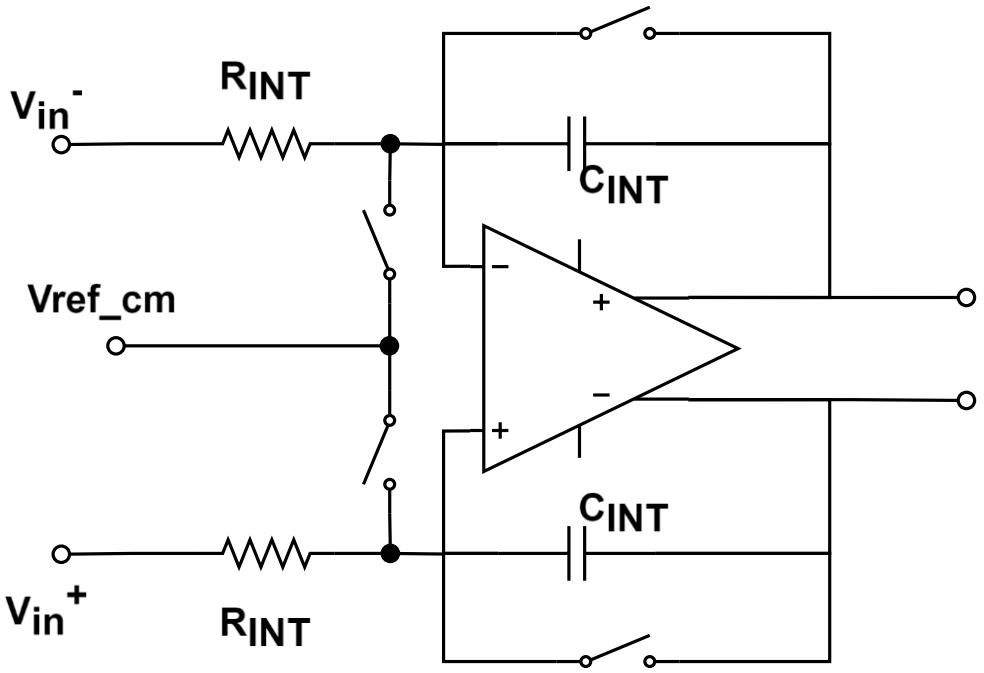
Thanks for your attention

Grant M2RN002806 MIN/ PID2022-139842NB-C21 funded by MICIU/AEI/ 10.13039/501100011033, as appropriate, by the “European Union NextGenerationEU/PRTR” and by Generalitat de Catalunya.

Back-up
Pole-zero filter and integrator schematics



Pole-zero filter schematic



Integrator schematic

Back-up
Track-and-Hold phases

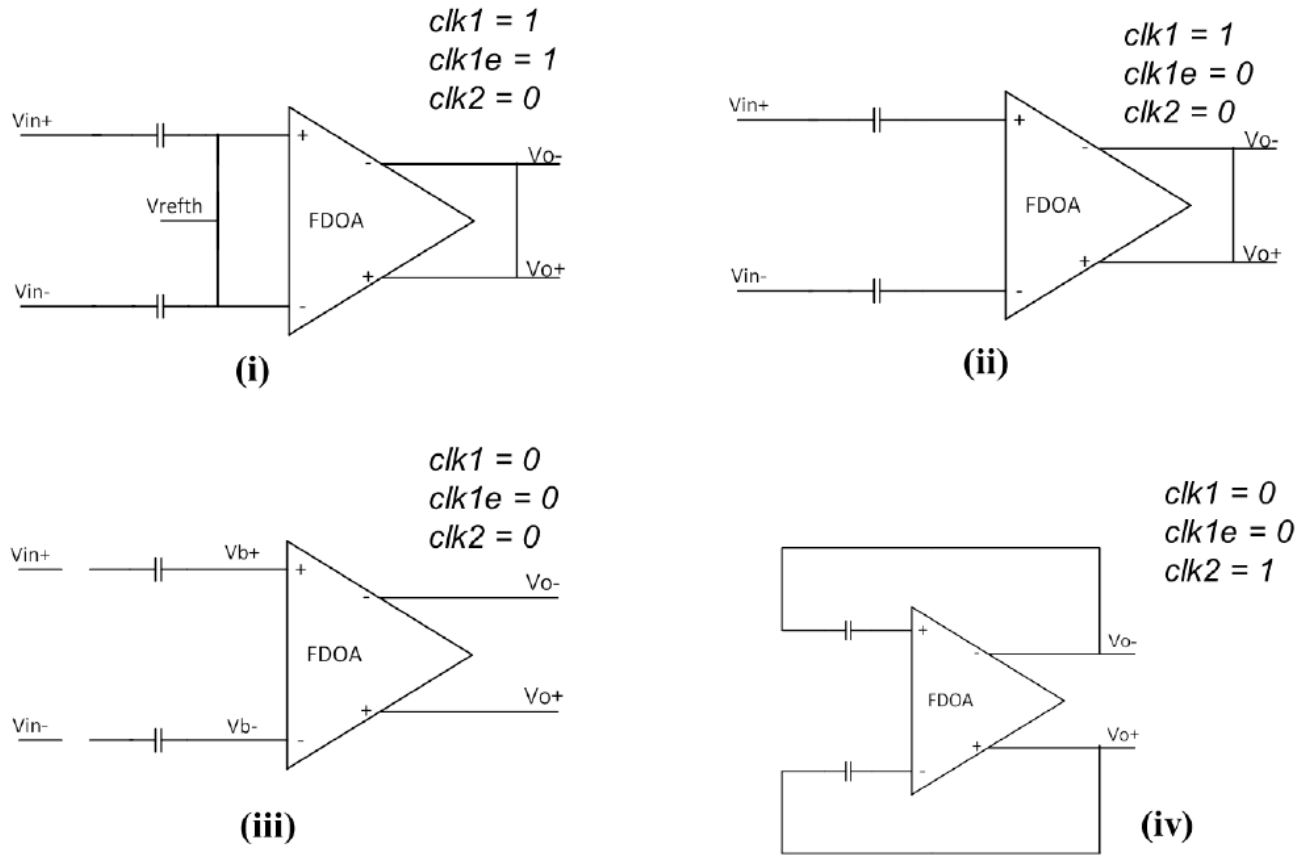
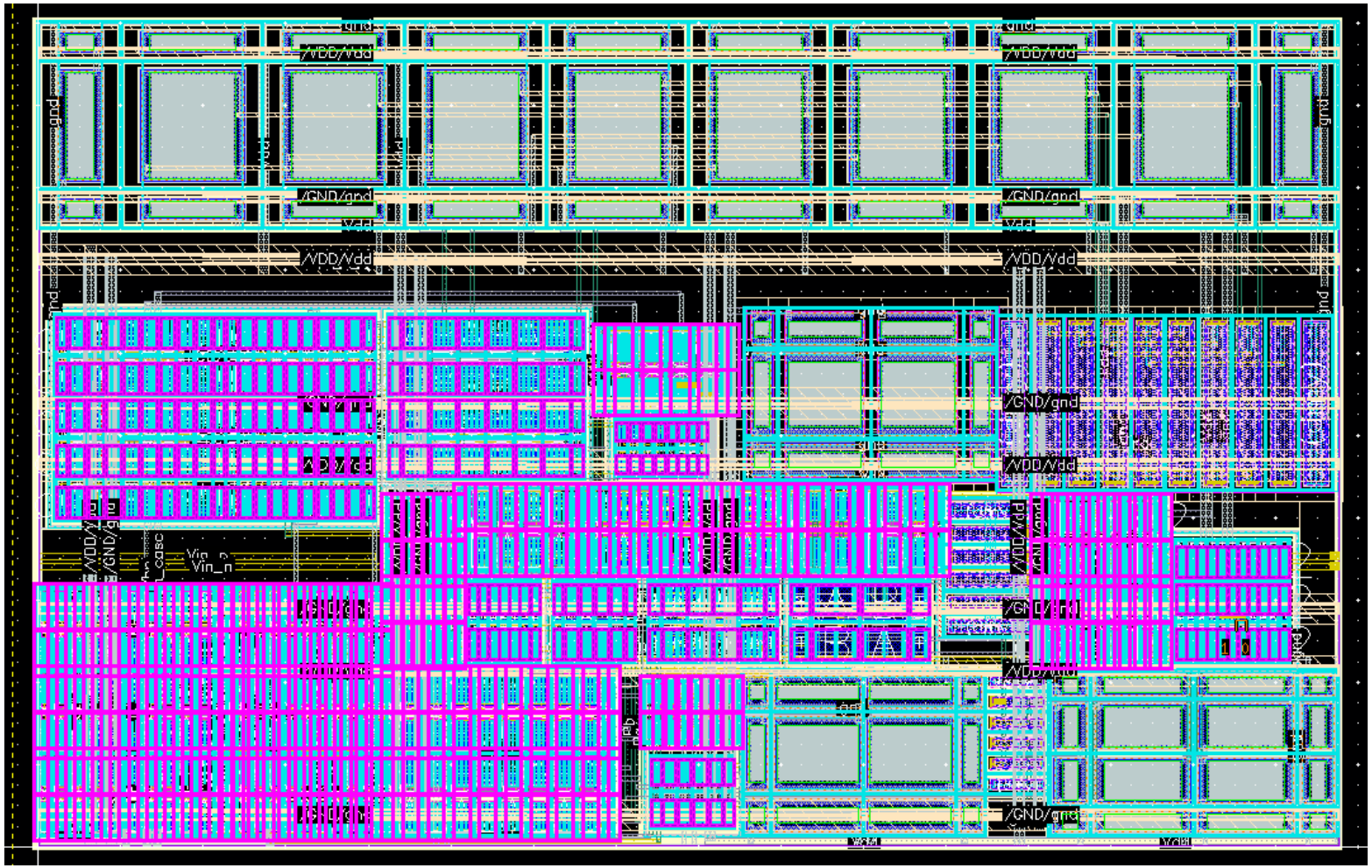


Figure 3.37 – Track-and-Hold phases.

Back-up
FDOA Layout

FDOA LAYOUT (80 x 126 um)



Back-up
FDOA for the ADC driver. Simulation results

- GBW > 300 MHz is enough to ensure the measure is held for the time required by the ADC.
- Still needs adjustment to guarantee stability for C_L = 10 pF.

	Schematic TT					
C_L	5 pF	6 pF	7 pF	8 pF	9 pF	10 pF
GBW (MHz)	320.5	320.5	320.4	320.4	320.4	320.4
DC gain (dB)	81.81	81.81	81.81	81.81	81.81	81.81
Phase Margin (º)	72.59	69.58	66.67	63.91	61.33	58.96
Vout + DC (mV)	599.7	599.7	599.7	599.7	599.7	599.7
Vout - DC (mV)	599.7	599.7	599.7	599.7	599.7	599.7
SR+ (V/µs)	374.7	374.7	373.5	371.8	369.9	368
SR- (V/µs)	-374.8	-374.7	-373.6	-371.8	-369.9	-367.9
I (mA)	4.032	4.032	4.032	4.032	4.032	4.032
Power (mW)	4.838	4.838	4.838	4.838	4.838	4.838