

TWEPP 2024 - October 1st, 2024

Design update and characterization of sub-10ps TDC ASIC in 28nm for future 4D trackers

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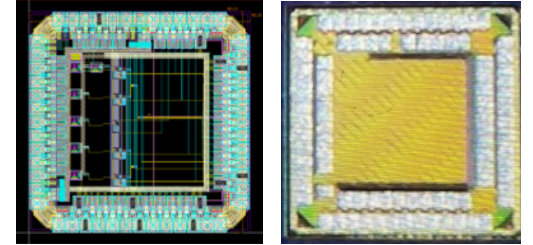
Aldo Pena Perez (SLAC), Angelo Dragone (SLAC), Ariel G. Schwartzman (SLAC),
Bojan Markovic (SLAC), Caterina Vernieri (SLAC), Dong Su (SLAC), Larry Ruckman (SLAC), Lorenzo Rota
(SLAC), Valentina Cairo (CERN)

Status

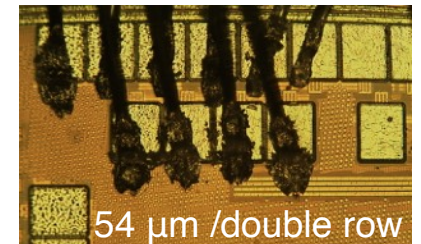
Design of a sub-10ps TDC ASIC

- Novel 2D Vernier ring-oscillator TDC with embedded sliding-scale technique
 - 28nm technology
 - Necessary to enable 4D operation in tracker
 - Improves conversion linearity
- A first 4-channel prototype ASIC produced in 2023
 - The 1mm² area had the bounding-PAD pitch too aggressive for successful assembly.
 - Design, test setup and challenges presented at [TWEPP 2023](#).
 - Design and characterization of sub-10ps TDC ASIC in 28nm CMOS technology for future 4D trackers (Larry Lou Jr Ruckman)
- Second prototype produced in 2024
 - 2mm² area,
 - PAD pitch of 72 μm : single row
- Test setup and characterization results are presented hereafter.

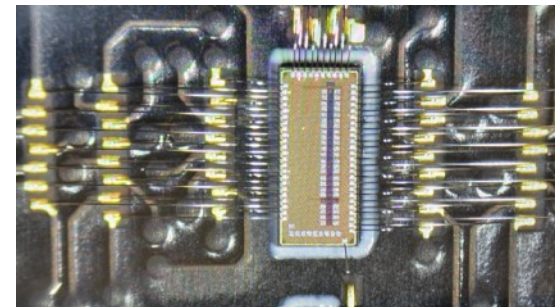
v1 (submitted Jan. 2023):



wire-bonding issues:



v2 (submitted Jan. 2024):



28nm TDC Architecture

- **2D Vernier Architecture:**

- Fast Ring Oscillator with 50ps propagation delay cells;
- Slow Ring Oscillator with 56.25ps propagation delay cells;

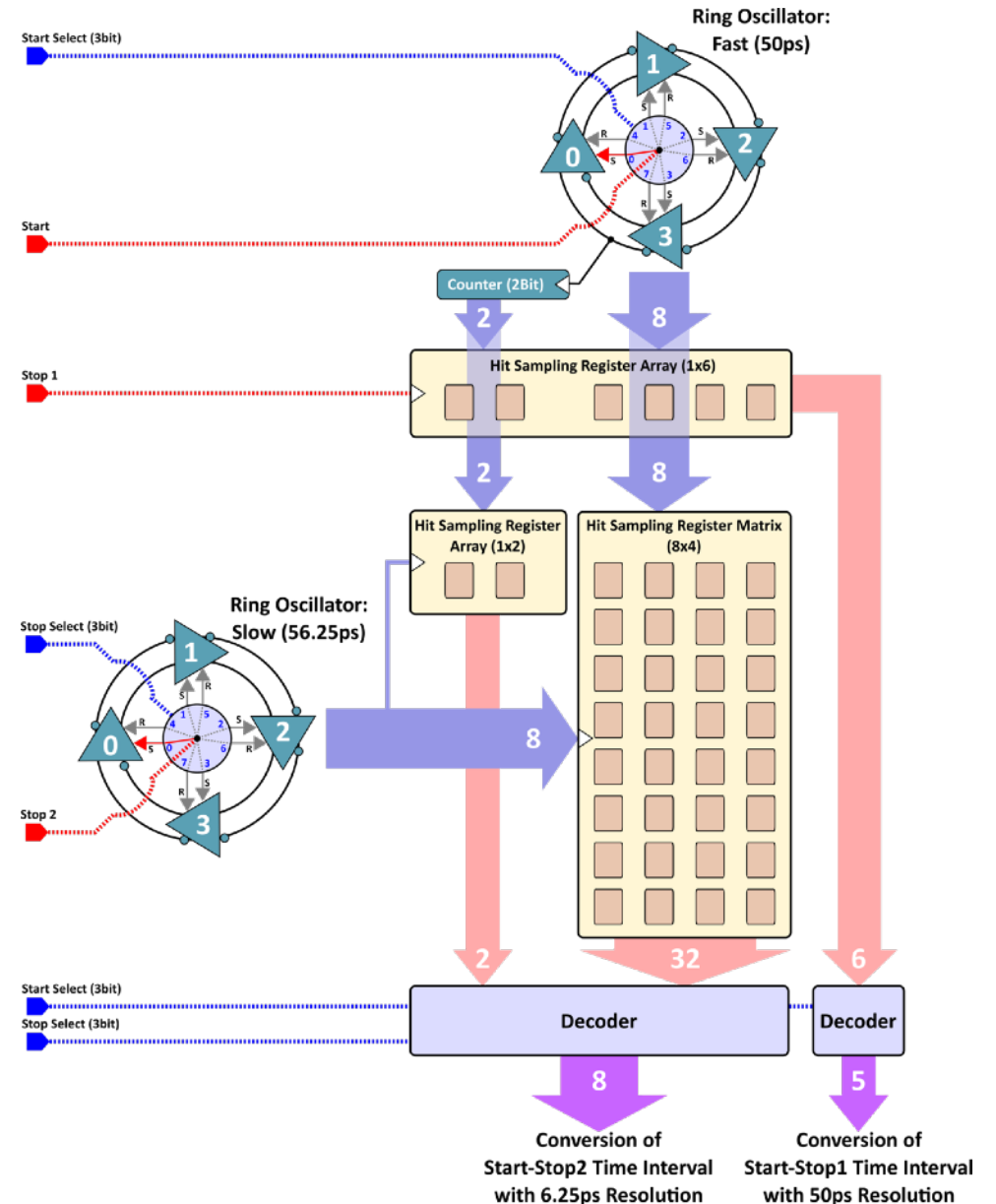
- START + two STOP signal for simultaneous time-of-arrival (TOA) and time-over-threshold (TOT) measurements;

- Start-Stop1 - Coarse time resolution (TOT): 50ps;

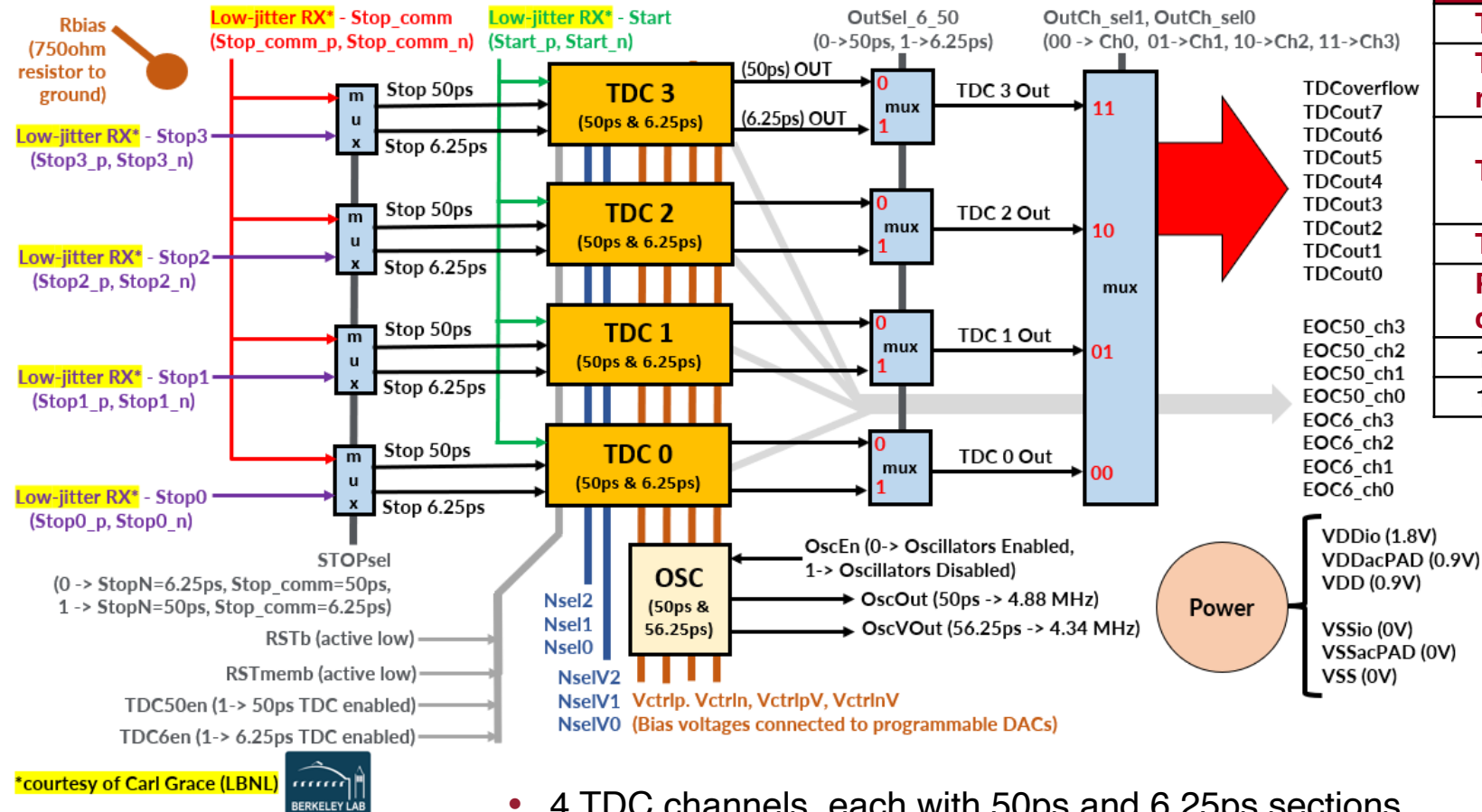
- Start-Stop2 - Fine time resolution (TOA): $56.25\text{ps} - 50\text{ps} = 6.25\text{ps}$;

- **Sliding scale technique for improvement of conversion linearity:**

- Both ring oscillators have programmable starting conditions via delay cell set/reset function;
- Starting conditions randomly selected each measurement cycle and corresponding values subtracted from the conversion result;
- Same time intervals converted with different parts/bins of the TDC conversion characteristics;
- Sliding scale transforms the non-linearities into stochastic variable thus effectively improving the conversion linearity at the expense of worsening single-shoot precision.



4-channel TDC prototype ASIC (Recap)



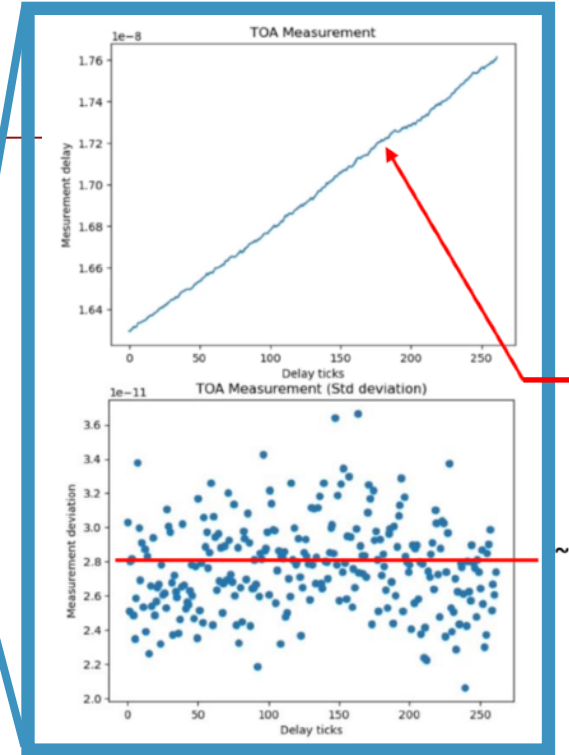
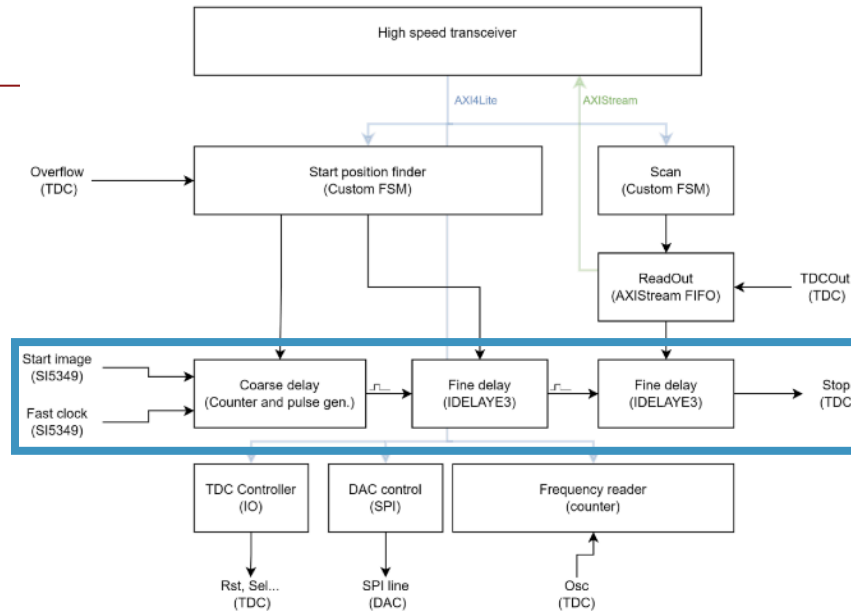
| | TDC metrics |
|--------------------------|--|
| Technology | 28nm |
| Timing resolution | 6.25ps (TOA) / 50ps (TOT) |
| Time depth | 1.6ns (8bit / 5bit) easily extendable by simple addition of bits to the counter |
| TDC area | 19 μ m x 44 μ m |
| Power consumption | (average, 25ns conversion cycle / bunch crossing) |
| 10% occupancy | 16 μ W |
| 1% occupancy | 2.5 μ W |

- 4 TDC channels, each with 50ps and 6.25ps sections
- Common Start, a common Stop1 and 4 separated Stop2 inputs
- Low-jitter receivers provided by LBNL
- Fast and Slow Oscillators for propagation delay control

Test Setup

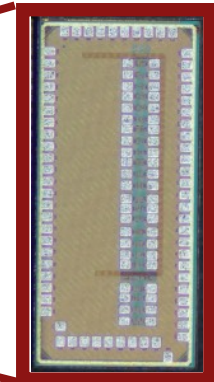
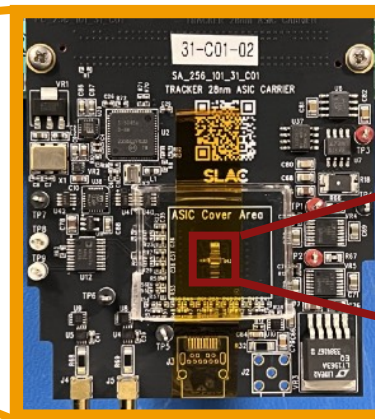
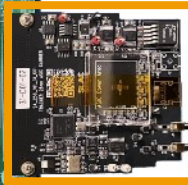
First test setup design

- FMC card featuring the 28nm TDC
 - Connected to KCU105 dev. board
 - **Start signal from SI5349 PLL**
 - **Stop signal from FPGA delay**
- Controlled via PGP4 link @10Gbps



IDELAY3's non-linearity

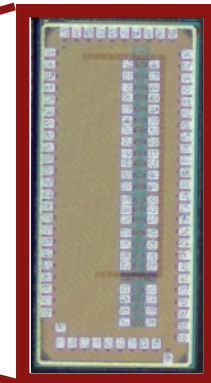
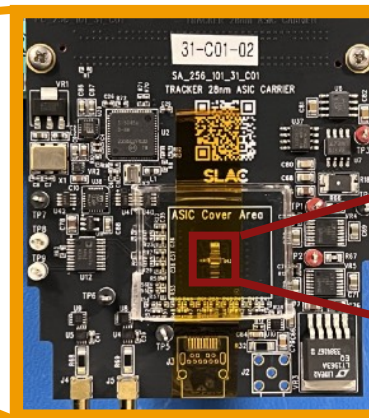
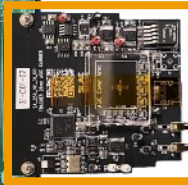
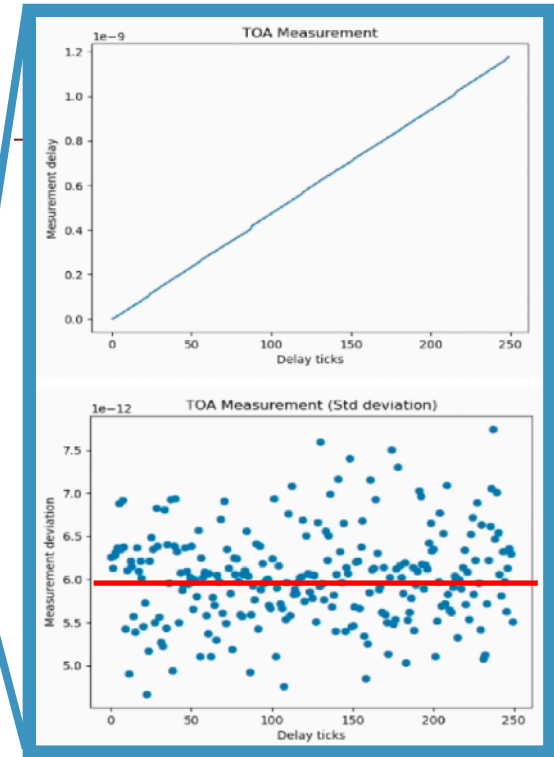
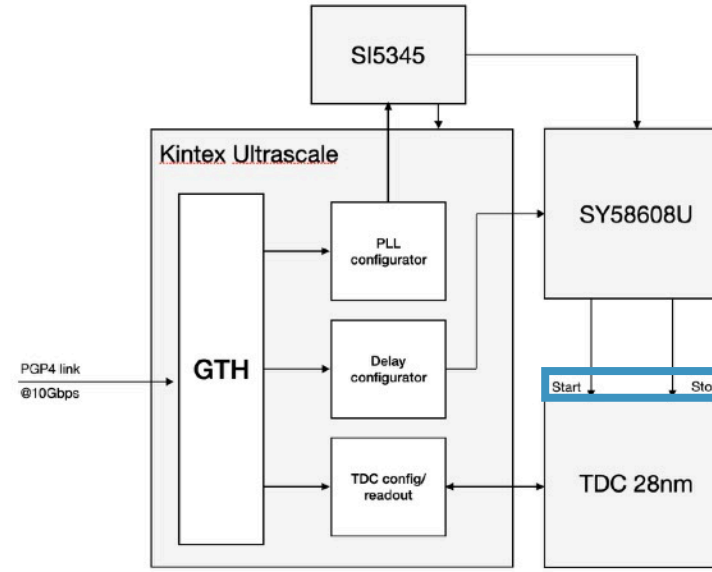
~28ps



Test Setup

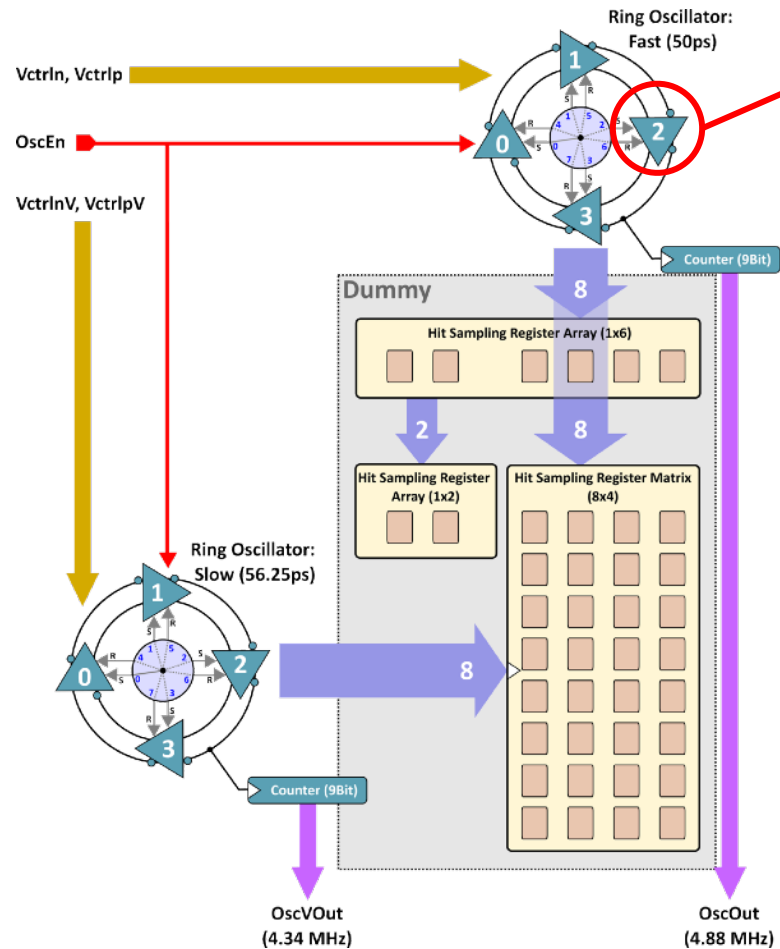
Redesign of the test setup

- FMC card featuring the 28nm TDC
 - Connected to KCU105 dev. board
 - **External programmable delay (SY58608U)**
 - 5ps resolution, 2.56ns range
 - Start/Stop signal from a PLL
- Controlled via PGP4 link @10Gbps

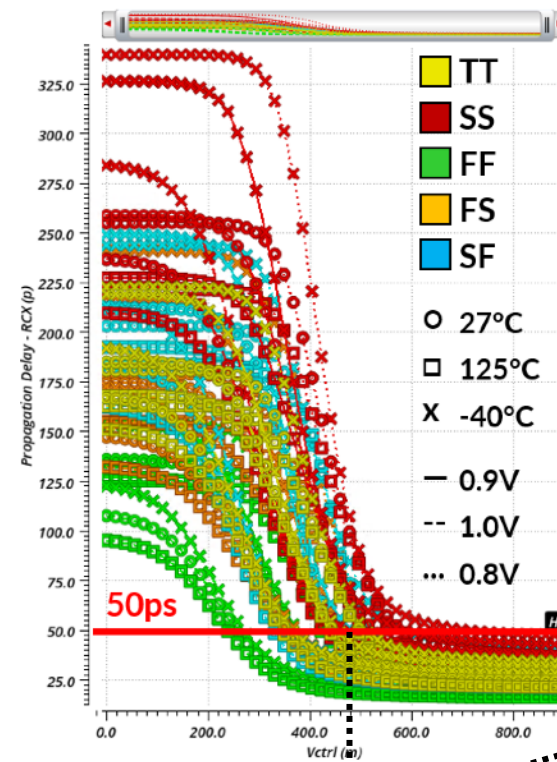


Delay Cell Propagation Delay Setup

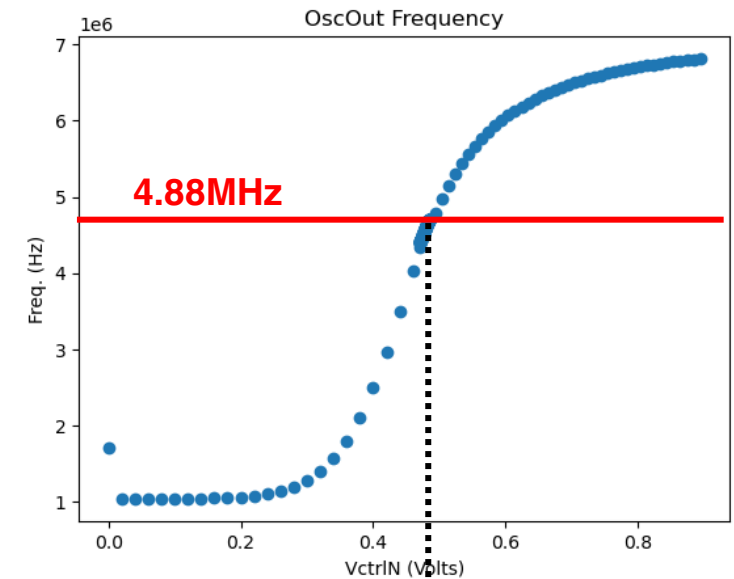
- Eventually, in future implementations, the Delay Cell propagation delay will be stabilized against PVT variation by an on-ASIC Delay-Locked Loops (DLLs). In the prototype ASIC, the control voltages (Vctrl) are set by the external DACs on the ASIC carrier board and controlled via software.



Cell Propagation Delay VS Vctrl
– Simulation (RCX):



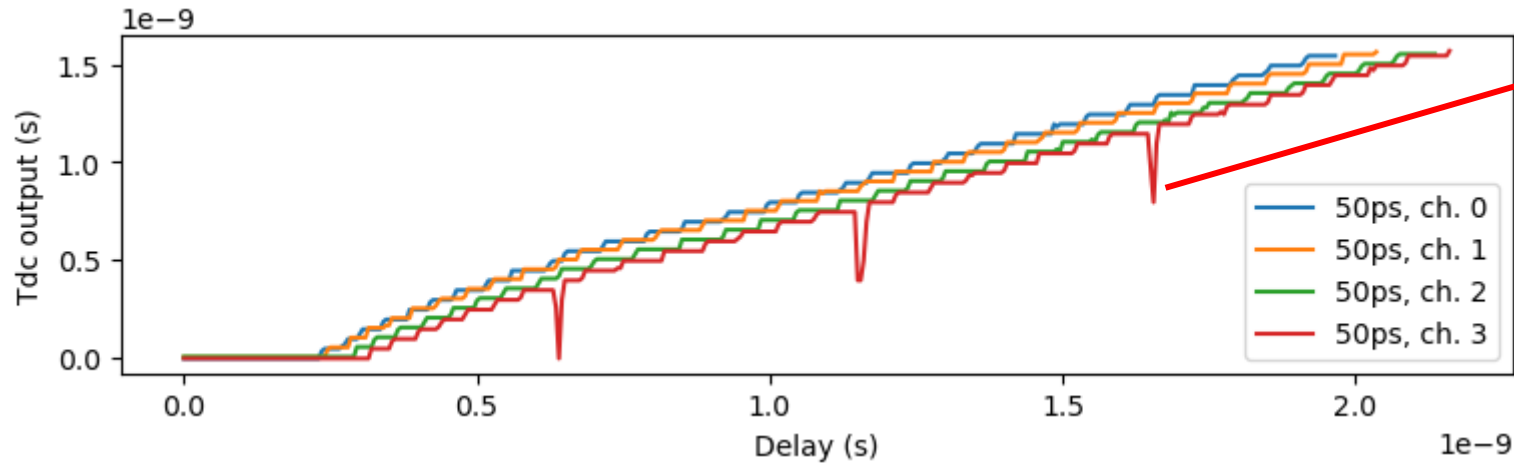
OscOut frequency VS Vctrl
scan (measurement):



Measurement matches well the
simulation results (TT)

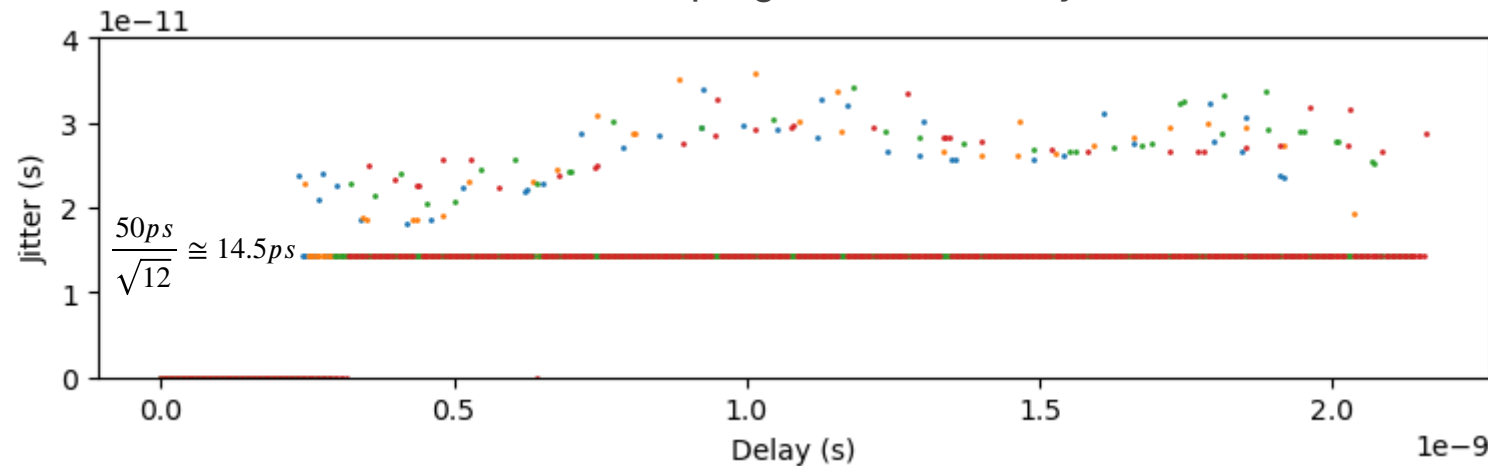
50ps (TOT) Measurements

TDC Output VS programmable delay:



Some channels show “glitches” in the conversion characteristics that are sensitive to supply voltage, temperature and Vctrl settings. The issue was traced to a race condition in the counter sampling logic due to parasitic introduced on the ASIC top level routing (outside the TDC itself). **Fixed in the next ASIC employing the TDC.**

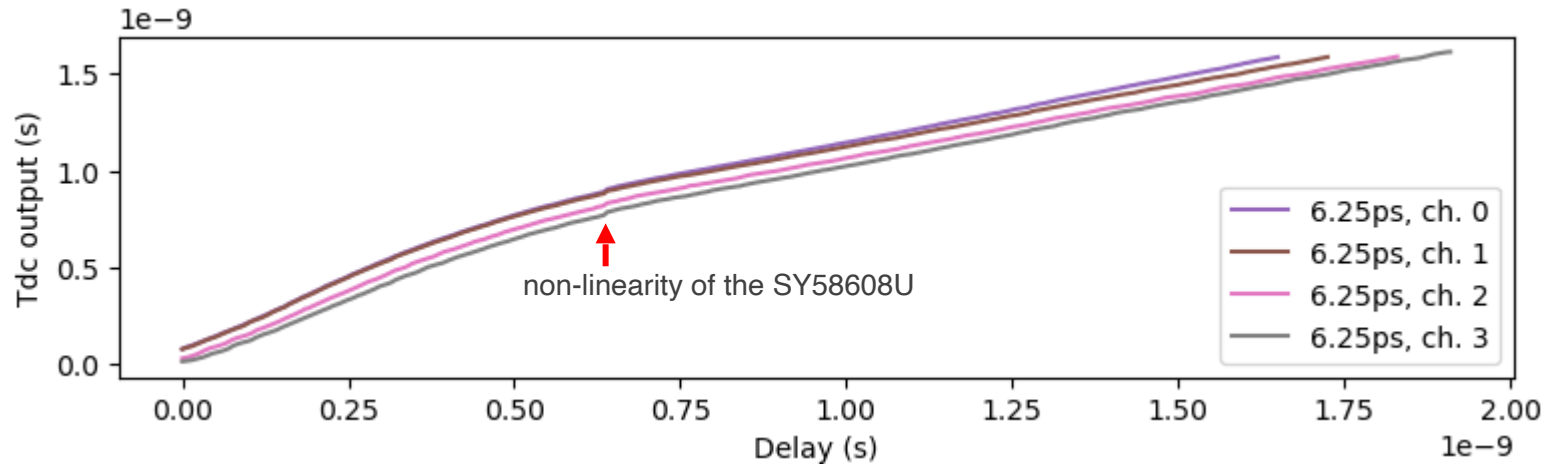
Jitter VS programmable delay:



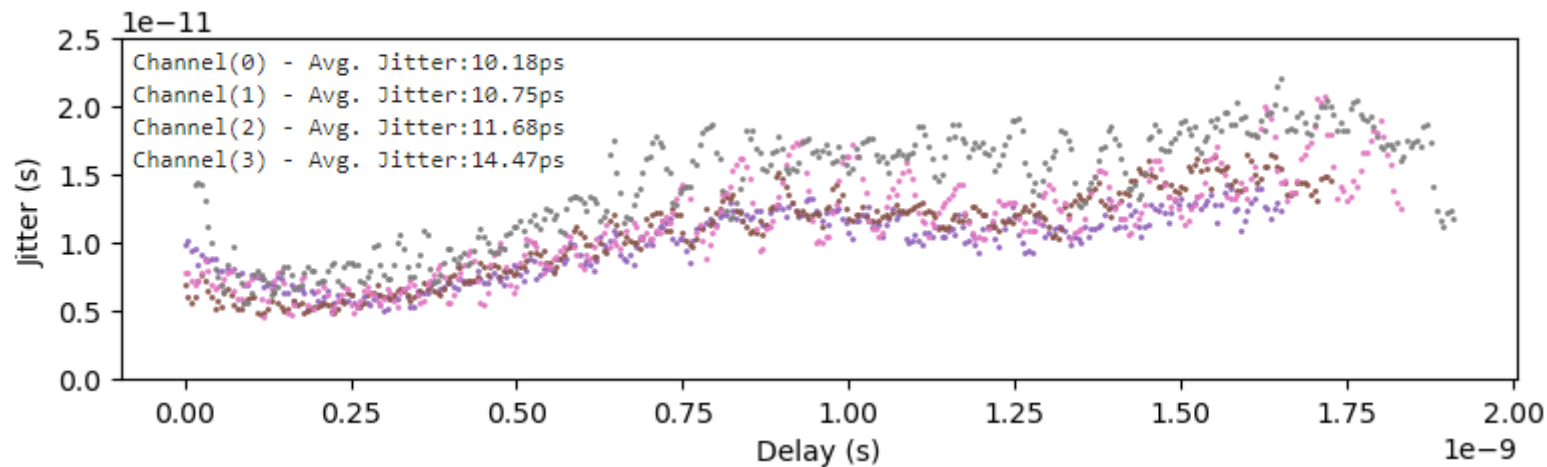
Jitter for 50ps measurements is dominated by the quantization error

6.25ps (TOA) Measurements

TDC Output VS programmable delay:



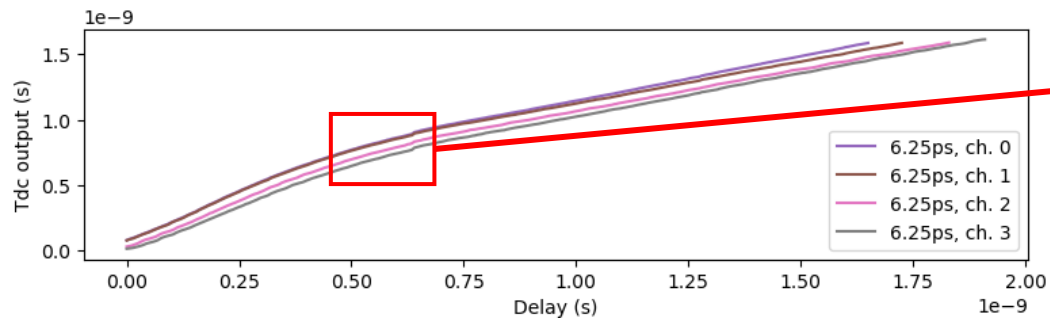
Jitter VS programmable delay:



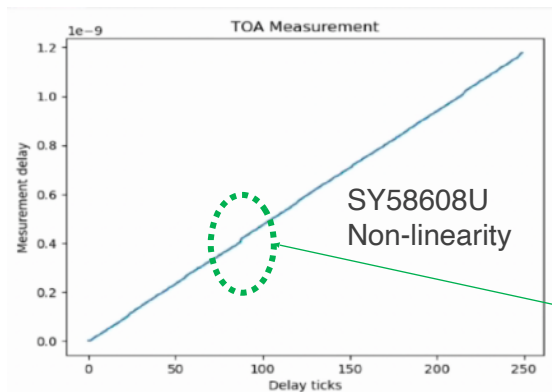
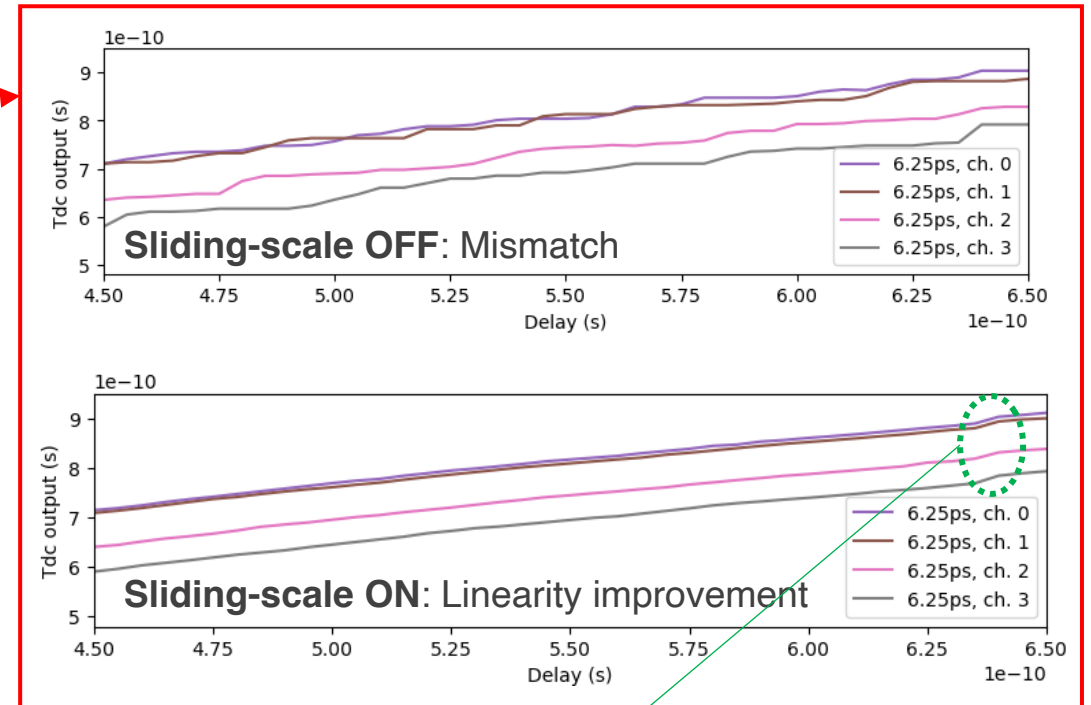
- The channels receive the same Start-Stop signals but due to in-ASIC routing, the Start signal arrives first to ch0 and ch1 followed by ch2 and ch3
- The curvature of the characteristics is due to absence of in-ASIC capacitors on the critical Vctrl lines (driven by external DACs) causing the TDC resolution to change as they operate.
- Jitter worsened by the disturbances on the un-filtered Vctrl lines
- In-ASIC capacitors added to Vctrl lines in the next ASIC employing the TDC (see Bojan's talk "**Design of 28nm readout ASIC prototype for 3D-integrated LGAD sensors**" in the afternoon session)

Sliding-Scale Linearity Improvement

- Achieving sub-10ps resolution in all PVT conditions requires Vernier architecture (LSB given by the difference of propagation delays) that suffers heavily from mismatch (especially true for implementations that target small pixel sizes) resulting in significant non-linearities of the TDC characteristics.
- The developed TDC implement the sliding-scale technique [1,2] for linearity improvement to mitigate the weakness of the Vernier approach.



zoom



[1] C. Cottini, E. Gatti, and V. Svelto, "A new method for analog to digital conversion," Nucl. Instr. Meth., vol. 24, p. 241, Aug. 1963.

[2] E. Gatti, P. F. Manfredi, and D. Marino, "Analysis and characterization of cyclic-scale compensated analog-to-digital converters," Nucl. Instrum. Methods, vol. 165, no. 2, pp. 225-230, Oct. 1979.

Summary

Pico-second TDC is a central feature in all future detectors

- 4 dimensional trackers and calorimeter improvement by BIB reduction
- Requires sub-10ps resolution

28nm TDC prototype produced

- 1st TDC version designed in 2023 had wire-bonding issues
- Redesigned in 2024 to increase the chip area and remove 2 layer pads
- First 28nm TDC received in June 2024

Test setup redesigned and validated

- Test setup was re-designed due to bad jitter performance
- Stop signal generation through external programmable delay
- Same start/stop source, only delay in between (relative jitter went below 6.25ps)

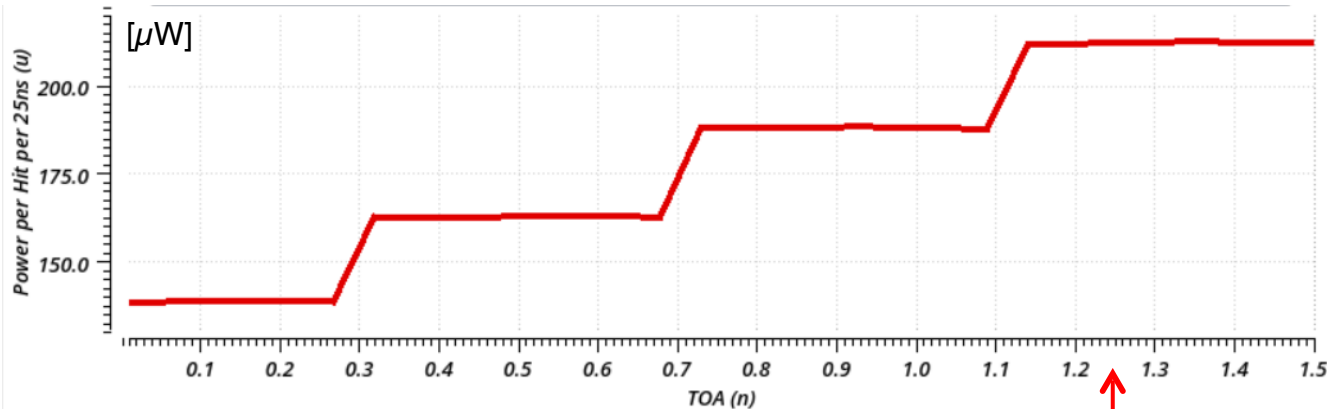
TDC ASIC testing

- Delay cell propagation matches the simulation
- 50ps Time-Over-Threshold (TOT) shows glitches due to parasitics.
 - Traced and fixed in the next ASIC that will embed the TDC
- 6.25ps Time-Of-Arrival shows a curvature due to a missing in-ASIC capacitor
 - Fixed in the next ASIC that will embed the TDC
- Sliding scale techniques works as expected.

Backup

28nm TDC – Power, Conversion Time, Area

- Average power within 25ns window VS TOA (RCX):



- TDC idle consumption (due to leakage): $\sim 1.2\mu W$
- TDC power consumption depends on time-interval being measured
 - For uniformly distributed time-intervals T_i the average power consumption per Hit in a 25ns measurement window is:

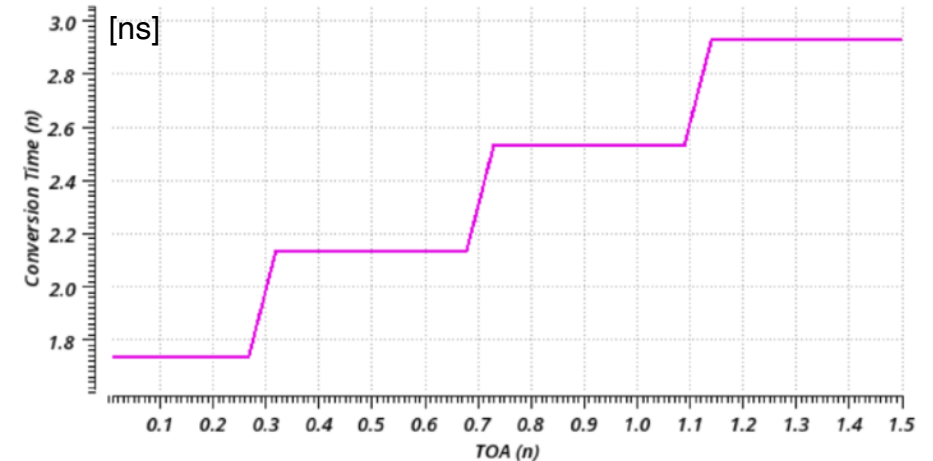
$$P_{\frac{av}{hit}/T_{CK}} = 173\mu W$$

- Average power consumption:

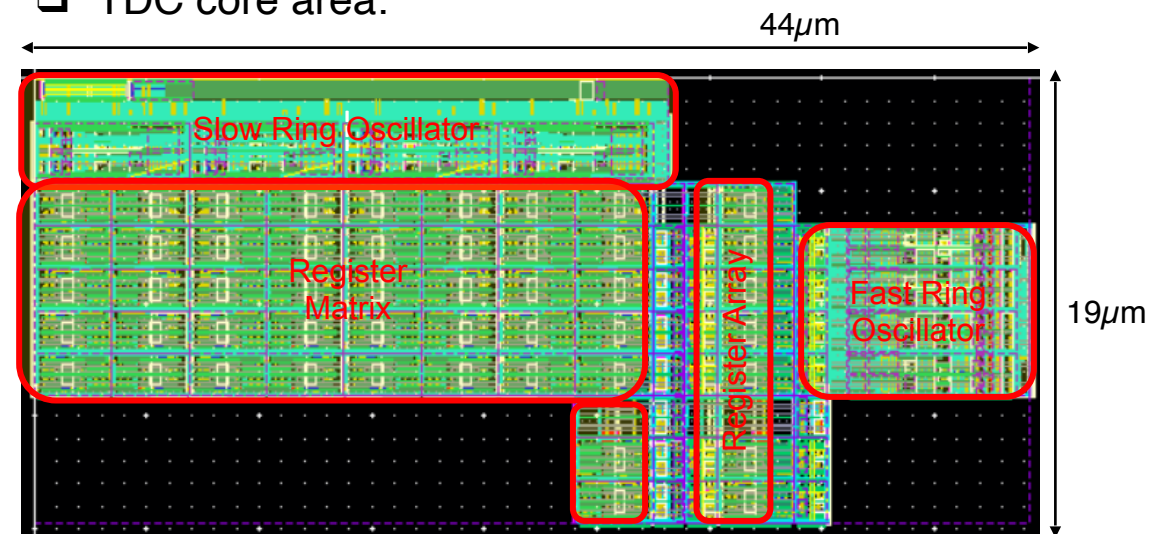
$$P_{av} = 1.2\mu W \cdot (1 - Occupancy) + P_{\frac{av}{hit}/T_{CK}} \cdot Occupancy$$

- For 10% occupancy: $\sim 18.4\mu W$
- For 1% occupancy: $\sim 2.9\mu W$

- Time between Start signal and the end of conversion VS TOA (RCX):

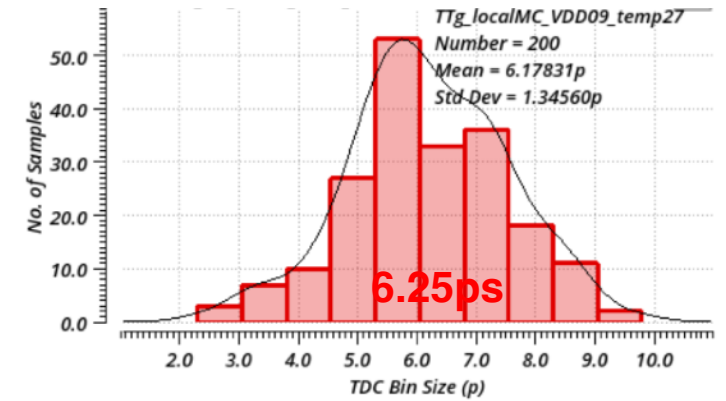
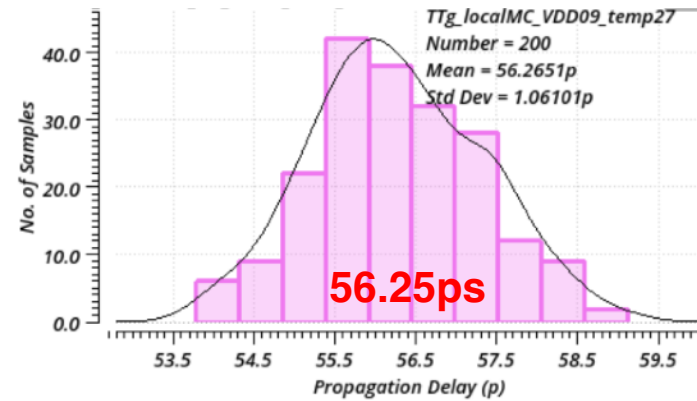
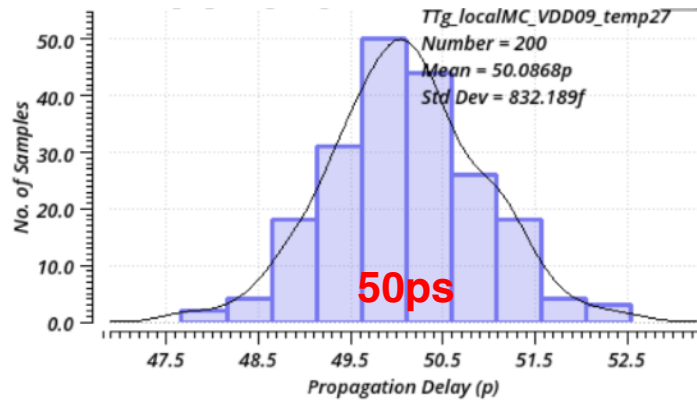


- TDC core area:

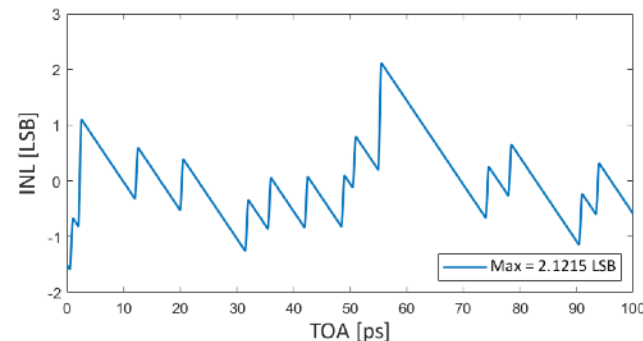
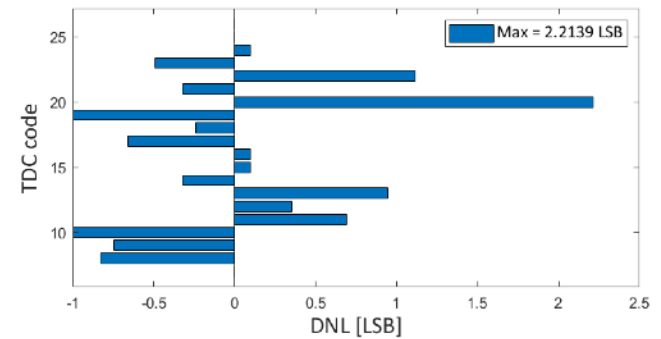
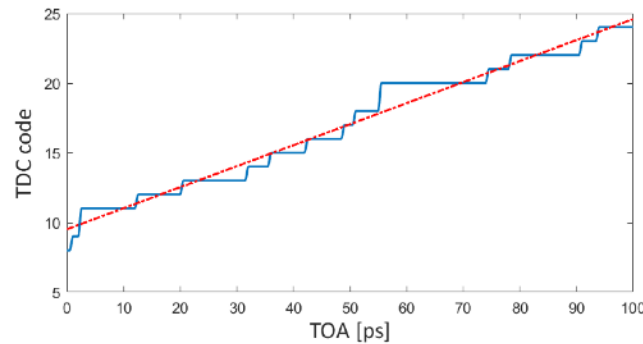


2D Vernier TDC - Mismatch

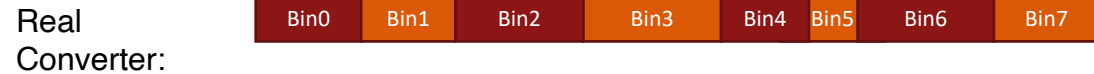
□ Delay Cell Mismatch (RCX, Global Corner + Local MC, N° of runs: 200):



□ 2D Vernier TDC characteristics with mismatch (Global Corner + Local MC, one iteration):



Linearity Improvement: Sliding-Scale

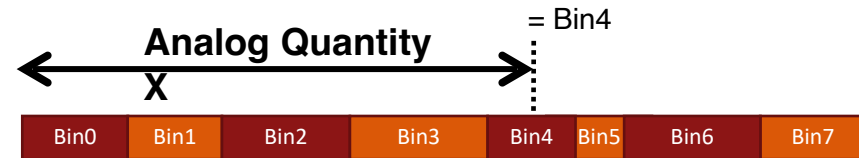


[1] C. Cottini, **E. Gatti**, and V. Svelto, "A new method for analog to digital conversion," Nucl. Instr. Meth., vol. 24, p. 241, Aug. 1963.

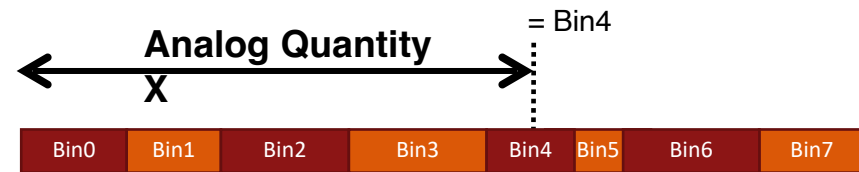
[2] **E. Gatti**, P. F. Manfredi, and D. Marino, "Analysis and characterization of cyclic-scale compensated analog-to-digital converters," Nucl. Instrum. Methods, vol. 165, no. 2, pp. 225–230, Oct. 1979.

Regular Converter:

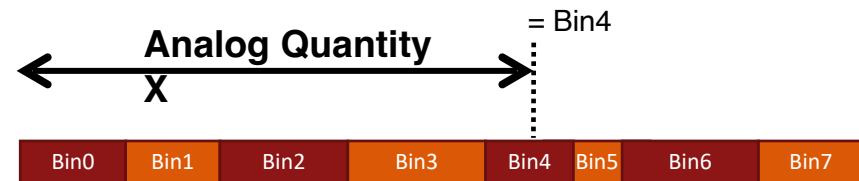
Measurement1:



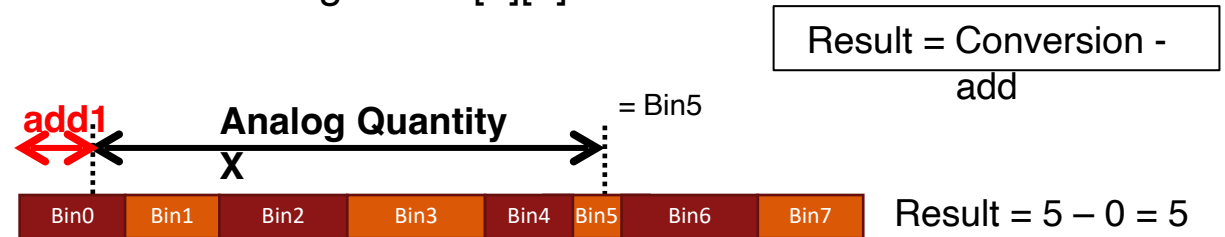
Measurement2:



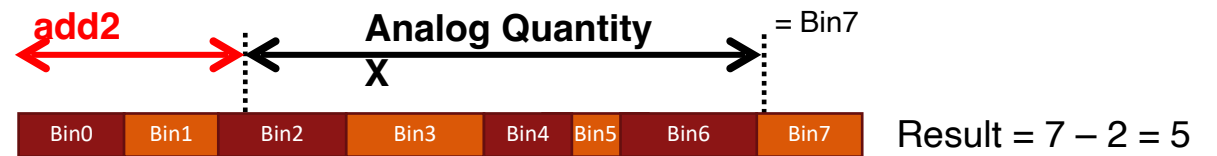
Measurement3:



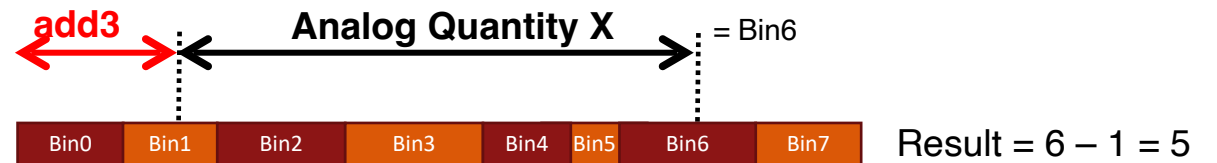
Sliding Scale [1][2]



Result = 5 - 0 = 5



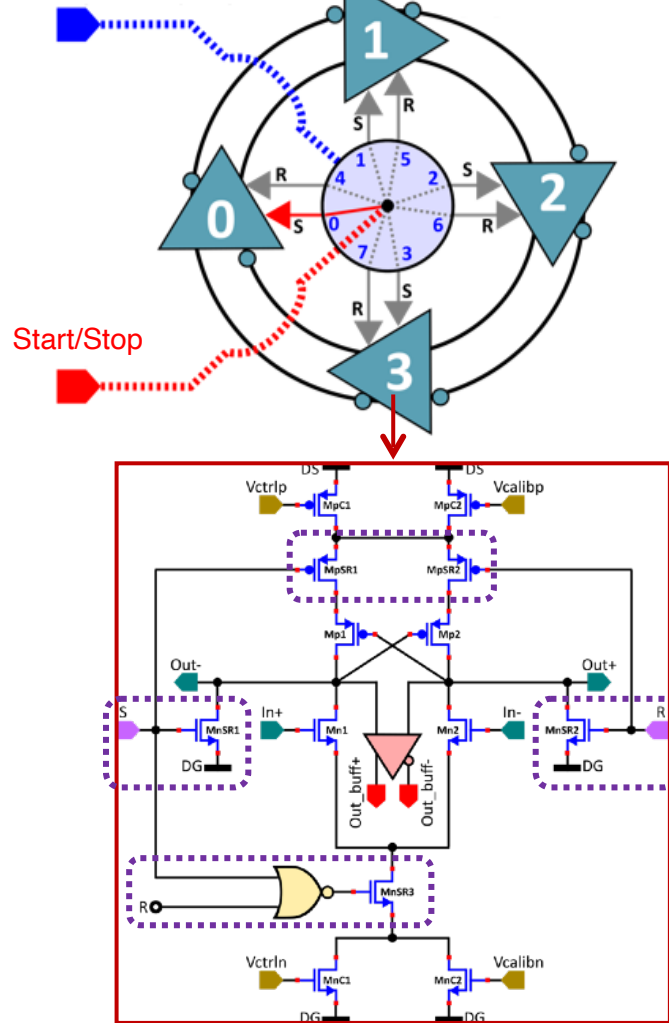
Result = 7 - 2 = 5



Result = 6 - 1 = 5

Sliding-Scale Implementation

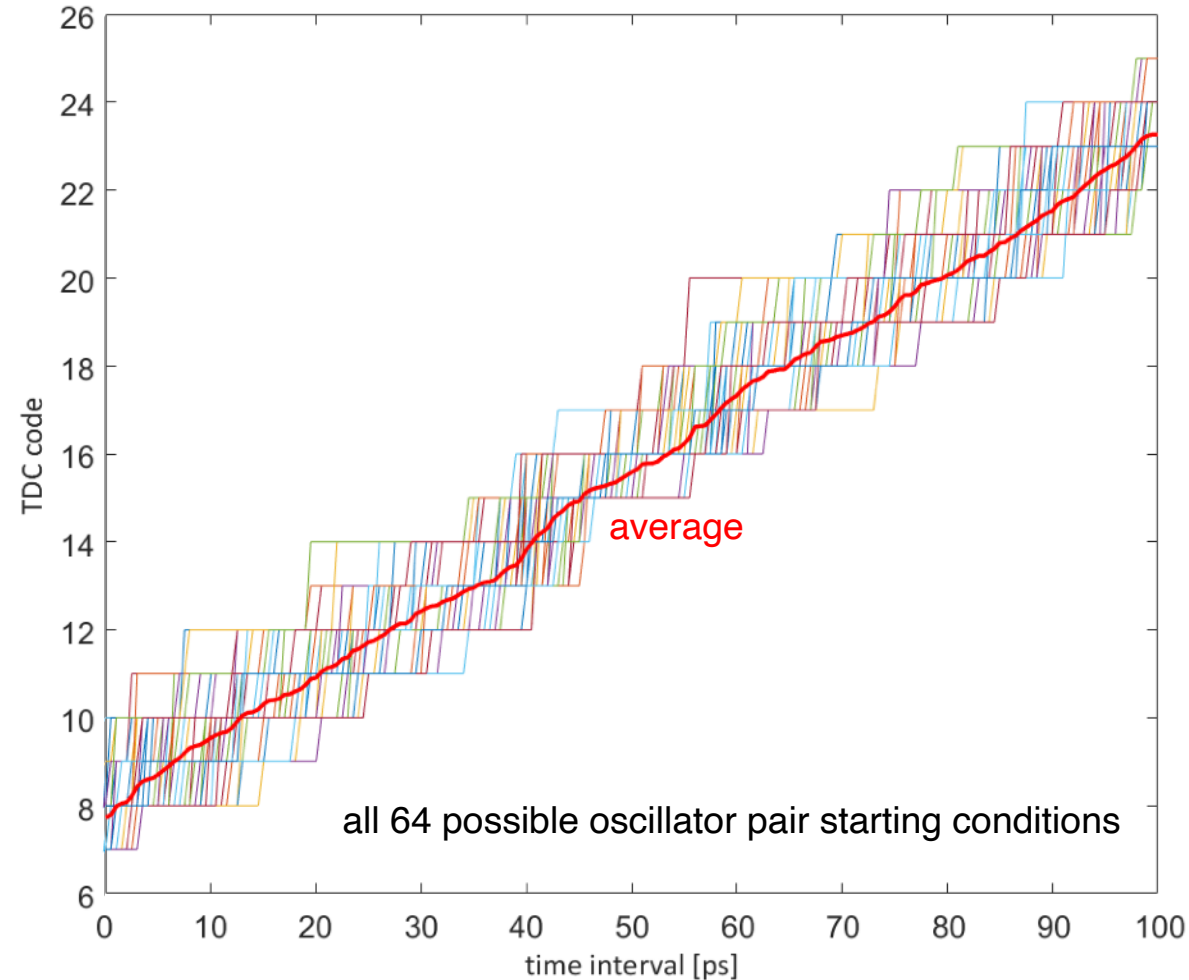
Start/Stop Select (3bit)



Sliding-Scale technique:

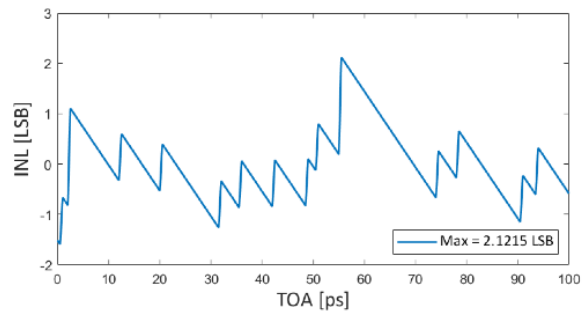
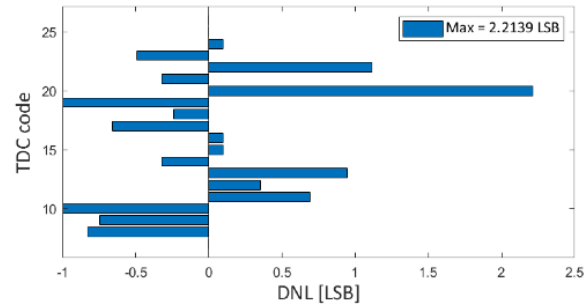
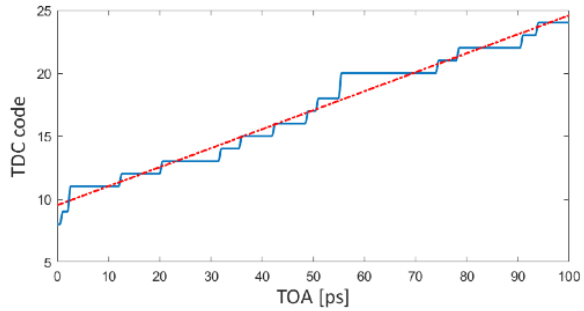
- Both ring oscillators have programmable starting conditions via delay cell **set/reset** function;
- Starting conditions randomly selected each measurement cycle and corresponding values subtracted from the conversion result;
- Same time intervals converted with different parts/bins of the TDC conversion characteristics;

TDC characteristics with mismatch:

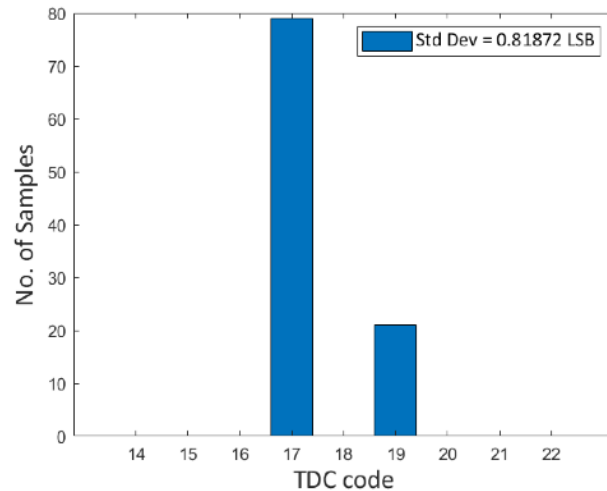


28nm TDC Architecture – Sliding Scale

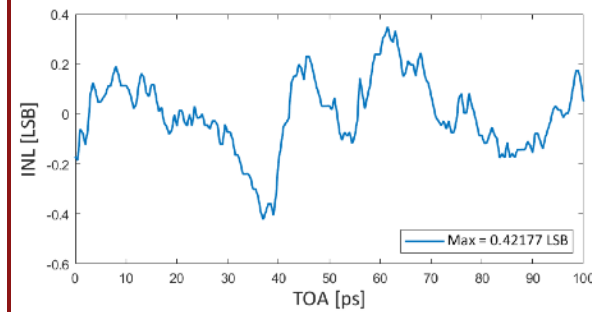
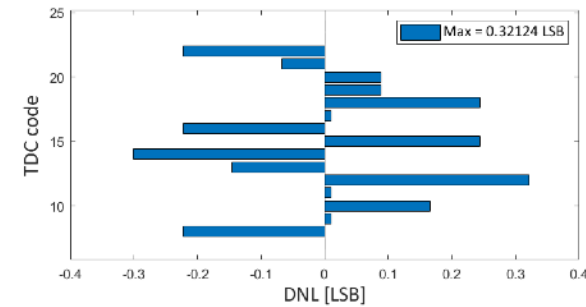
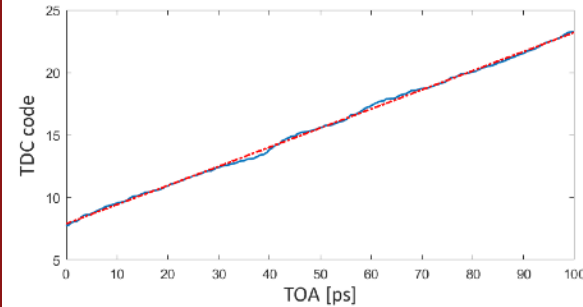
TDC characteristics with sliding scale disabled



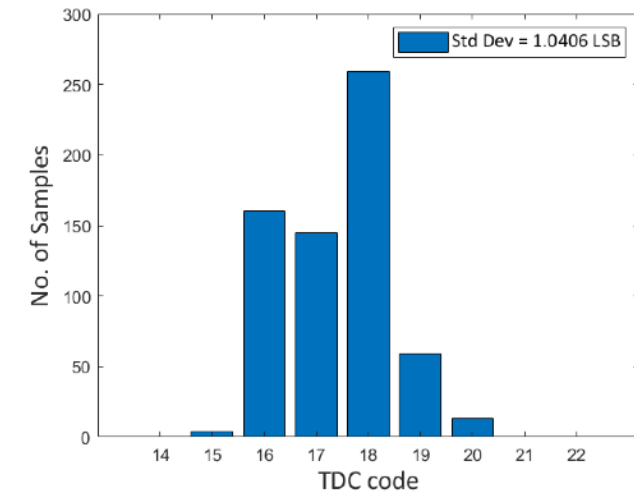
Transient noise simulation – sliding scale disabled:



Equivalent TDC characteristics with sliding scale enabled



Transient noise simulation – sliding scale enabled:



Sliding scale transforms the non-linearities into stochastic variable thus effectively improving the conversion linearity at the expense of worsening single-shoot precision: